1. Objectives

The objective of this mini-project is to design and build a NMOS common-source amplifier. The design goal is to maximize the amplification and to explore the limits of voltage gain using a single transistor. In addition, you will design the amplifier according to specifications of lower 3-dB cut-off frequency and input impedance. Specifically, you will:

1. Learn to design a common-source amplifier using a NMOS transistor
2. Learn what parameters determine the voltage gain and how to maximize it.
3. Learn the low-frequency response of the amplifier
4. Verify the design with PSpice
5. Build the amplifier
6. Measure the amplifier's characteristics

2. Background

The common-source amplifier is shown in Figure 1 below. It is a similar amplifier as the one you used in the previous lab. During this lab, you analyzed the biasing circuit and measured the voltage gain. The goal of the new lab assignment is to design the amplifier, build and test it.

![Common-Source Amplifier with a NMOS transistor.](image)

Figure 1: Common-Source Amplifier with a NMOS transistor.
2.1. Voltage Gain, Input and Output resistance

We already know that voltage gain $G_V$ is given by

$$G_v = -\frac{R_g}{R_g + R_{\text{sig}}} \cdot g_m (R_D \parallel R_L \parallel r_o) \approx -\frac{R_g}{R_g + R_{\text{sig}}} g_m (R_D \parallel R_L) \tag{1}$$

The open-circuit overall voltage gain is given by

$$G_{vo} = -\frac{R_g}{R_g + R_{\text{sig}}} g_m R_D \tag{2}$$

in which $g_m$ is the transconductance given by

$$g_m = k_n \cdot \frac{W}{L} (V_{GS} - V_i) = \sqrt{2I_D k_n \cdot \frac{W}{L}} \tag{3}$$

The input resistor is $R_{in} = R_{G1} || R_{G2}$ and output resistor $R_{out} = R_D$.

2.2 Low-Frequency Response

The frequency response at low frequencies is limited by the coupling capacitor $C_{C1}$ and $C_{C2}$, and the bypass capacitor $C_S$. Assuming that the poles associated with each capacitor does not influence each other one can easily find the poles. The expression of the pole associated with capacitor $C_i$ can be written as,

$$f_{3\text{dB}} = \frac{\omega_{3\text{dB}}}{2\pi} = \frac{1}{2\pi} \cdot \frac{1}{2\pi C_i R_{eq}} \tag{4}$$

in which $R_{eq}$ is the equivalent resistor seen over the terminals of capacitor $C_i$ when the other capacitors are short circuited. Let us apply this for each of the three capacitors $C_{C1}$, $C_{C2}$ and $C_S$:

$$f_{pC1} = \frac{1}{2\pi C_{C1} (R_g + R_{\text{sig}})} \tag{5}$$

$$f_{pC2} = \frac{1}{2\pi C_{C2} (R_D + R_L)} \tag{6}$$

$$f_{pC_s} = \frac{1}{2\pi C_S (R_s \parallel \frac{1}{g_m})} = \frac{1}{2\pi C_S} \cdot \frac{R_s}{1 + g_m R_S} \approx \frac{g_m}{2\pi C_S} \tag{7}$$
The simplification is expression (7) is valid as long as $R_S \gg 1/g_m$. These three formulas can be used to find the values of the three capacitors, as explained below.

2.3 Selecting the capacitors

One notices that the resistor seen by the bypass capacitor is $1/g_m$ which is a relatively small value. As a result, we will usually make the pole associated with $C_S$ to be the 3-dB frequency $f_L$.

$$f_L = f_{pC_S} = \frac{1}{2\pi C_S (R_S \parallel 1/g_m)} = \frac{1}{2\pi C_S \frac{R_S}{1 + g_m R_S}} \approx \frac{g_m}{2\pi C_S}$$

The poles associated with the coupling capacitors are usually made about 10 times smaller than the one caused by the bypass capacitor. Since the resistors $R_G$ and $R_D$ are pretty large, the capacitors are not as large as the bypass capacitor.

$$f_{pC1} = f_{pC2} = f_L/10$$

3. Pre-lab Assignment

Your task is to design a NMOS common-source amplifier, as shown in Figure 1 with maximum gain. The amplifier has the following specification:

- Maximize the open-circuit voltage gain $G_{vo}$; you should get an amplification of at least $-25 \text{ V/V}$ but not larger than $-50 \text{ V/V}$ without a load resistance $R_L$.
- Input impedance $10\text{Kohm}$ or larger, the
- Lower 3-dB frequency $f_L$ should be maximum 50 Hz and
- The output swing should be at least $5\text{Vpp}$.

The NMOS transistor has the following characteristics: $V_t=1.2\text{V}$; $k_n \cdot W/L=0.7\text{mA/V}^2$. $\lambda = 0.004\text{V}$. The signal resistor $R_{sig} = 50 \text{Ohm}$.

3.1 Reading

Review the background material of the previous lab (MOSFET Lab2 - Biasing and the Common Source Amplifier) or read the sections "Common-Source Amplifier" in the textbook Microelectronic Circuits by Sedra-Smith (5th ed), section 4.7.3, and "Frequency Response of the CS Amplifier", sections 4.9.1 and 4.9.3.

3.2 Hand calculations: Design

a. Find: the values of the resistors, and DC current $I_D$. There are many possible solutions that will fulfill the spec for the mid-frequency amplification. Make judicious choices and use the rule of thumbs when appropriate.
**Hint**: Write down the expression for the amplification as a function of $I_D$ and $R_D$. This gives one relationship between $I_D$ and $R_D$. Is there another relationship you can come up with that will help you find the values of $I_D$ and $R_D$? You should select values for the resistors that are available in the lab: see list of available components.

b. Once you have determined the DC current and all resistors find the transconductance $g_m$ and small signal output resistance $r_o$ of the amplifier. Also, verify that the amplification $G_{vo}$ is what you intended it to be.

c. What is the minimum drain voltage and corresponding output swing at the drain? Also calculate the DC power dissipation.

d. What is the input $R_{in}$ and output resistance $R_{out}$ of the amplifier? Now, add a load resistor $R_L$ of 15kOhm. What is the overall voltage gain $G_V$? Calculate the DC power dissipation. Notice the drastic effect of adding a load resistance on the amplification? Is this drastic dependence on the load resistance related to the fact that your open-circuit amplification is very large? Is there a way to reduce the influence of the load resistance?

e. Determine the values of the coupling capacitor and the bypass capacitor. You can use the procedure outlined in the background section. Select values of the capacitors that are available in the lab.

### 3.3 PSpice simulations

a. Enter the schematic. Do not include the load resistor $R_L$ yet. Use for the NMOS transistor one of the CD4007 transistors (same as the one used in the lab). The model can be found in the ese216lib library. This library can be downloaded from the ESE216 website. Save both the `cd4007.lib` and `CD4007.OLB` in your directory. Add the library path to the PSpice and the Simulator (see Adding Vendor Libraries in the PSPICE Primer).

b. Do a Bias simulation and verify all DC voltages and DC currents. Compare these values with the calculated one.

c. Next apply a sinusoidal input signal of 0.05 Vampl and 5kHz. Do a transient simulation and display the signal at the drain. Verify that the voltage amplification is close to the specified one.

d. Now add a 15 kOhm load and find the amplification $G_V$. Compare it with the hand calculations.

e. Do an AC analysis and plot the magnitude of the voltage gain $G_{vo}$ and $G_V$. Do a sweep from 0.1 Hz up to 1MHz (note: Spice uses MEG for Mega and not M). Determine $f_L$. Where are the lower poles located? Do they correspond to the one you used to design the circuit?
3.4 Summarize

Summarize your results in table format shown below

<table>
<thead>
<tr>
<th>Specification/Calculation</th>
<th>Simulated results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{vo}$ (V/V)</td>
<td></td>
</tr>
<tr>
<td>$G_v$ (V/V)</td>
<td></td>
</tr>
<tr>
<td>$R_{in}$ (kOhm)</td>
<td>---</td>
</tr>
<tr>
<td>$R_{out}$ (kOhm)</td>
<td>---</td>
</tr>
<tr>
<td>$V_{Dmin}$ (V)</td>
<td>---</td>
</tr>
<tr>
<td>Max. output swing (Vpp)</td>
<td>---</td>
</tr>
<tr>
<td>Power dissipation (mW)</td>
<td></td>
</tr>
<tr>
<td>$f_L$ (Hz)</td>
<td></td>
</tr>
</tbody>
</table>

4. In-Lab Experiments

4.1 Parts

HFC4007UB MOS transistor array ([data sheet](#) from ST Microelectronics)
- Resistors
- Capacitors
- Oscilloscope with FFT module
- Digital multimeter (Voltage and Current meter)

4.2 Procedure

a. Build the amplifier you designed as part of the prelab shown in Figure 3 below. Use the HFC4007 (or CD4007) MOSFET transistor array, shown in the Figure 3 below. It may be convenient to use a 50kOhm potentiometer for $R_{G2}$. Do not add $R_L$. 
b. Measure the DC voltages \(V_D, V_G\) and \(V_S\) and the current \(I_D\). Compare these values with the one of your design. Measure also the total current supplied by the power supply. What is the corresponding power dissipation?

c. Do not connect a load resistor \(R_L\) yet. Apply a sinusoidal input signal of amplitude of 50mV and frequency of 5 kHz. Measure the output voltage. If the output is distorted you need to decrease the input amplitude (use a voltage divider if needed). Verify the open-circuit voltage gain \(G_{vo}\). It is possible that the amplification is somewhat off from the calculated one. This is due to the fact that the actual transistor is different from the one used in the calculations and the simulations. As long as you get an amplification about 40V/V it should be ok. Also, take the FFT of the output signal and determine the total harmonic distortion THD.

d. Increase the input signal to determine the maximum output signal swing before noticeable distortion occurs? Take the FFT of the maximum output signal and determine its total harmonic distortion THD. How much has the THD increased as compared to the one measured in the previous section?

e. Adjust the input amplitude to 50mV and vary the frequency of the input signal between 1Hz and 1MHz. These measurements are done without a load resistor \(R_L\). Take about 10 measurement points per decade around the low frequency poles. Determine \(f_L\) Ones the frequency response is flat you can take one or tow measurements per decade (e.g. 1kHz, 4kHz, 10kHz, 40kHz, 100kHz, etc) up to the point where the amplitude starts to decrease. Measure the high frequency 3dB point, \(f_H\). Take several measurements around this frequency so that you can draw the Body plot. What is the bandwidth and the gain-bandwidth product of your amplifier?
f. Apply a load resistor of 15kOhm and determine the voltage gain $G_v$. Compare the result with the one from the pre-lab.

Follow the guidelines for writing the report. In addition, the report should include:

a. Summary of the design process and results.

b. Experimental results and a comparison with the design values. If there are differences explain what may have caused these differences between the calculated and measured values. Is there an disadvantage of having such a large amplification (consider bandwidth, gain-bandwidth, output impedance, load dependency).

c. Table summarizing the calculation, PSpice and measured results.

d. Discussion.

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