A LOW-VOLTAGE/LOW-POWER SECOND-ORDER $\Delta\Sigma$ MODULATOR WITH SIGNAL ADAPTIVE CONTROL ARCHITECTURE

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ABSTRACT

A Signal Adaptive Control (SAC) architecture for a second-order $\Delta\Sigma$ modulator ($\Delta\Sigma M$) design is presented. The proposed architecture effectively reduces the power dissipation and the harmonic distortion of the first stage integrator in the modulator. The essence of this architecture, is to switch off the DAC feed-back signal to the first stage during some iterations, and to compensate the signal at the input of the second stage, in an adaptive manner. Transistor-level simulations have shown the feasibility of this architecture.

1. INTRODUCTION

Recently, work [1,2] has been directed towards low-voltage /low-power $\Delta\Sigma M$ designs with switched op-amp techniques. For a better power-resolution-speed trade-off in the $\Delta\Sigma M$ design, the in-band quantization noise should be less than the in-band thermal noise. Even when this is satisfied, the first stage SC integrator usually consumes 60%-75% of the total power of the modulator. The reason for this observation is discussed as follows. For low-voltage design, lowering the supply voltage inevitably reduces the linear signal swing, i.e. reduces the achievable dynamic range. In the $\Delta\Sigma M$ SC circuit, the dynamic range is limited by the supply voltage at the upper end and by noise at the lower end. It is the noise at the input node of the modulator that dominates the total noise of the modulator. This noise is proportional to kT/C_s, in which C_s is the sampling capacitance at the input node, k is the Boltzmann constant, T is the absolute temperature. Thus, for a specific dynamic range and a reduced signal swing, the capacitors in the first integrator stage need to be large enough to suppress the noise, requiring a large current consumption and a large die area. The capacitors used in the following stages can be much smaller, because these capacitor sizes are determined by matching requirements rather than the noise. Furthermore, for a certain signal level, the integrator linearity degrades when the supply voltage is lowered. To save power and improve performance further, it is key to decrease the power and reduce the distortion at the first stage. For this purpose, this paper presents an architecture level solution, using a Signal Adaptive Control (SAC) structure. The feasibility of the SAC architecture has been shown with Hspice transistor level simulations.

2. THE PROBLEMS IN THE CONVENTIONAL ARCHITECTURE

In the conventional second-order $\Delta\Sigma M$ (Fig.1), the first stage integrates the signal $x[n]-v_f[n]$. The input signal x is oversampled, therefore it can be considered constant for several successive iterations. The DAC feedback signal v_f, however, takes the value of $+V_{ref}$ or $-V_{ref}$ in any iteration, depending on the comparator output. As a result, the input to the first integrator stage can be as large as $2V_{ref}$ and the output changes between two successive iterations $\Delta u_n = u[n]-u[n-1]$ are large. This results in a large amount of power consumption in the first stage. That is, if a class-AB OTA is used, its dynamic power dissipation is proportional to $C_L(\Delta u)^2$, where C_L is the effective load of the first stage OTA. If a class-A OTA is used, the required slew rate is proportional to $\max(\Delta u_n)$, the stand-by current must be large enough to accommodate the slew rate to satisfy the integration settling requirement. Meanwhile, large capacitances are used at the first stage to suppress kT/C noise, increasing the power dissipation in the first stage.

In the low-voltage $\Delta\Sigma M$ design, the configuration of the first stage shown in Fig.2 are usually used. In this configuration, the OTA input common mode signal can be set at ground, to minimize the voltage supply of the OTA and maximize the over-drive voltage ($v_{gs}-V_T$) of the switches used at the input node. The disadvantage of the configuration in Fig.2 is that the DAC feed-back paths with C_F and switches are introduced. These feed-back paths increase the effective load capac-

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itance of the OTA, which is shown in Eq. (1).

$$C_L = C_S + C_F + \frac{(C_I + C_S + C_F)C_l}{C_I} \qquad (1)$$

where C_S, C_F, C_I are the sampling capacitance, the feed-back capacitance, and the integrating capacitance respectively, C_l includes the sampling capacitance of the common-mode feedback circuits and the sampling capacitance of the next stage (if switched op-amp technique is used). The introduction of the DAC feed-back paths also boosts the kT/C noise at the input node.

To further improve the performance and reduce the power dissipation of the $\Delta\Sigma M$, in this paper we propose a Signal Adaptive Control (SAC) architecture. In this architecture, we show that the feed-back signal v_f to the first stage is not necessary in all integration iterations.

3. SAC ARCHITECTURE

In the conventional $\Delta\Sigma M$ (Fig.1), the DAC feedback signal v_f to the first stage exhibits redundancy. The basic idea of SAC architecture is to find opportunities to cancel $v_f[n] = +V_{ref}(or - V_{ref})$ with $v_f[n+1] = -V_{ref}(or + V_{ref})$ to the first stage during successive iterations, and to ensure that the modulator output is not affected by such actions. This operation is realized by adaptively controlling the switches S1, S2, S3 and S4 shown in Fig.3.

The principle of the SAC architecture is based on the behavioral analysis of the conventional $\Delta\Sigma M$, which is usually characterized by the output traces of the two SC integrators. Fig.4 shows a snapshot from a Matlab simulation, which demonstrates the SAC operation. On the phase one of $[2T, 3T]$ and $[3T, 4T]$, the comparator outputs are '-' and '+' respectively, since $v[2T] < 0$ and $v[3T] > 0$. The conventional DAC will feed back a $-V_{ref}$ in $[2\frac{1}{2}T, 3T]$ and feed back a $+V_{ref}$ in $[3\frac{1}{2}T, 4T]$ to the input nodes of both the integrators. The first stage output tracks 'AbC' as shown in Fig.4(c). In the SAC modulator, the above $-V_{ref}$ and $+V_{ref}$ are cancelled by switching off S1 (Fig.3) in $[2\frac{1}{2}T, 3T]$ and $[3\frac{1}{2}T, 4T]$. The first stage output tracks 'ABC' instead of 'AbC'. To ensure that the modulator output is not affected by the above action, the signal difference between B and b is compensated at the input node of the second stage, by switching on S2 (Fig.3) in $[3\frac{1}{2}T, 4T]$.

Similarly, if two iterations are needed for the second stage output to return from the negative value to the positive value (for example, $t = 4T$ and $t = 5T$ in Fig.4(c)), the SAC operation switches off the feed-back signal $-V_{ref}$ to the first stage twice. This is cancelled by not applying $+V_{ref}$ to the first stage twice respectively at $t = 6T$ and $t = 7T$. Again,the trace of the second stage output is unaffected due to a compensating signal at the input of the second stage, keeping the modulator output the same as the conventional modulator. It can be shown that, for $x > 0$, when trace $v[n]$ becomes negative, it takes at most three iterations before it returns to positive [3]. For $x < 0$, the situation behaves in the same way symmetrically. Thus, the SAC operation switches off S1 at most three iterations successively (for example, $t = 10T, 11T, 12T$ in Fig.4(c)). The control of switch S1 depends on the modulator output at phase one of the current iteration and the modulator output of the previous iteration. The control of switches S2, S3 and S4 depends on the successive iteration times in which S1 is switched off. Switches S2, S3, S4 are all closed in $[12\frac{1}{2}T, 13T]$ to compensate the signal at the input of the second integrator.

4. ADVANTAGES OF THE SAC ARCHITECTURE

Reduce Power Dissipation. If a class-AB OTA is used, its dynamic power dissipation is proportional to $C_L(\Delta u)^2$. The SAC operation reduces the output changes Δu of the first stage between two successive iterations (not for all successive iterations, but for some of them). During the off-switching of the DAC feed-back path, C_F does not contribute to the OTA output effective load. Simulation shows that the dynamic power of the first stage can be reduced by 2/3 when the input is a sinusoid signal with an amplitude of $0.7V_{ref}$ and a frequency of $0.001f_s$, where V_{ref} is the reference voltage and f_s is the sampling frequency of the modulator.

If a class-A OTA is used, the SAC operation reduces the required slew rate (SR) of the OTA to be half of the SR required in the conventional modulator. This will reduce the stand-by current and the power dissipation of the class-A OTA considerably. In a $\Delta\Sigma M$, the integration settling process is more likely limited by the slew rate (resulting in nonlinear settling) than by the gain-bandwidth product GBW (linear settling). The required slew rate is proportional to the maximum input voltage to the integrator. The maximum input can be as large as $2V_{ref}$ in the conventional architecture, but it is reduced to be V_{ref} in the SAC architecture.

Improve Modulator Linearity. In an integration process, the nonlinear settling exists because of non-ideal factors, which causes distortion. If referring to the input node, the time-domain error due to distortion can be expressed as follows [4].

$$e_n = \sum_{i=0} c_i(x[n-1] - v_f[n-1])^i \qquad (2)$$

where x and v_f are the input and the DAC feed back

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signal in the modulator, coefficients c_i can be determined by simulation or measurements for a specific design. If a fully differential schematic is used, the even-number index coefficients are much smaller than the odd-number index ones. For a certain integrator design, the SAC operation reduces the integrator input $(x - v_f)$ by switching off feed back for some iterations, therefore, it reduces the distortion in those iterations. Fig.5 shows this effect with a comparison between the conventional architecture and the SAC architecture.

Minimize kT/C Noise. Compared to the conventional $\Delta\Sigma M$, the difference at the input node of the SAC architecture is to adaptively control the switch in the DAC feedback path. Thus, the kT/C noise at the input node of the new modulator, which is the dominating factor limiting the performance of the whole modulator, is not larger than the noise of the conventional one. As a matter of fact, the kT/C noise contributed by the switches in the feed-back path can be ignored when this path is switched off. This is because, in current CMOS technologies, the on and off resistances of the MOS switches differ up to ten orders of magnitude. The noise power due to an off-channel is concentrated at extremely low frequencies. Therefore, this noise contribution can be considered as a slowly changing offset voltage and can be ignored in the signal band. The DAC feedback path is kept off for almost all iterations when the input signal is small, only the kT/C noise due to the sampling path contributes to the signal band. Therefore an extra SNR gain is obtained when the input signal is small, as shown in Fig.6.

The essence of the SAC architecture, is to switch off the DAC feedback to the first stage for some iterations in an adaptive manner. To not affect the modulator output, the signal is compensated at the input of the second integator stage. The signal load at the first stage is considerably reduced at the cost of increasing a very small load capacitance at the second stage. However, the total power is reduced and the whole performance is improved because the size of the second stage is much smaller than the first stage, but also because the first stage performance determines to a large extent the overall system performance. The noise, and the mismatching error introduced at the second stage, are all suppressed with the first-order noise shaping.

5. SIMULATION RESULTS

A transistor level simulation of the proposed architecture has been performed. In the Hspice simulation, a 0.35μm standard CMOS technology with $V_{T,n} = 0.6$ V, $V_{T,p} = -0.8$ V is used. The $\Delta\Sigma M$ is powered with a 1.2 V single polarity supply. The sampling frequency is 500 kHz. The over sampling ratio (OSR) is 64. The power density function plots of the conventional and the SAC architecture are shown in Fig.5. The SNDR versus input plot is shown in Fig.6. A dynamic range (SNR) of 72 dB has been obtained within a 3.4 kHz bandwidth. The peak signal to noise distortion ratio (SNDR) is 69 dB, which corresponds to 11.5-bit resolution. The SAC modulator consumes 21 μW power, while the conventional one consumes 37 μW.

6. CONCLUSION

A signal adaptive control (SAC) architecture for the second-order $\Delta\Sigma M$ design is presented. This architecture effectively reduces the power dissipation and improves the performance of the first stage in the modulator. The essence of this architecture, is to switch off the DAC signal to the first stage for some iterations, and to compensate the signal at the input of the second stage, in an adaptive manner. The feasibility of the SAC architecture has been shown with transistor level simulations.

7. REFERENCES

[1] V. Peluso, M. Steyaert, and W.Sansen, "A 1.5V-100μW $\Delta\Sigma$ modulator with 12-b dynamic range using the switched-opamp technique," *IEEE J. of Solid-State Circuits*, 32(7):943–952, July 1997.

[2] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900 mV - 40μW $\Delta\Sigma$ modulator with 77 db dynamic range," *Proc. ISSCC*, San Francisco, CA, Feb. 1998.

[3] Ronan Farrell and Orla Feely, "A novel approach to bounding the integrator output of second order sigma-delta converters," *Proc. IEEE ISCAS*, Vol.1, pp: 521–524, 1996.

[4] Guangming Yin and Willy Sansen, "A high frequency and high-resolution fourth-order $\Sigma\Delta$ A/D converter in BiCMOS technology," *IEEE J. of Solid-State Circuits*, 29(8):857–865, August 1994.

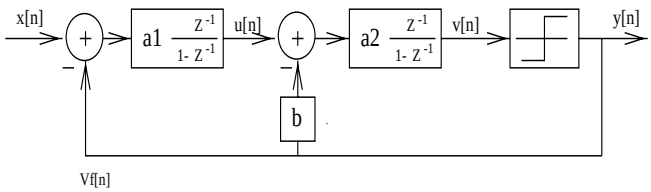

Figure 1: The block diagram of the conventional second-order $\Delta\Sigma M$.

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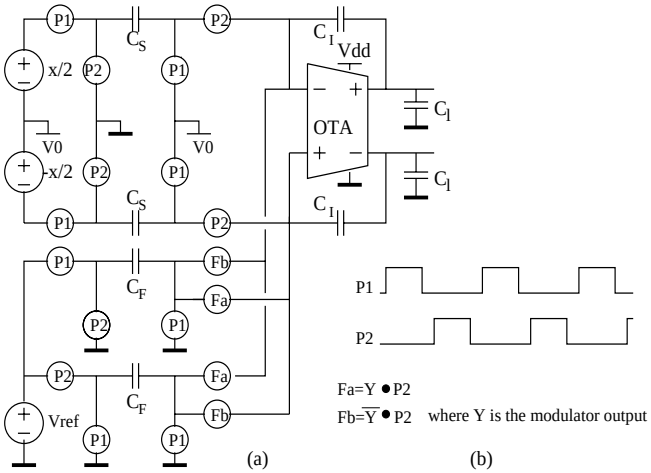

Figure 2: (a) A single-polarity reference SC integrator; (b) a non-overlapping two-phase clock and control signals.

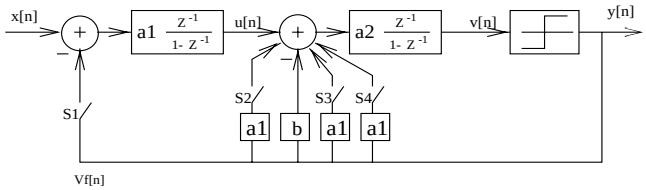

Figure 3: The block diagram of the SAC $\Delta\Sigma M$.

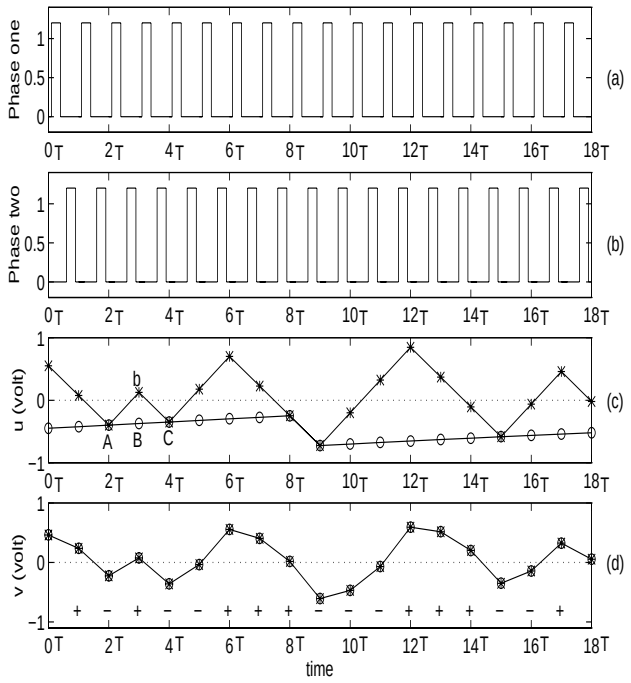

Figure 4: (a)(b)non-overlapping two-phase clock; (c) the first stage integrator output; (d) the second stage integrator output and the comparator output(bottom). (*: conventional modulator, o: SAC modulator, T: sampling period)

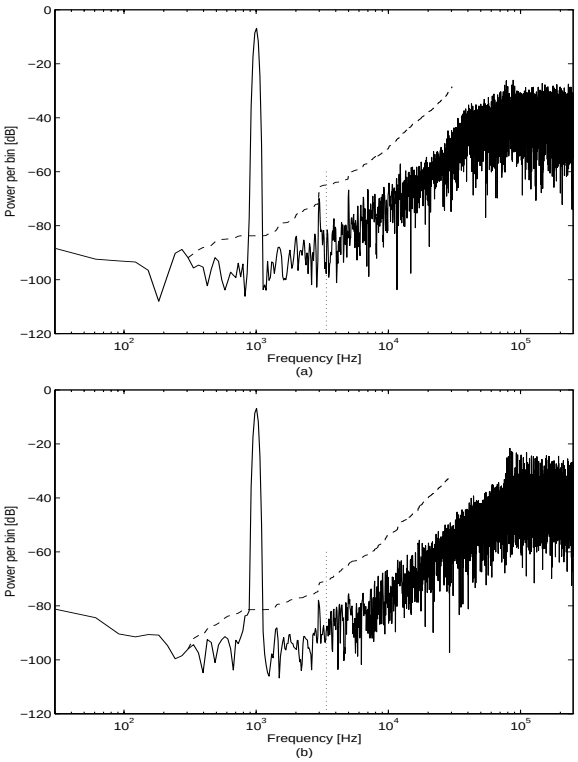

Figure 5: The power density function (solid trace, 16384-point FFT) and the cumulative noise and distortion power (dashed trace, starting from 300Hz) of (a) the conventional architecture; (b) the SAC architecture. The third order distortion is reduced by 5dB with SAC architecture.

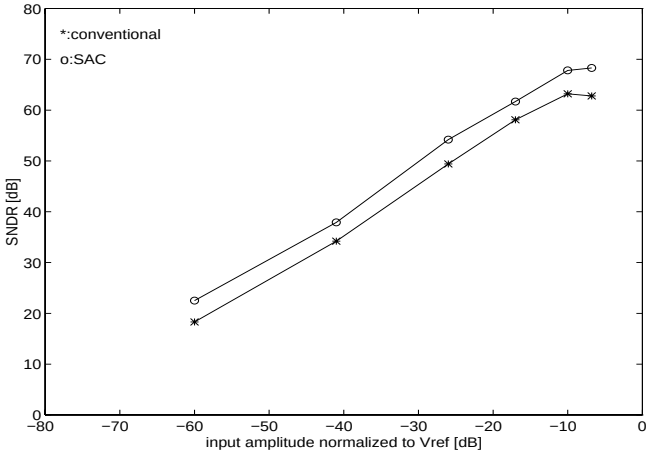

Figure 6: The SNDR versus input amplitude plots for the conventional and the SAC architecture. When input is small, about 4dB SNDR gain is obtained since the kT/C noise is minimized with the SAC architecture. When input is large, around 4-6dB SNDR gain is obtained since the linearity of the first stage is improved with the SAC architecture.

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