A First Generation DPGA

Derrick Chen Ian Eslick Edward Tau Jeremy Brown

André DeHon

Acknowledgments: Support for this research was provided in part by the Advanced Research Projects Agency under Office of Naval Research contracts ONR N00014-91-J-1698 and Rome Labs contract number F30602-94-C-0252.

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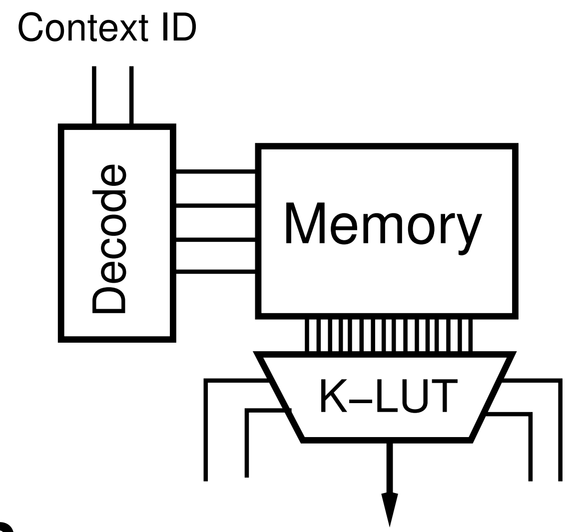
Outline

- What is a DPGA?
- DPGA Application
- DPGA Prototype
  - Highlights
  - Architecture
  - Implementation
- Conclusions

Dynamically Programmable Gate Arrays

- **Multiple Context FPGA**
- **Broadcast a** *Context Identifier*
- **Indirect** *Instruction* **Lookup**
- **Features:**
  - **Rapid Context Switch**
  - **Exploits local, on-chip Bandwidth**
  - **Spatially and Temporally Varying Computation**
  - **High Logic Density**
  - **Reuse gates and wires in time**



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Dynamically Programmable Gate Arrays

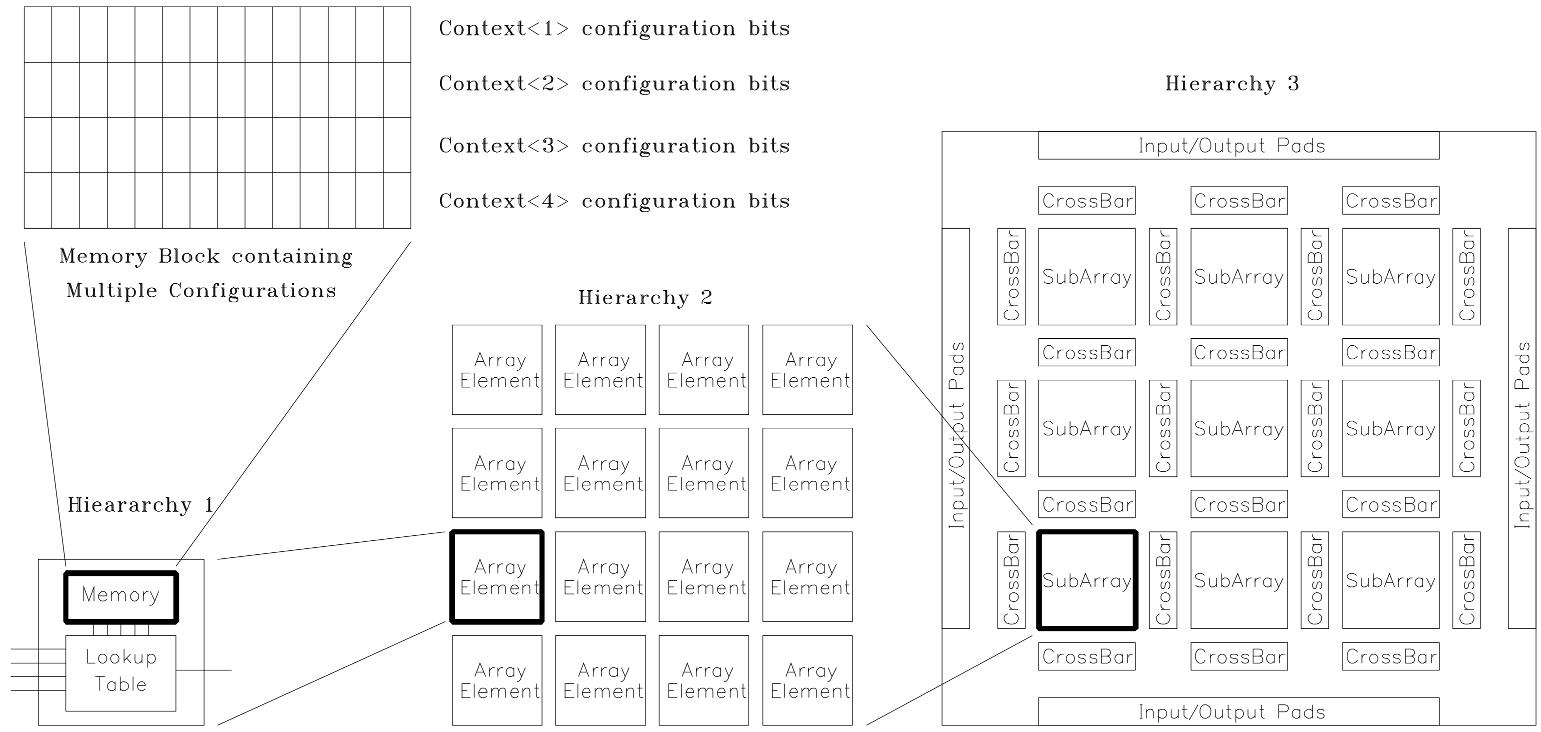
(Application)

- Rapid context switch FPGA
- Time-slice computation
- Temporal Pipelining
- Operation Cache
- Processor Assistance
- Multi-stream SIMD
- Boundary condition handling

DPGA Prototype – Highlights

- 4 on-chip configuration contexts
- DRAM configuration cells
- Automatic refresh of dynamic memory elements
- Non-intrusive background loading
- Wide bus architecture for high-speed context loading
- Two-level routing architecture

DPGA Prototype – Overview

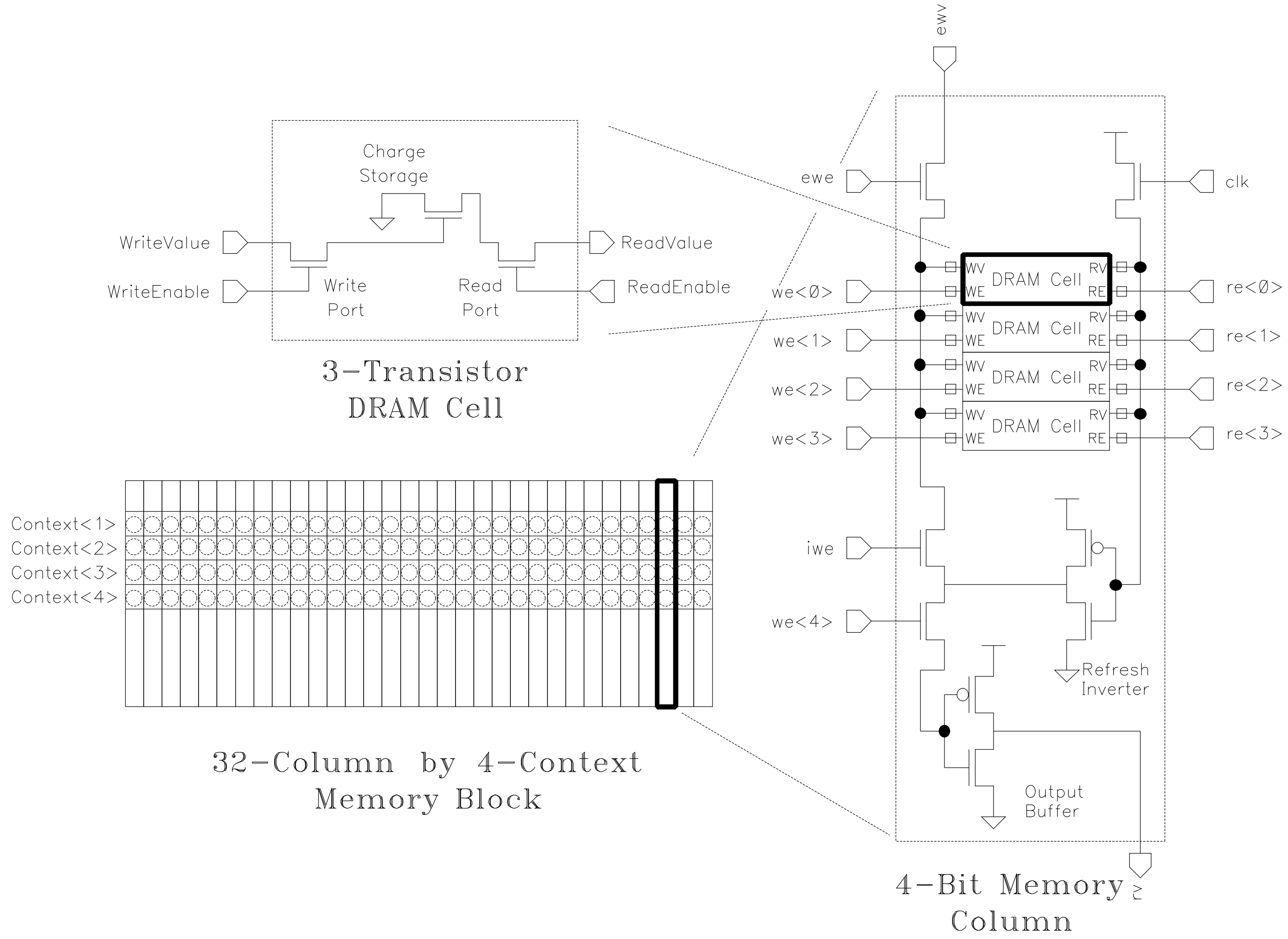


Array Element
4–Input Lookup Table

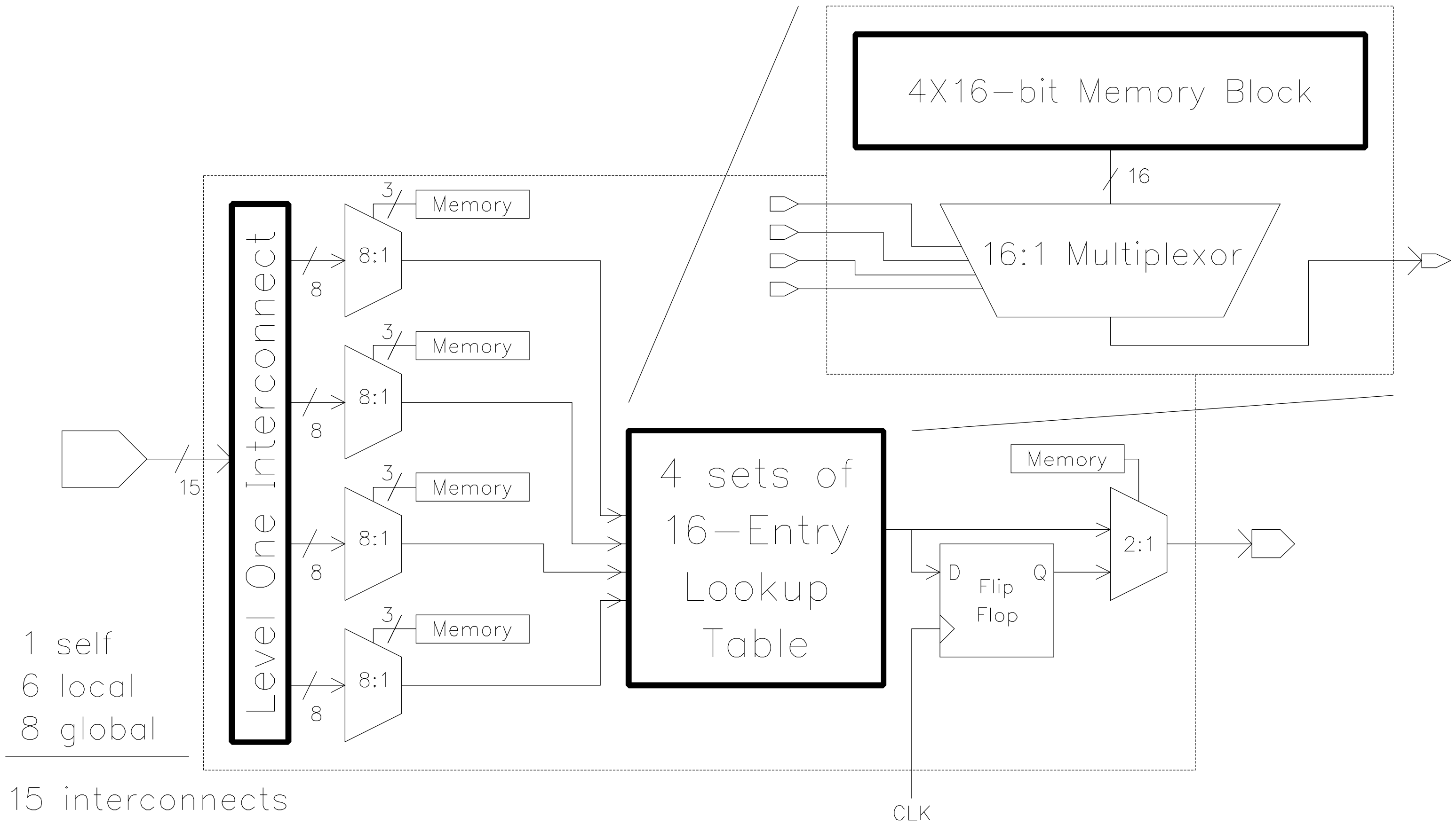
SubArray
4x4 composition of Array Element

Full DPGA
3x3 Composition of SubArrays
with Programmable CrossBar

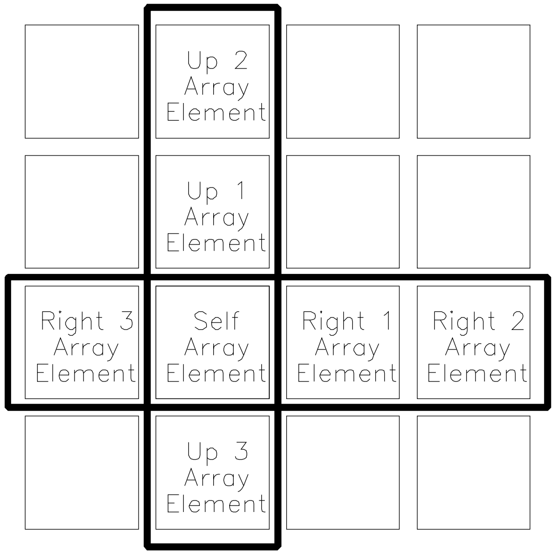
DPGA Prototype – Context Memory

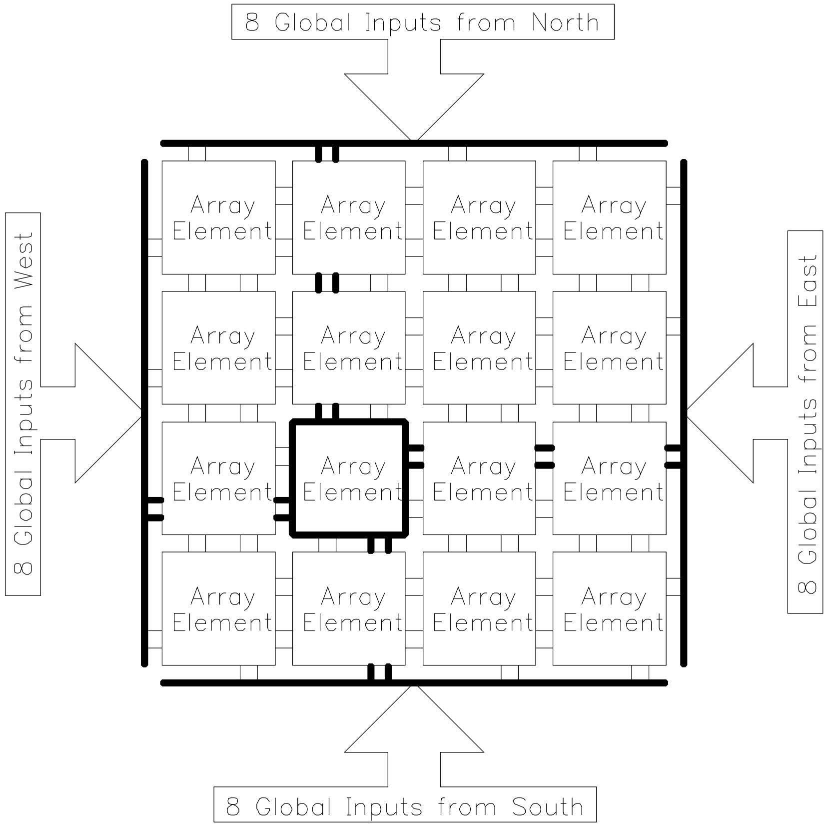


DPGA Prototype – Array Element



DPGA Prototype – Local Interconnect





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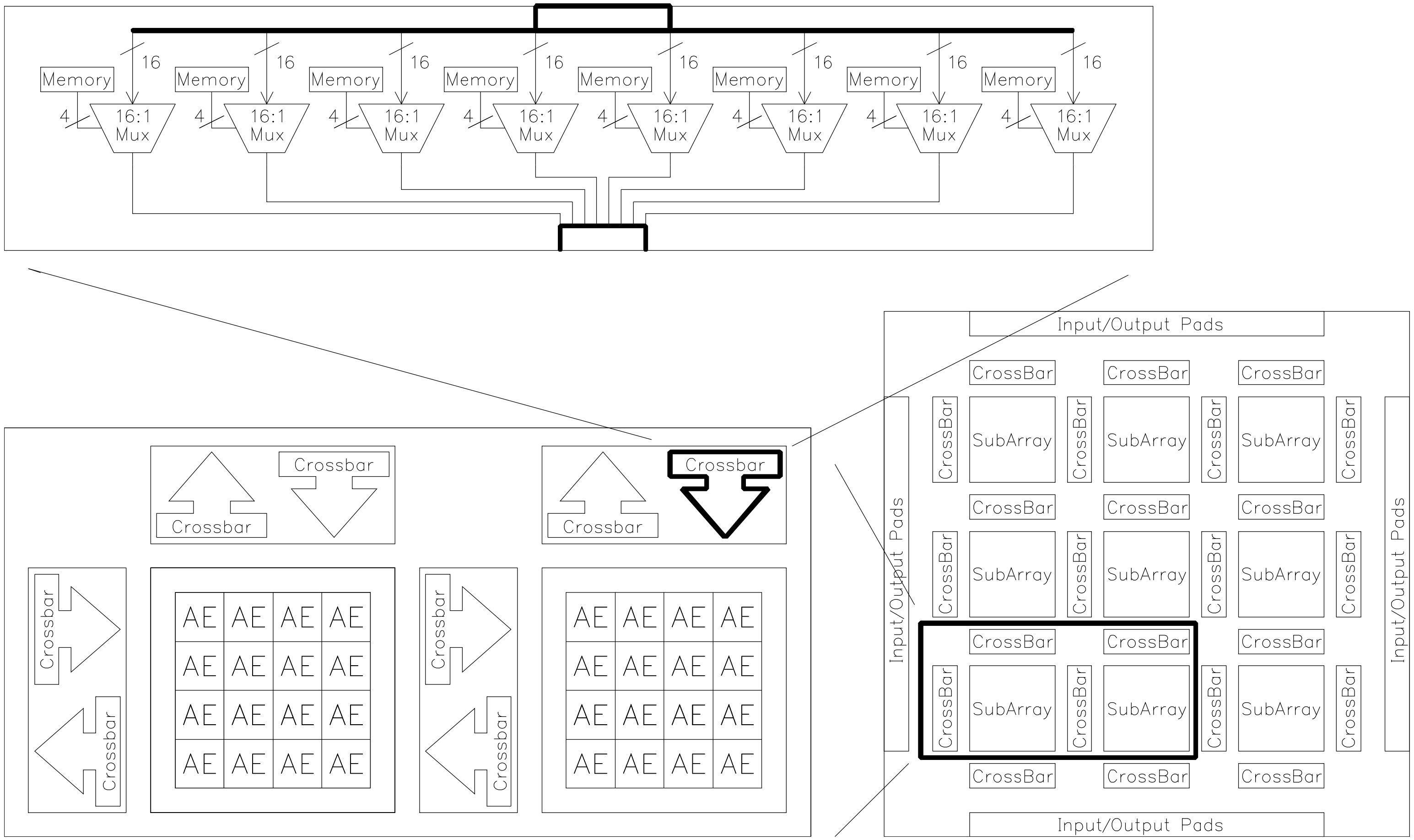
DPGA Prototype – Subarray Interconnect



DPGA Prototype – Areas

- 3 metal, 1μ drawn 0.85μ effective CMOS process

Unit	Size
Die	7.1mm$\times$6.8mm
Core	5.6mm$\times$4.7mm
Array Core	5.25mm$\times$4.4mm
Subarray+crossbar tile	1460$\mu\times$1750μ
Crossbar	495$\mu\times$270μ
Subarray	1150$\mu\times$1400μ
Local Decode	253$\mu\times$167μ
Array Element	275$\mu\times$240μ

DPGA Prototype – Area Percentages

Function	Elements	Percent
Logic	Total	16
	Memory array	10
	Memory decode	3
	Fixed Logic	3
Network	Total	66
	Memory array	15
	Memory decode	5
	Switching	19
	Wiring	27
Blank		18
Total		100

Memory Contribution

- Prototype (4 context, DRAM Memory)
  - Memory + Decode $\Rightarrow$ 33/82 = 40% Active Area
- Larger memory cells (*e.g.* SRAM)
  - Memory would dominate (70-80% for 4 contexts)
- Smaller memory cells (*e.g.* native DRAM)
  - Marginal cost of additional contexts decreases

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DPGA Prototype – Estimated Timings

Path	Delay symbol	slow-speed	nominal
CLK→configuration memory stable	t_{mem}	4 ns	2.5 ns
CLK→XBAR out	t_{xbar_1}	8.5 ns	5 ns
XBAR in→XBAR out	t_{xbar}	4.5 ns	2.5 ns
LUT in→LUT output	t_{lut}	9 ns	3.5 ns
CLK→CLK maximum (DRAM leakage)	$t_{clk_{max}}$		200 ns

$$t_{cycle} = t_{mem} + n_l \cdot t_{lut} + n_x \cdot t_{xbar}$$

Conclusions

- DPGA
  - Multiple Context FPGA
  - Rapid context switch
  - Increased effective logic density
  - Spatially and temporally varying computation
- Implementation Experience
  - 4-8 contexts viable (DRAM)
  - Single cycle context switch
  - Background load