

University of Pennsylvania
Digital Design Laboratory

Introduction to Xilinx ISE 8.2i

[Overview](#)
[Design Flow](#)
[Navigator Window](#)
[Device Types](#)
[Quick Tutorial](#)
[Pattern Wizard](#)
[Finite State Machine creation](#)
[References and resources](#)

Xilinx ISE Overview

The Xilinx ISE system is an integrated design environment that consists of a set of programs to create (capture), simulate and implement digital designs in a FPGA or CPLD target device. All the tools use a graphical user interface (GUI) that allows all programs to be executed from toolbars, menus or icons. On-line help is available from most windows (<http://toolbox.xilinx.com/docsan/xilinx8/books/manuals.pdf>).

This write-up is intended to get you started with the ISE tools. It gives a quick overview of how to create a design, simulate it and download it into a FPGA. For more detailed information please consult the on-line XILINX documentation and tutorials. The ISE User Guide is available on line.

Design Flow Overview

The following steps are involved in the realization of a digital system using Xilinx FPGAs, as illustrated by the following figure.

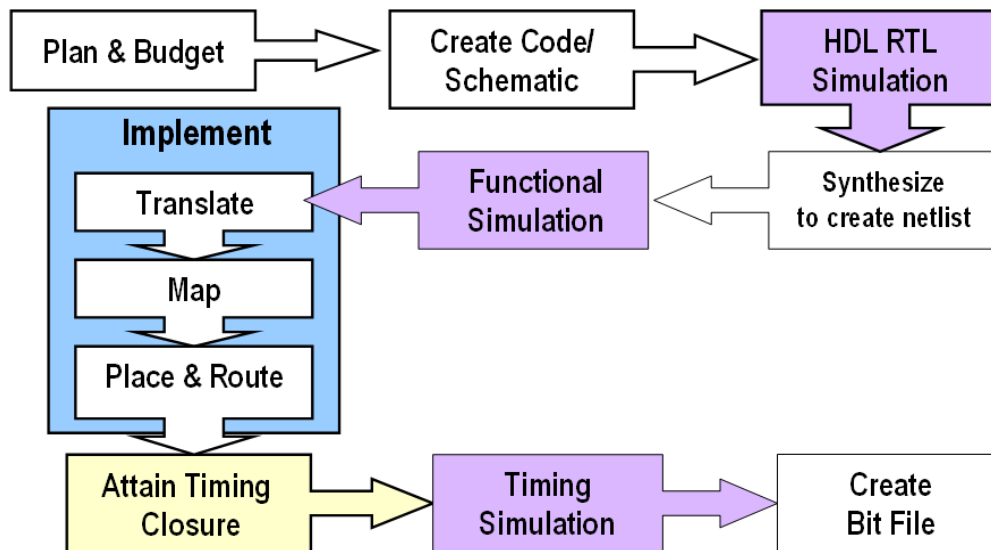


Figure: Overview of the various steps involved in the design flow of a digital system (Courtesy of J. Weintraub, Xilinx)

Design Entry

The first step is to enter your design. This can be done by creating “Source” files. Source files can be created in different formats such as a schematic, or a Hardware Description Language (HDL) such as VHDL, Verilog or ABEL. A project design will consist of a top-level source file and various lower-level source files. Any of these files can be either a schematic or a HDL file.

Design Synthesis

The synthesis step creates netlist files from the various source files. The netlist files can serve as input to the implementation module.

Design Verification (simulation)

This is an important step that should be done at various stages of the design. The simulator is used to verify the functionality of a design (functional simulation), the behavior and the timing (timing simulation) of your circuit. Timing simulation is run after implementing your circuit in the FPGA since it needs to know the actual placement and routing to find out the exact speed and timing of the circuit.

Design Implementation

After generating the netlist file (synthesis step), the implementation will convert the logic design into a physical file that can be downloaded on the target device (e.g. Virtex FPGA). This step involves three sub-steps: Translating the netlist, Mapping and Place&Route.

Device Configuration

This refers to the actual programming of the target FPGA by downloading the programming file to the Xilinx FPGA.

Project Navigator Window

The above steps are managed through a central ISE Project Navigator window, shown below.

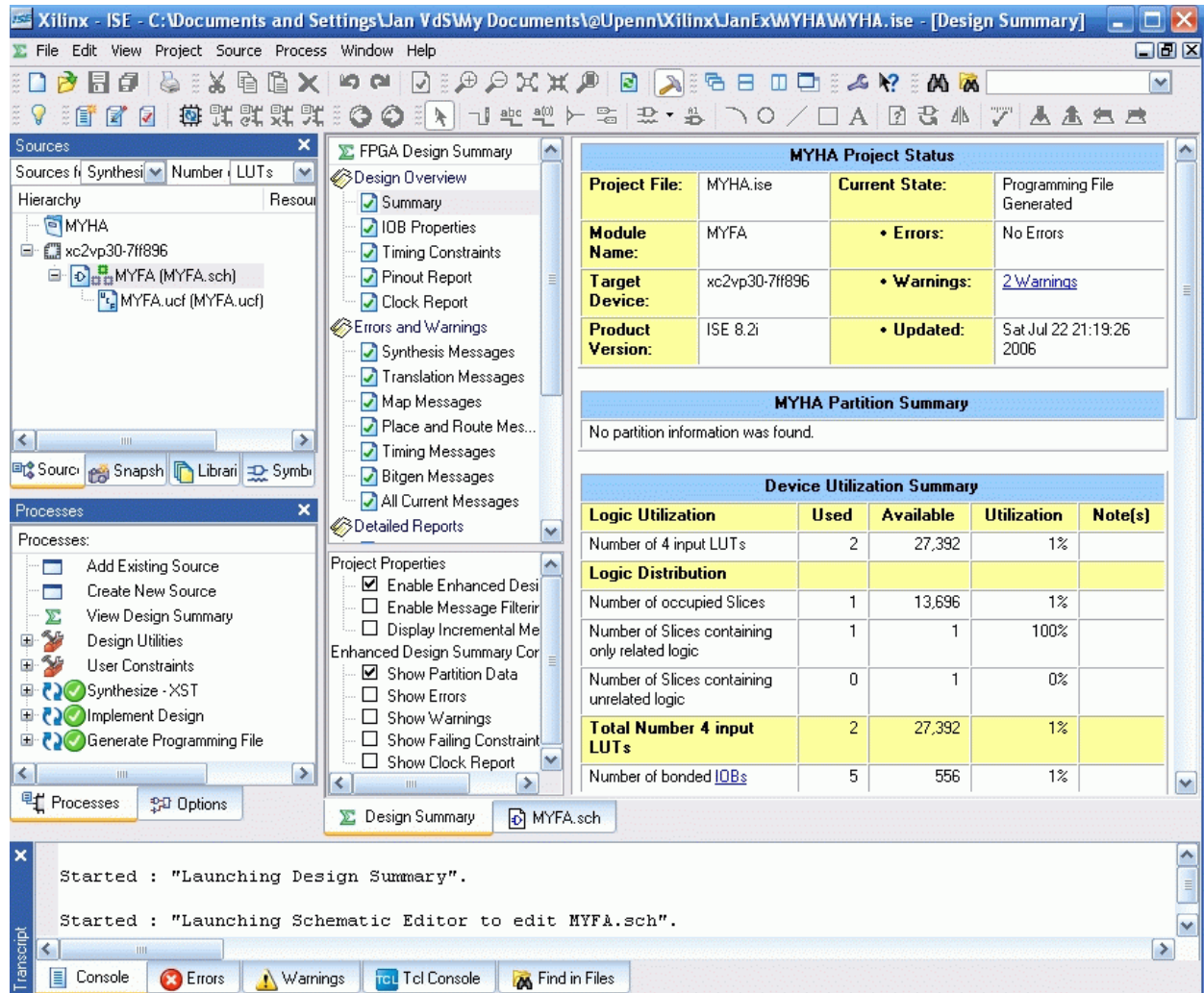


Figure: ISE Project Navigator Window (Screen clip from Xilinx (TM) ISE software)

Sources Window

This window contains the design source files for a project. These are the source files that you created or added to the project (see later on). A drop down list at the top of sources window allows you to select source files that are associated with a particular design aspect such as Synthesis/Implementation or Simulation.

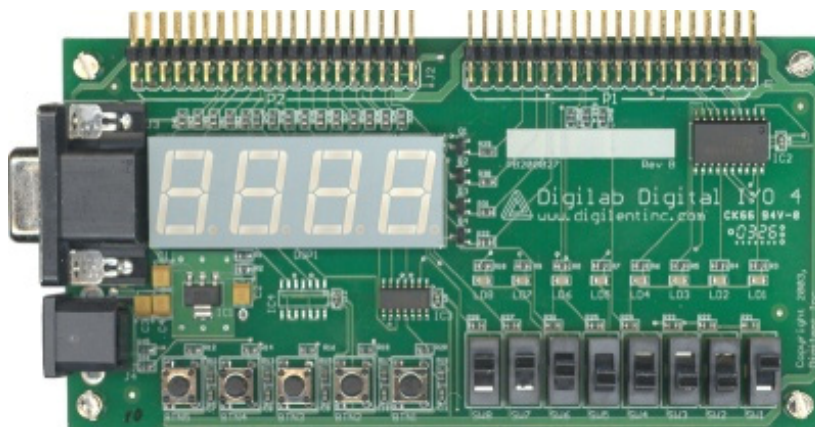
Processes Window

The processes windows list the available processes (corresponding to the process selected in the processes window). Typically you will select a particular process that you want to perform on the selected source file. This can include a simulation, implementation, etc. To run a process you can double click on the process. When a process has been successfully executed a red tick-off icon appears. When you run a high-level process, the Project Navigator will automatically run all the associated lower-level processes.

Device Types: FPGA and CPLD

There are two types of programmable logic devices. One is called a field programmable gate array (FPGA) and the other a complex logic device (CPLD). The CPLD XC9500 device has a PAL-like architecture and is non-volatile. It gives relatively good performance and is well suited for combinational logic circuits and control logic of medium complexity. The FPGA device (ex. Vertex series) has an array-like architecture and is volatile (SRAM based). It makes use of lookup tables (stored in the SRAM memory) to implement logic functions. It is good to realize complex logic functions that contain both combinational and sequential circuits. Its capacity is usually limited by the number of input/output pins and not by its complexity. FPGAs can currently implement up to 12 million (equivalent) logic gates and operate up to 550 MHz. The Virtex family of devices operates at 1.5 and 3.3 V I/O voltages. Besides the logic elements (look-up tables) it also contains RAM memory, DSP block, PowerPCs and several other complex digital cores. It can have up to over 800 I/O pins.

The development board you will be using ([Virtex-II Development Board](#)) has the XC2VP30 FPGA device. This chip has an array size of 80x46, contains 13969 slices, 428 Kb of distributed RAM, 2448 Kb of block RAM, two Power PC RISC Cores, 136 multiplier blocks and 8 Multi-Givebit transceivers. In addition to the main board, there is a [peripheral board](#) that contains individual LEDs, four debounced push-buttons, eight slide switches, a 3-bit VGA port and a PS/2 or keyboard port. The peripheral board is shown below. For more information consult the manual. A list of pinouts is given here.



Digilent DIO4 peripheral board with LEDs, seven-segment display, switches and push buttons.

Using the ISE software (quick tutorial)

[Schematic entry, simulation, implementation, downloading.](#)

References and resources

1. ISE Quick Start Tutorial: <http://toolbox.xilinx.com/docsan/xilinx8/books/docs/qst/qst.pdf>
2. ISE Software Manuals; <http://toolbox.xilinx.com/docsan/xilinx8/books/manuals.pdf>
3. ISE Project Navigator: <http://toolbox.xilinx.com/docsan/xilinx8/help/iseguide/iseguide.htm>
4. Design Flow Overview:
http://toolbox.xilinx.com/docsan/xilinx8/help/iseguide/html/ise_fpga_design_flow_overview.htm
5. ISE simulator:
<http://toolbox.xilinx.com/docsan/xilinx8/help/iseguide/mergedProjects/xsim/xsim.htm>
6. Xilinx Tutorials: <http://www.xilinx.com/support/techsup/tutorials/>
7. Software Manual: http://www.xilinx.com/support/software_manuals.htm
8. ISE Simulator:
<http://toolbox.xilinx.com/docsan/xilinx8/help/iseguide/mergedProjects/xsim/xsim.htm>
9. Xilinx Development Board for Virtex-II Pro (Digilent board):
<http://www.xilinx.com/univ/xupv2p.html>
10. Digilent DIO4 peripheral board manual:
<http://www.digilentinc.com/Products/Detail.cfm?Prod=DIO4&Nav1=Products&Nav2=Accessory>
11. Additional [Documentation and literature](#): <http://www.xilinx.com/support/library.htm>

Additional information:

There is also some useful information on the CSE372 website:

<http://www.cis.upenn.edu/~milom/cse372-Spring06/tutorial/>