

## BIPOLAR

Current  $i_C = I_S e^{\frac{v_{BE}}{V_T}} \approx 10^{-15} e^{40v_{BE}}$   
NPN forward-active mode

## CMOS

$$i_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (v_{GS} - V_{T0})^2 \approx 10^{-5} \frac{W}{L} (v_{GS} - 1)^2$$

n-MOS Saturation mode (si)

NOTE:

1. NPN bipolar transistor: a ten-fold increase in  $i_C$  is obtained with only a 60mV increase in  $v_{BE}$  due exponential relationship.
2. nMOS transistor: increasing  $v_{GS}$  to increase  $i_D$  has far less impact due to square law relationship.
3. Bipolar transistors are better for low-voltage design.

## Transconductance

$$g_m = \frac{I_C}{V_T} = \frac{I_C}{0.025} S = 40 I_C \quad g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} \approx 0.005 \sqrt{\frac{W}{L} I_D} S \approx 10 I_D$$

$$G = -g_m R_C$$

$$G = -g_m R_D$$

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_\pi + C_\mu}$$

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gd}}$$

## Noise & DC Offset

1. Bipolar transistors have lower offset voltages.
2. Bipolar transistors have lower 1/f noise.