University of Pennsylvania
Department of Electrical and Systems Engineering
ESE 319 Microelectronic Circuits

Midterm Exam #2
November 30, 2011

This exam is a closed book exam. Students are allowed to use a calculator (not a smart Phone or PDA with Internet Access) and a single page reference sheet (two sided). If you want opportunities for partial credit please show all work, justify all approximations and give the units for all parameters.

Consider the two-stage BJT differential-input, single-ended-output amplifier in Fig. 1 regarding the exercises that follow. Please use appropriate approximations throughout the exam.

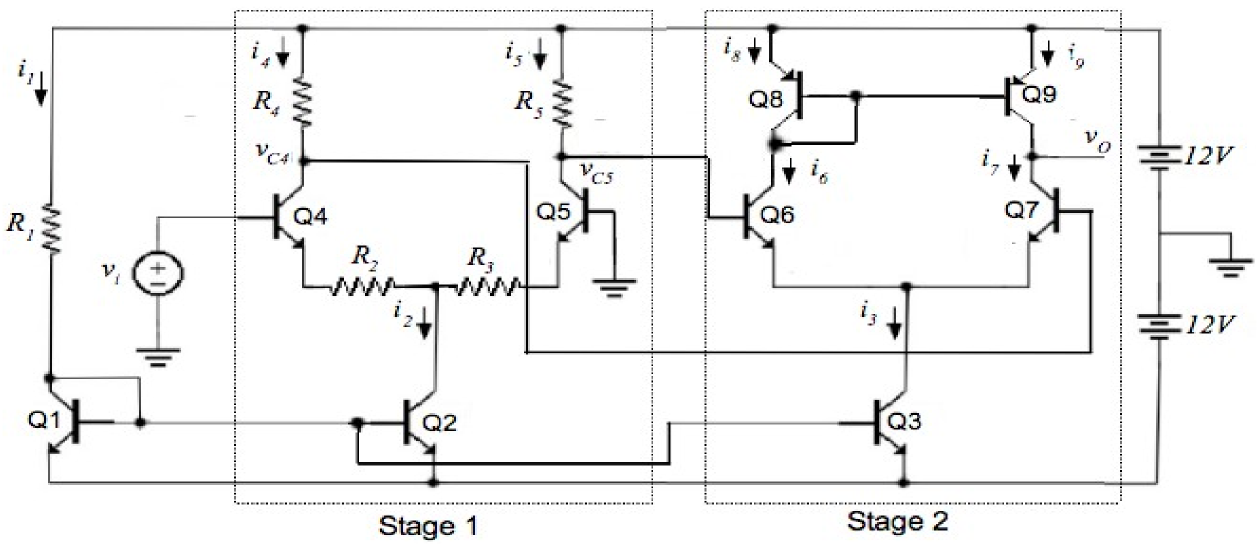

Fig. 1 Two-Stage BJT Differential Amplifier Schematic

In Fig. 1 voltage source v_i is the ac input signal, v_O be the large-signal output voltage (ac + dc), voltages v_{C4}, v_{C5} are large-signal collector voltages (ac + dc) for transistors Q4, Q5 and and each current i_1 through i_9 are large signal currents (ac + dc). The BJTs: for convenience in this exam let the parameters for all transistors (NPN and PNP) be $\beta = large$, $V_A = 100\,V$ and $V_{BEn} = V_{EBp} = 0.7\text{V}$.

1. For this two-stage amplifier to achieve its expected performance certain components are required to match, i.e. to be equal in value (also identical on-chip geometry and fabrication steps). Please state specifically the components in Fig. 1 that are <u>absolutely required</u> to be matched, and give specific reasons for your selections. It may be convenient to match more components than are absolutely required. Please only name the matches that are <u>absolutely required</u>. Refer to components by their numbered labels in Fig. 1. (10 pts)

2. Design the current mirror to set the dc component of i_1 to 1 mA. What are the values for the dc components of currents i_2 and i_3? (5 pts)

3. Determine the dc components for currents i_4 through i_9 and the small-signal parameters g_m, r_e, r_π and r_o for transistors Q2, Q4, Q6 and Q9 transistors. (5 pts)

4. Determine the symbolic expression for the stage 1 differential DM gain $A_{vd-stage1} = \dfrac{v_{c5} - v_{c4}}{v_i}$. Design stage 1 to realize $A_{vd-stage1} = 20$ and the dc component of v_{C4} to be V_{C4} = 7 V. What is the value for the dc component of v_{C5}? (30 pts)

5. Determine the symbolic expression for the stage 2 single-ended DM gain $A_{vd-stage2} = \frac{v_o}{v_{c5} - v_{c4}}$. Is there any design that can be done to set the value of $A_{v\text{-}stage2}$? If yes, design stage 2 to realize $A_{v\text{-}stage2} \geq 500$. If no, compute the value for $A_{v\text{-}stage2}$. (20 pts)

6. Gain $A_{vd\text{-}stage1}$ is weakly dependent on temperature T and gain $A_{vd\text{-}stage2}$ is strongly temperature dependent. Use your results in parts 4 and 5 of this exam to either support or refute this assertion. (10 pts)

6. Calculate the overall gain $A_{v-tot} = \frac{v_o}{v_i}$. Please note that signs are important. (20 pts)

EXTRA CREDIT: (12 pts)
The gain and phase of the loop-gain for a feedback amplifier has been plotted from experimental data in Fig. 2.

1. Define phase margin w.r.t. the data .plotted in Fig. 2. (3 pts)
2. Estimate the phase margin. (5 pts)
3. Is the feedback amplifier stable? Is it absolutely stable? (4 pts)

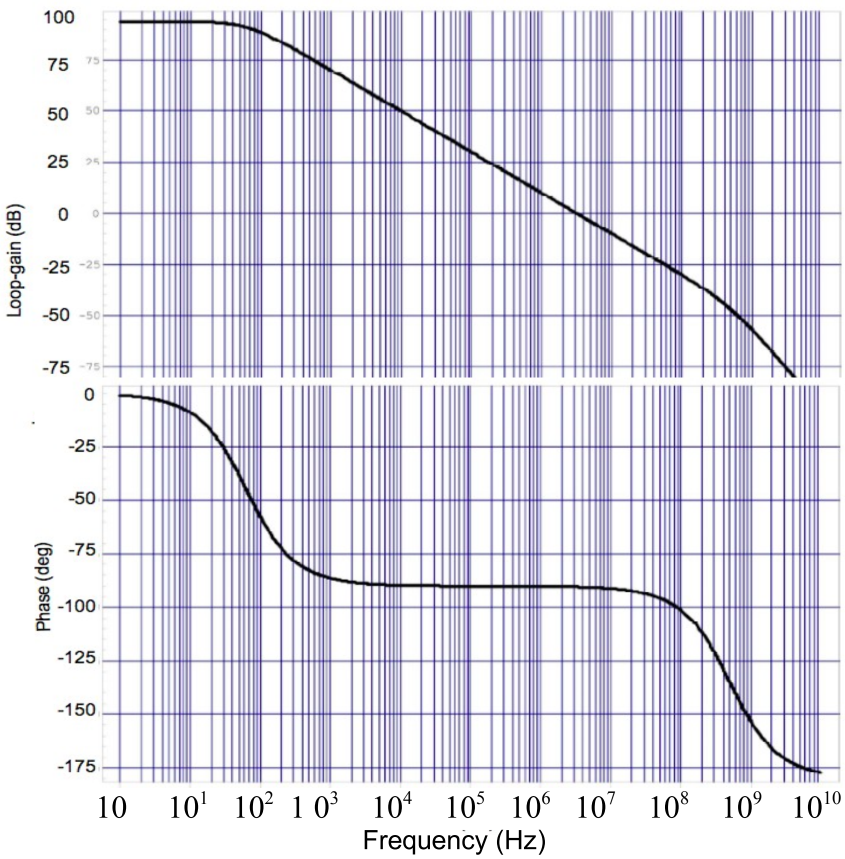

Fig. 2 Loop-gain gain and phase vs. frequency