University of Pennsylvania
Department of Electrical and Systems Engineering
ESE319

Laboratory Experiment - High Frequency Amplifier

Introduction.

This two-week lab involves the analysis, design, and experimental evaluation of a high frequency amplifier circuit of your choosing. The only specs are that the gain should be 10 ±10% and flat i.e., within 10%, two 3 dB cutoff points f_L and f_H specified $f_L \leq 100$ kHz and $f_H \geq 10$ MHz.

NOTE:
A gain of ten means that the output voltage of the amplifier should be ten times the *open circuit* voltage of the function generator. The input impedance of your amplifier may be low enough to load the function generator so that its terminal voltage when connected to the amplifier input will be lower than its open circuit voltage. Do not rely on the function generator reading for the input voltage to the amplifier, use the scope to read it. Design your amplifier to have sufficient gain to compensate for this loading.

First step – Design and simulate the amplifier in-lab during week 1.

Complete the design the amplifier in-lab and include it with the lab report. Your design results are to include a circuit diagram with component values, pencil and paper analysis to support your design, and the results of Multisim simulations to verify the design. Use only common transistor types and standard resistor values. Be thorough and careful in your analysis! When simulating, be sure to use the correct *Multisim* models for the transistors you select and the actual component values. Include important parasitic elements. Sketch out your Protoboard layout, so that you can include estimates of layout parasitic elements in your simulations. (See Hint f below.)

Second step – implement, test, and adjust the amplifier in lab – start in week 1 and complete in week 2.

Once your amplifier design has been verified by simulation to satisfy the specifications you are ready to implement your deign. If you have been thorough in your preliminary design and simulation efforts, your design probably will likely work on the first try. If you took unsubstantiated shortcuts, you may have to redesign and re-layout the circuit.

Hints.

A few suggestions to help with the design, simulation, and construction of your amplifier are in order.

a. The inductance in the leads that you use to connect the amplifier to the power supply is not negligible at high frequencies. This inductance exists between the supply voltage source and ground – a path that we want to be a short circuit at ac. The effect of this power supply lead inductance will show up as a gain "peaking" at the upper end of your amplifier frequency response. Therefore, the inductance of both leads must be included in the incremental equivalent circuit for your amplifier. A reasonably accurate formula for estimating this lead inductance is:

$$L(\mu H) = .002\, l \left[2.5 \log_{10}\left(4\frac{l}{d} - 0.75 \right) \right]$$

Where:

l = length of wire in cm.
d = diameter of wire in cm.
2.54 cm = 1 inch.

Example:

Two power supply leads equal about 2 meters of #18 wire (diameter 40.3 mils, or 40.3 thousandths of an inch) = 3.89 µH.

Reactance at 10 MHz :

$$X_L = 2\pi f L = 2 \bullet 3.14 \bullet 10^7 \bullet 3.89 \bullet 10^{-6} \approx 244\Omega$$

To "short out" this inductance use a single power supply and place a bypass capacitor between V_{CC} and ground on the Protoboard power bus. Don't choose too large a value for this bypass capacitor. Large capacitors self-resonate with their own lead inductance at relatively low frequencies and act as inductors with increasing impedance above resonance! You may have to experiment with the capacitor to find a value that completely eliminates gain "peaking" at the higher amplifier frequencies.

b. Since we want to minimize the "shunting" effect of parasitic transistor and circuit capacitances, large values of g_m and I_C are desirable and smaller resistor values should be used. Thus the circuit should be biased for relatively high collector currents using low values of external emitter and collector resistors.

c. Keep leads short with components close together, while simultaneously isolating input leads from output ones.

d. Use 10x scope probes for all high frequency measurements. **The scope impedance, even with 10x probes, will load the output of your amplifier and reduce its gain at high frequencies**. Split the output load resistor into two series resistors and use the scope to measure the voltage to ground across the resistor connected to the power supply lead. Choose this resistor so that its resistance is lower than the probe (capacitive) reactance at 10 MHz by at least a factor of 10. **Remember to correct your gain calculations to account for this voltage division. You are measuring only a fraction of the actual output voltage!**

e. Use the voltage source and ground buses on your Protoboard.

f. There is about 0.5 pF capacitance between two adjacent socket holes on the Protoboard. If there are five holes in parallel, this amounts to about 2.5 pF. Take this capacitance into consideration both when you lay out and when you simulate your circuit.

g. Don't waste time trying to satisfy the given specifications with a single stage common emitter amplifier! The Miller effect present in the common emitter amplifier with gain will make it extremely difficult to meet the $f_H \geq 10$ MHz spec.

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