

University of Pennsylvania
Department of Electrical and Systems Engineering
ESE 319
Mini-project – Op Amp and Active Filter

1. Introduction.

This mini-project will use knowledge that you have gained in this course to design, simulate, implement and test a basic op amp circuit and use it in a 2nd order active filter circuit. The CA3046 and THAT340P transistor array chips are available for your use in this project. This project is a three-week project. Datasheets for the CA3046 and THAT340P are posted on the ESE319 website.

2. Basic op-amp design.

The most basic op amp is a differential input, single-ended output op amp comprised of a differential stage and an output stage as shown in Fig. 1. The op-amp is to approximate a voltage-controlled voltage source.

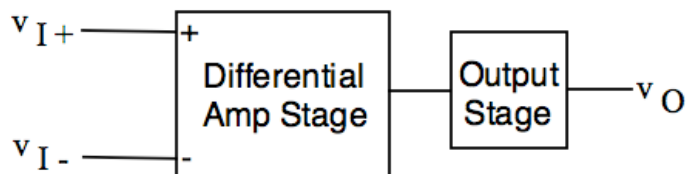


Fig. 1 Basic Op Amp

Your group assignment is to design a basic op amp of the kind illustrated in Fig.1 that realizes the following specifications, using supply voltages of ± 10 V:

Open-Loop:

- a. I bias of less than or equal to 5 mA
- b. Single-ended differential gain greater than 40 dB (differential input to single-ended output).
- c. Single-ended differential unity-gain-bandwidth of greater than 10 MHz.
- d. CMRR greater than 40 dB up to 10 MHz.
- e. Simulated phase margin of greater than 20° .
- f. No load power drain that is less than 0.1 Watt.

Closed-loop, unity-gain amplifier:

- a. Apply feedback to realize a non-inverting closed-loop gain of unity or 0 dB.
- b. Closed-loop amplifier must drive a load of 10 k Ω and 15 pF load at a frequency of 10 MHz with less than 1 % degradation in signal level.
- c. No load power drain that is less than 0.1 Watt.

3. Active Filter.

Use the unity gain closed-loop specified in part 2 to implement a 2nd order maximally-flat-magnitude (MFM) pass-band or Butterworth low-pass filter using the Sallen-Key active filter circuit shown in Fig. 2.

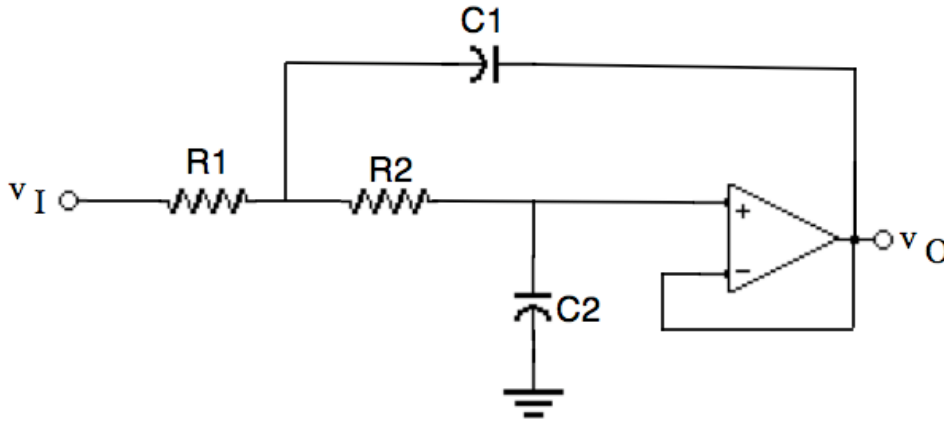


Fig. 2 Sallen-Key 2nd order filter circuit

The voltage transfer function for the MFM or Butterworth Sallen-Key filter circuit in Fig. 2 is as follows:

$$G(s) = \frac{1/R_1 R_2 C_1 C_2}{s^2 + s(1/R_2 C_1 + 1/R_1 C_1) + 1/R_1 R_2 C_1 C_2} = \frac{\omega_0^2}{s^2 + s\sqrt{2}\omega_0 + \omega_0^2}$$

With $R_1 = R_2 = R$ and $C_2 = 100 \text{ pF}$, choose RCA lab resistor and capacitor values for R and C_1 to achieve $f_0 = 180 \text{ kHz} \pm 10\%$ and $20 \log_{10} |G(j2\pi f)| = 0 \text{ dB} \pm 0.1 \text{ dB}$ for $f \leq 50 \text{ kHz}$.

4. Simulation.

A. Open-loop – once you have your basic op amp circuit, simulate your circuit to evaluate the following:

- All important DC currents and voltages for each stage of your op amp design.
- Single-ended differential-mode gain vs. frequency from 0 to 1 GHz.
- Single-ended differential-mode phase vs. frequency from 0 to 1 GHz and determine the phase margin.
- Single-ended common-mode gain vs. frequency from 0 to 1 GHz.
- Verify that the open-loop op amp specifications in section 2 have been met with some margin.
- Conduct any other simulations you deem necessary to evaluate your design.

B. Closed-loop – close the loop to achieve unity or 0 dB non-inverting gain. Simulate your closed-loop circuit to evaluate.

- Gain vs. frequency for your open-loop op amp from 0 to 1 GHz.
- Apply a square wave input with amplitude 1 or 2 V and frequency of say 1 kHz and evaluate the characteristics of the amplifier response.
- Verify that the closed-loop specifications in section 2 have been met with some margin.
- Conduct any other simulations you deem necessary to evaluate your design.

C. Filter – determining the component values for the filter specifications in section 3, simulate your filter circuit to evaluate the following:

- Gain vs. frequency for your open-loop op amp from 0 to 100 MHz.
- Verify that the filter specifications in section 3 have been met with some margin.

- c. Conduct any other simulations you deem necessary to evaluate your design.

5. Proto-board implementation and experimental measurement.

A. Open-loop op amp.

- a. Build the op-amp on your Proto-board and evaluate the open-loop performance of your op-amp.
- b. Due to their large gain, open-loop op amps are notoriously tricky to test. You may need to add components to your proto-board to assist the measurement equipment to conduct meaningful measurements.
- c. Verify that open-loop op amp specs in section 2 have been met.

B. Closed-loop amplifier.

- a. Close the loop on your proto-board op amp to realize unity or 0 dB non-inverting gain.
- b. Measure gain vs. frequency from 0 to 15 MHz.
- c. Verify that the closed-loop amplifier specifications in section 2 have been met.

C. Filter.

- a. Connect on your proto-board the filter components needed to your closed-loop amplifier to realize the Sallen-Key Butterworth 2nd order low-pass filter circuit.
- b. Measure gain vs. frequency from 0 to 15 MHz.
- c. Verify that the filter specifications in section 3 have been met.

6. Suggested project schedule.

To help you pace your progress, you should plan to complete your basic op amp design and Multisim simulations by the end of week 1, complete the proto-board implementation, debug and test your open-loop and unity-gain closed-loop op-amp by the end of week 2 and complete the design, proto-board implementation and test of your filter by the end of week 3.

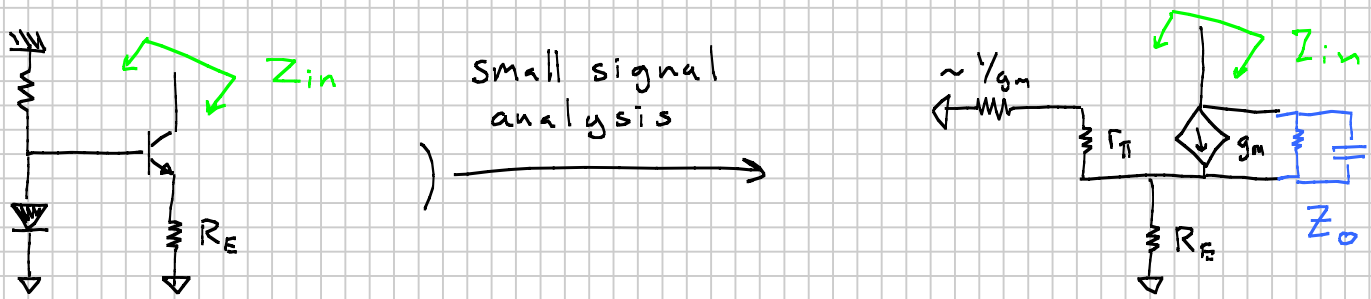
7. Report requirements. The basic project is completed when:

- a. Document your work with schematics, simulation and experimental results.
- b. Were you able to experimentally verify all of the specifications for the open-loop op amp, the closed-loop amplifier and the filter. If not, what specifications were you not able to verify and why were you not able to verify them.
- c. Were all of the specifications for the open-loop op amp, closed-loop amplifier and filter met? If not, discuss the specifications that were not met.
- d. The basic op amp that you were asked to design can be improved upon. Discuss at least one improvement that can be made to improve the performance of the op amp, e.g. gain, stability, operating range, etc. Identify specific circuit improvements that you would make to effect the improvement(s) that you identify. Verify your identified circuit improvement(s) using Multisim.

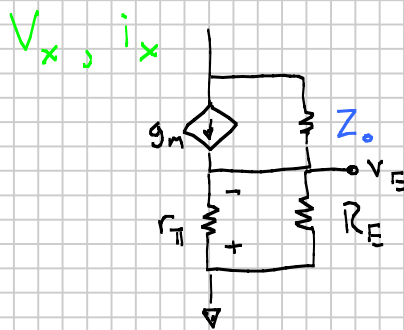
Active load with emitter degeneration

Note Title

11/10/2008



$$r_{\pi} \gg 1/g_m$$



$$i_x = i_{g_m} + i_{z_o}$$

$$= -g_m V_E + (V_x - V_E) / Z_o$$

$$V_E = i_x (R_E \parallel r_{\pi})$$

$$i_x = -g_m (R_E \parallel r_{\pi}) i_x + V_x / Z_o - i_x \frac{(R_E \parallel r_{\pi})}{Z_o}$$

$$Z_x = \frac{V_x}{i_x} = (R_E \parallel r_{\pi}) (1 + g_m Z_o) \approx (R_E \parallel r_{\pi}) g_m Z_o$$

Adding emitter degeneration to an active current source increases its output Z_o impedance by a factor of $(R_E \parallel r_{\pi}) g_m$.