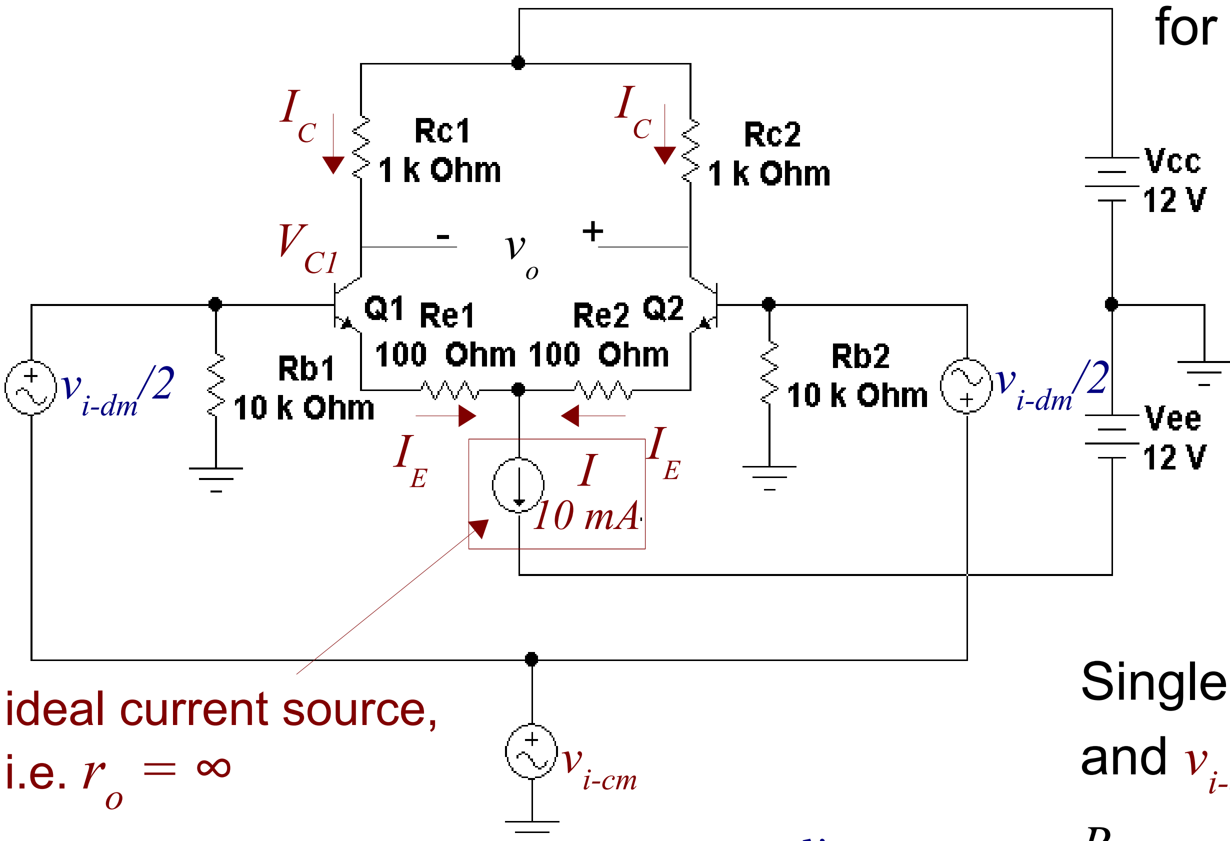
Differential Amplifier Design

- Design with ideal current source bias.
- Differential and common mode gain results
- Add finite output resistance to current source.
- Replace ideal current source with current mirror.

Quick Amplifier Design



By inspection DC bias ($v_{i\text{-}dm} = v_{i\text{-}cm} = 0$) for Q1 & Q2 is common mode:

$$I_E = \frac{I}{2} = 5\,mA$$

Neglecting I_B:

$$I_C = I_E = 5\,mA$$

$$V_{R_c} = 5\,V \Rightarrow V_{C1} = V_{CC} - V_{R_c} = 7\,V$$

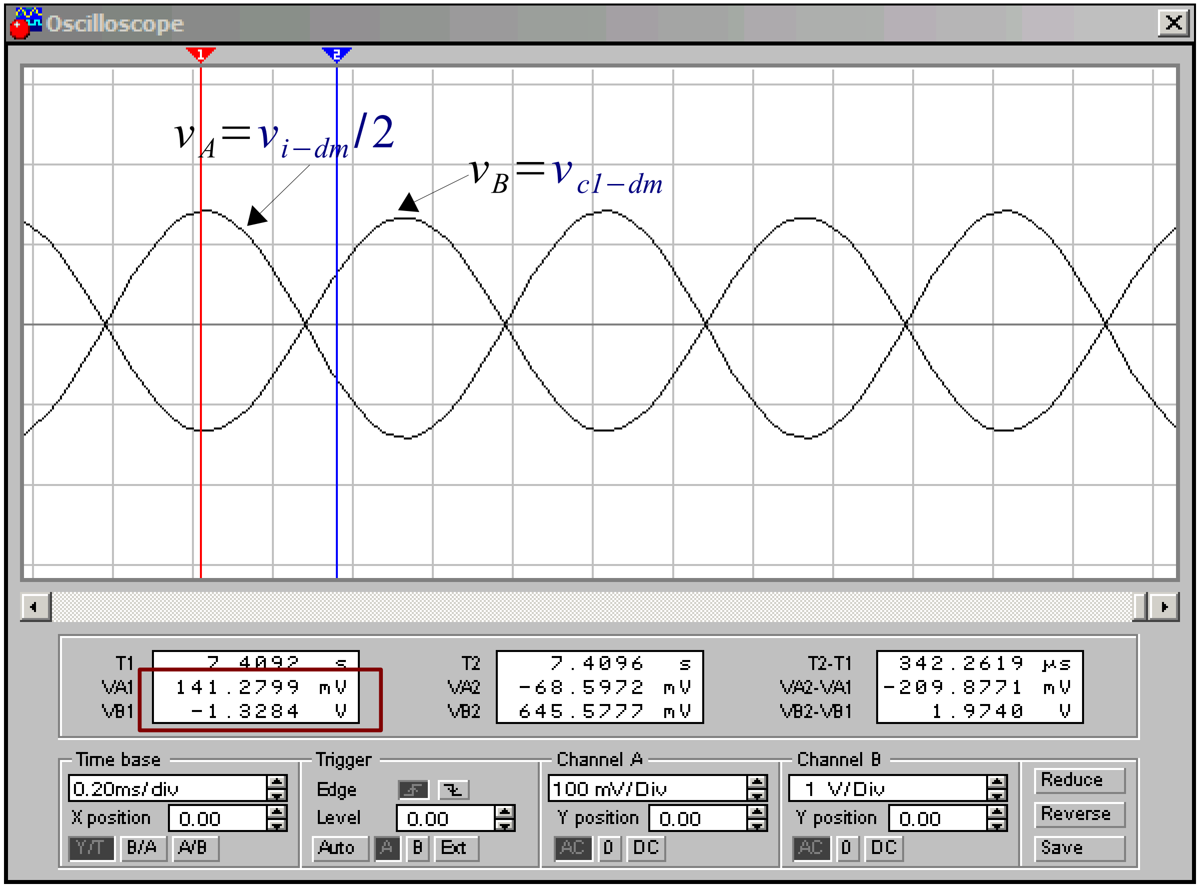
$$V_E = -V_{BE} = -0.7\,V$$

$$V_{CE} = V_C - V_E = 7.7\,V$$

Single-ended voltage gains w.r.t. $v_{i\text{-}dm}/2$ and $v_{i\text{-}cm}$ (for Q1 side):

$$A'_{v-dm1} = \frac{v_{c1-dm}}{v_i = v_{i-dm}/2} \approx \frac{-R_C}{R_E} = -10 \qquad A_{v-cm1} = \frac{v_{c1-cm}}{v_{cm}} \approx -\frac{R_C}{2\,r_o} = 0$$

Differential- Mode AC Gain Results



"Scope" output B at collector of Q1, i.e. $v_B = v_{c1-dm}$.

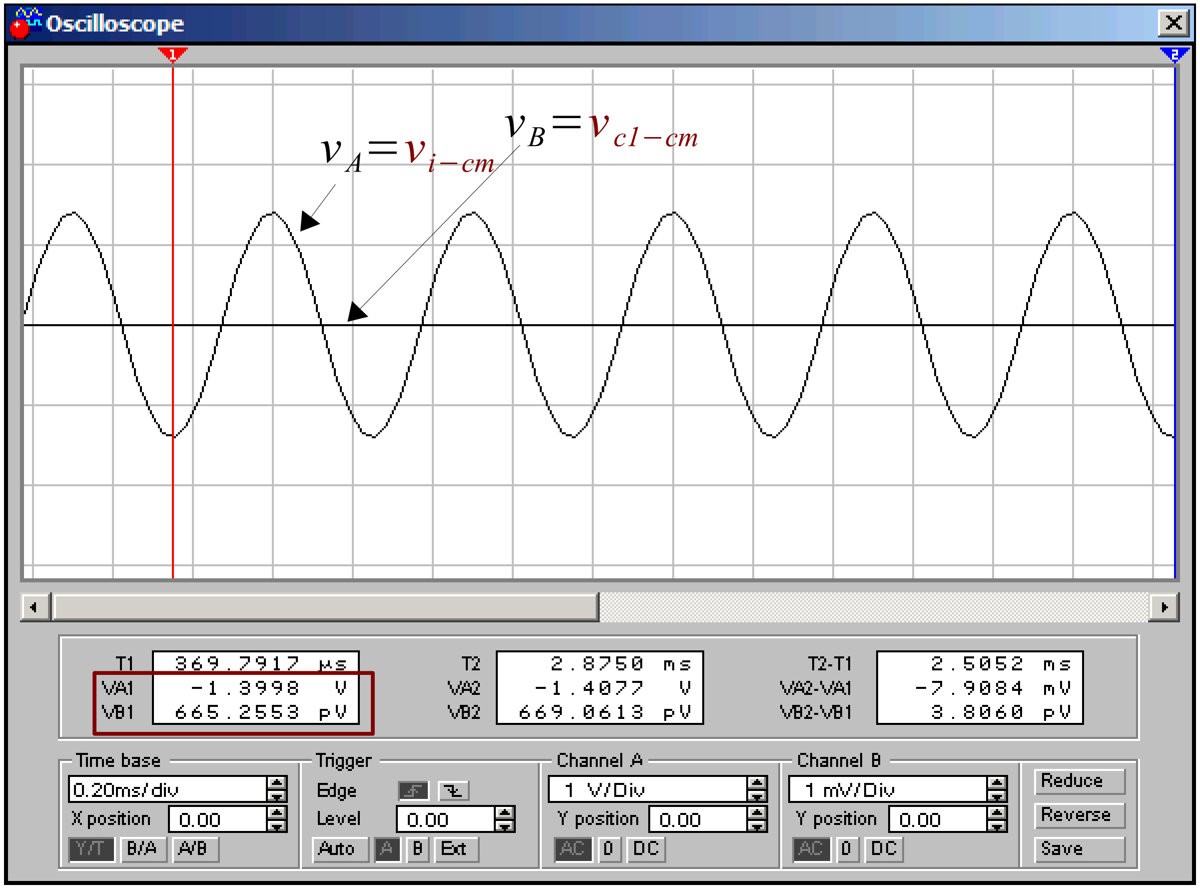
Input voltage $v_A = v_i = v_{i-dm}/2$
$0.14\ V_{peak}\ arg\ (0^o)$ at $f = 1\ kHz$.

Output voltage $v_B = v_{c1-dm}$
$1.33\ V_{peak}\ arg\ (180^o)$.

Measured gain:

$$A'_{v-dm1} = \frac{v_B}{v_A} = \frac{v_{c1-dm}}{v_i} = \frac{-1.33\ V}{0.14\ V} = -9.5$$

Common Mode AC Results



"Scope" output B at collector of Q1, i.e. $v_B = v_{c1-cm} = 0\,V$.

Input voltage $v_A = v_{i-cm}$ $0.14\ V_{peak}\ arg\ (0^o)$ at $f = 1\ kHz$.

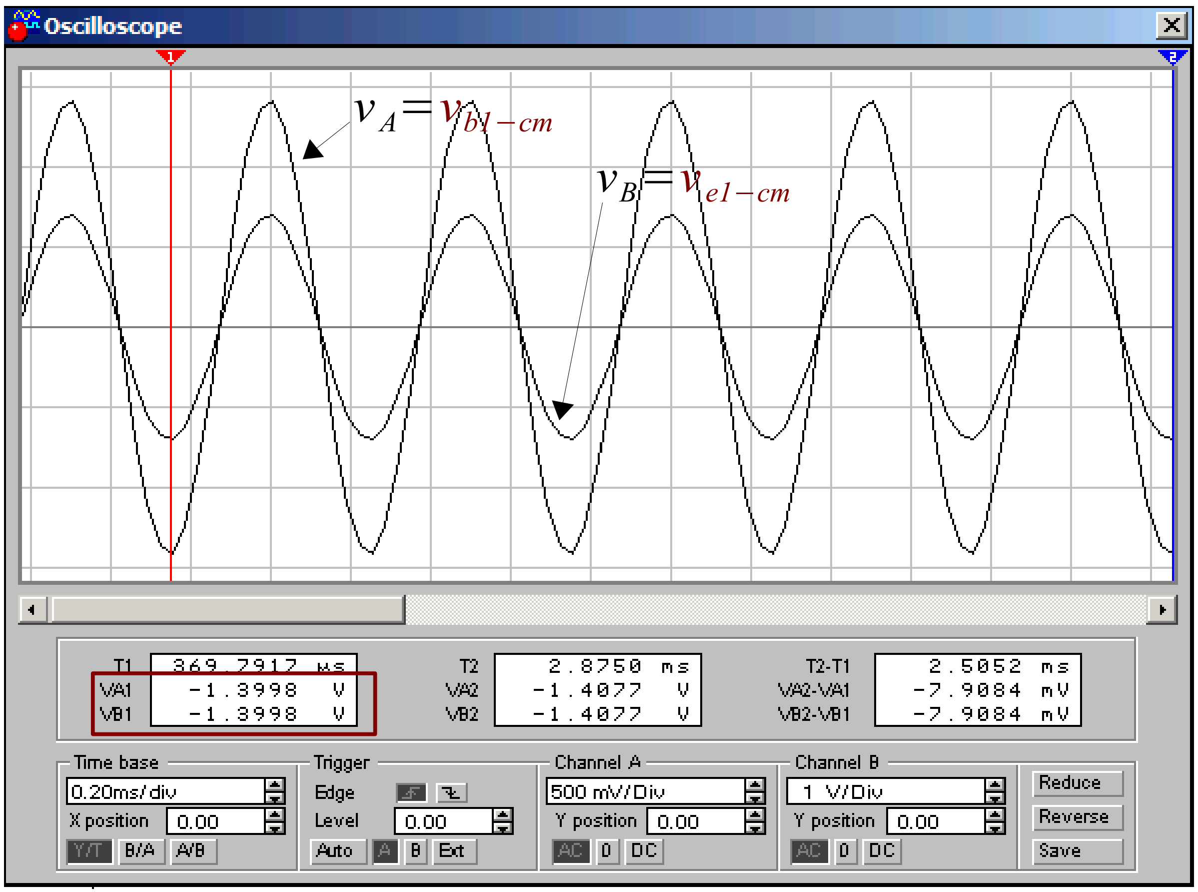
Since I is an ideal current source $r_o = \infty$ => $A_{v-cm1} = 0$.

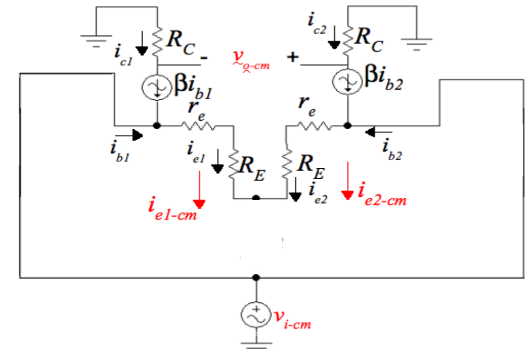
No common mode signal current ($i_{cm} = 0$ => $i_{e-cm} = 0$)

$$\Rightarrow v_{c1-cm} = 0\,V_{peak}$$

$$CMRR \approx 20\log_{10}\left|\frac{-9.5}{0}\right| = \infty$$

Common Mode AC Results - II





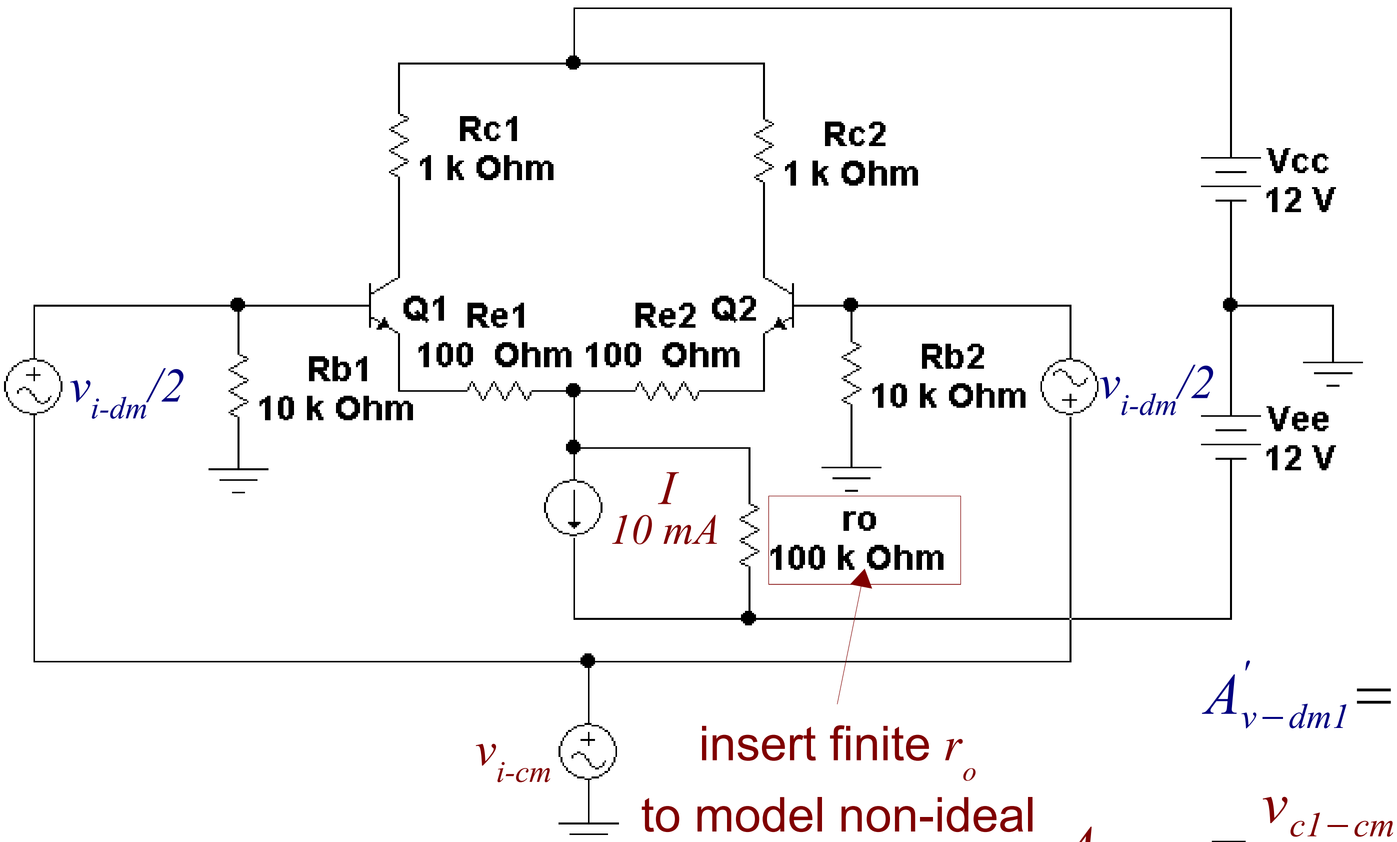
Comparing ac base and emitter voltages to ground for Q1, i.e. v_{b1-cm} , v_{e1-cm} .

$$v_{b1-cm} = v_{e1-cm} = 1.4\, V_{peak}$$

$$\Rightarrow v_{be-cm} = 0\, V_{peak}$$

Since $i_{e\text{-}cm} = 0$, we expect $v_{be-cm} = 0\, V_{peak}$, i.e. all base voltage appears at emitter.

Common Mode Results - Add r_o to Model

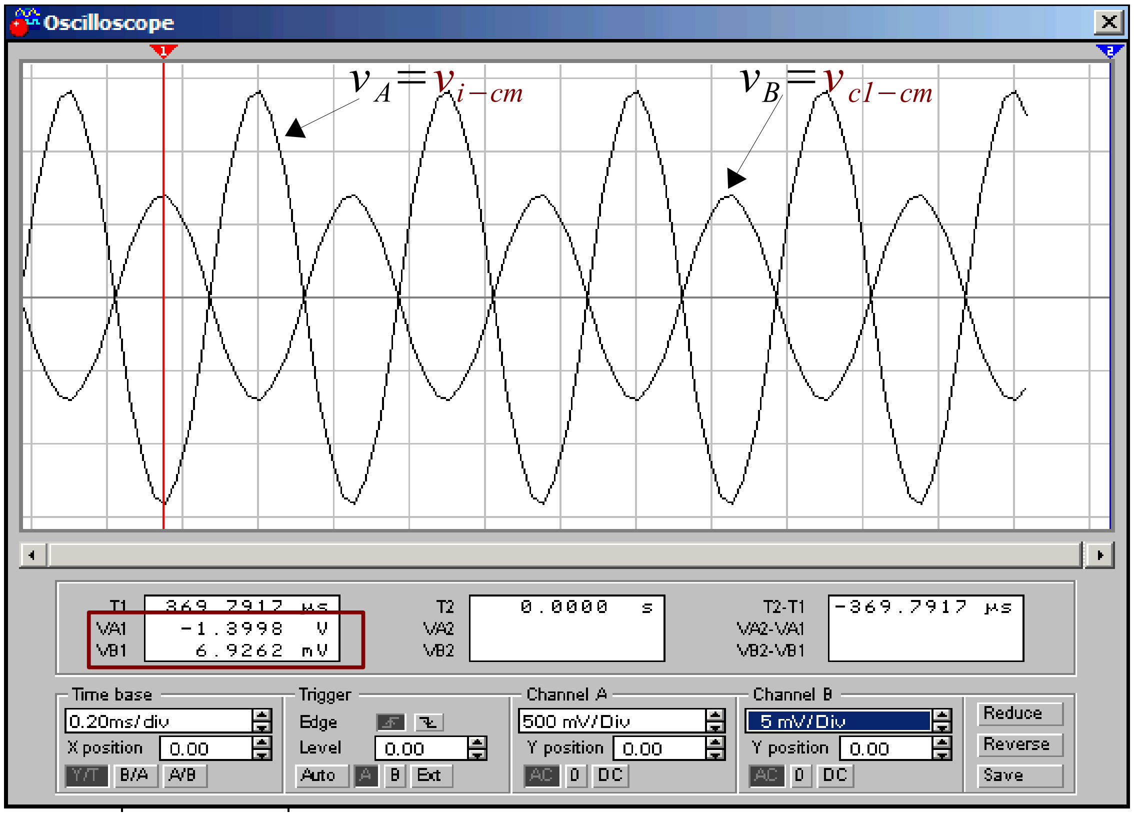


insert finite r_o
to model non-ideal
current source

$$A'_{v-dm1}=\frac{v_{c1-dm}}{v_i}\approx\frac{-R_C}{R_E}=-10$$

$$A_{v-cm1}=\frac{v_{c1-cm}}{v_{i-cm}}\approx-\frac{R_C}{2r_o}=\frac{-1}{200}=-0.005$$

Common Mode Results - Add Finite r_o



$r_o = 100\,k\,\Omega$

"Scope" output B at collector of Q1, i.e. $v_B = v_{c1-cm}$.

Input voltage $v_A = v_{i-cm}$
$1.4\ V_{peak}\ arg\ (0^o)$ at $f = 1\ kHz$.

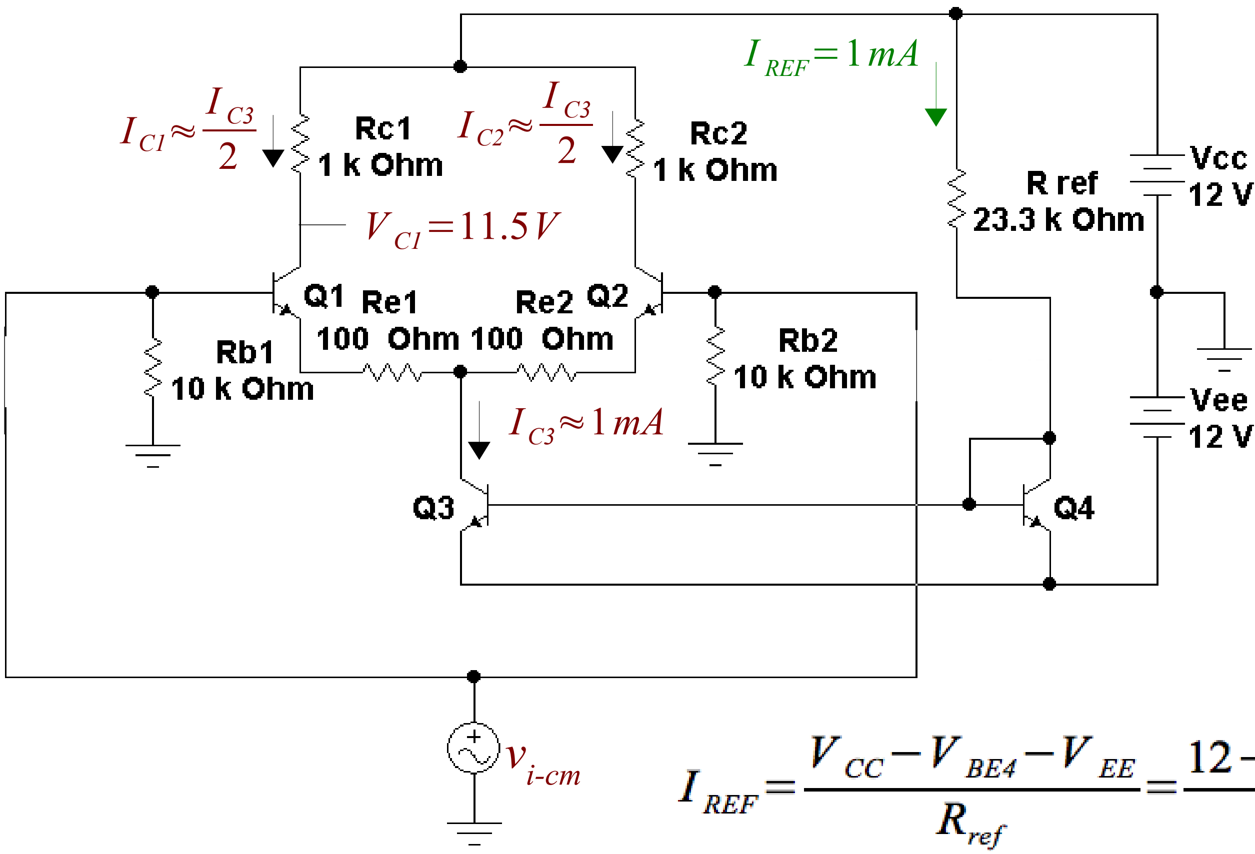
Output voltage $v_B = v_{c1-cm}$
$0.007\ V_{peak}\ arg\ (180^o)$.

$$A_{v-cm1} \approx \frac{-0.007}{1.4} = -0.005$$

$A'_{v-dm1} = -9.5$ (unchanged)

$$CMRR \approx 20 \log_{10}\left(\frac{9.5}{0.005}\right) \approx 66\,dB$$

Simulation with Current Mirror



Matched 2N2222 BJTs (Q1, Q2, Q3 and Q4).

$I_{C3}\approx 1\,mA$

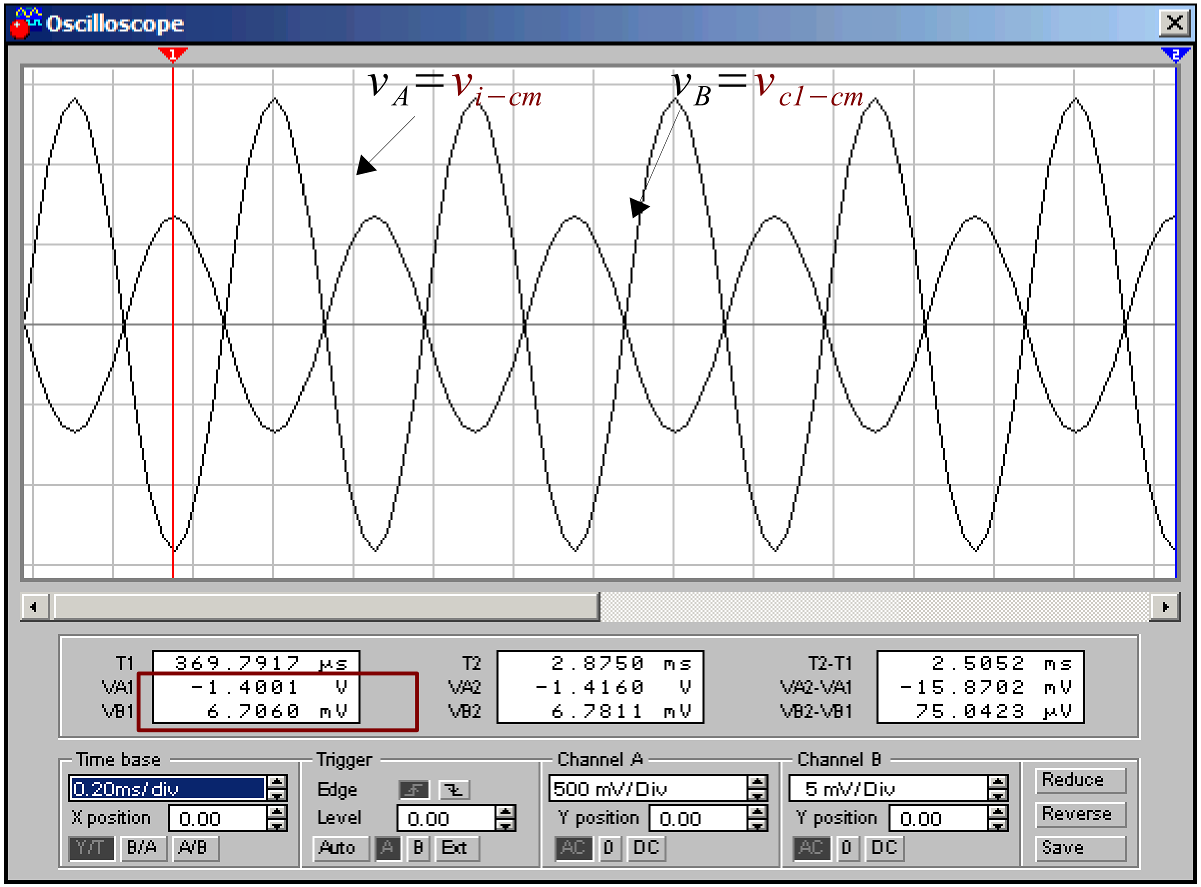
$\Rightarrow I_{C1}=I_{C2}\approx 0.5\,mA$

$R_{ref}=23.3\,k\,\Omega$

$$I_{REF}=\frac{V_{CC}-V_{BE4}-V_{EE}}{R_{ref}}=\frac{12-0.7-(-12\mathrm{V})}{23.3}mA\approx 1\,mA$$

NOTE: - The zero-to-peak ac voltage swing across each R_C now only $0.5\ V$!

Simulation with Current Mirror - II



"Scope" output B at collector of Q1, i.e. $v_B = v_{c1-cm}$.

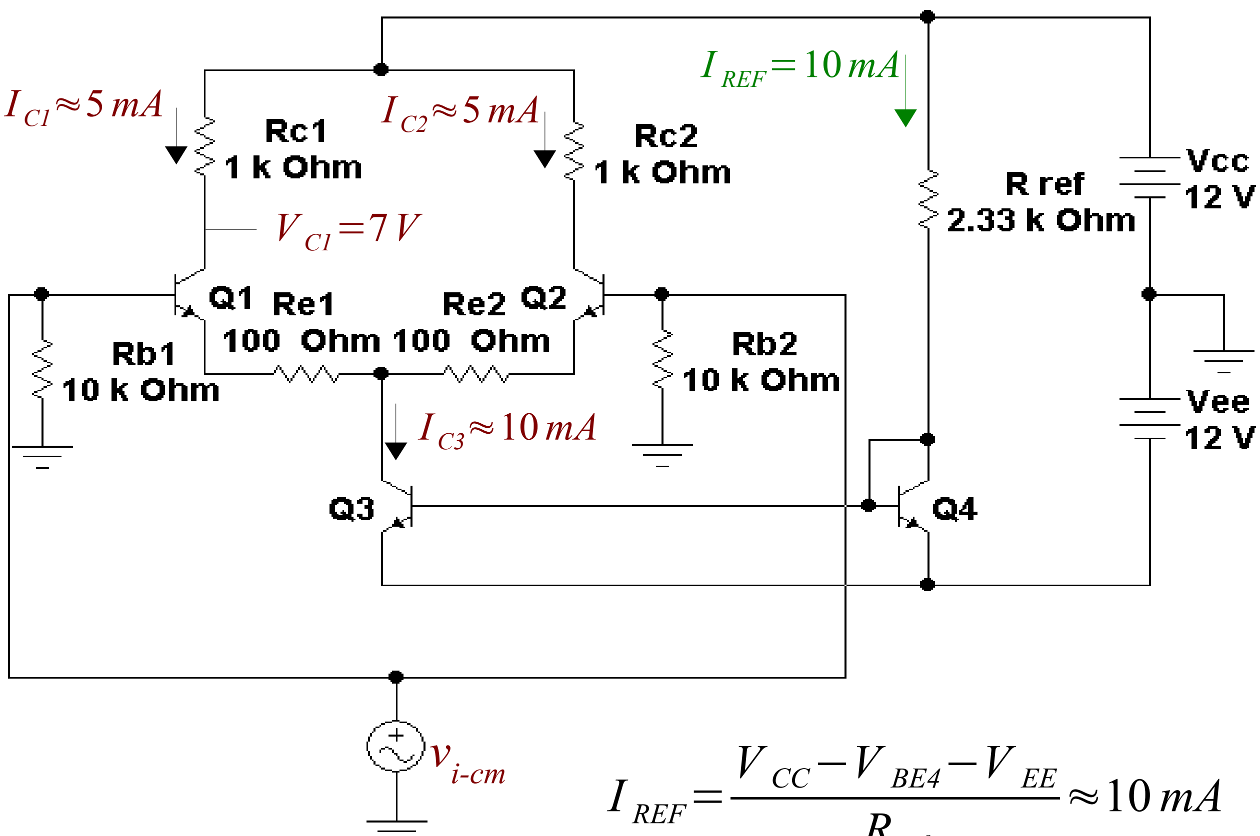
Input voltage $v_A = v_{i-cm}$ $1.4\ V_{peak}\ arg\ (0^o)$ at $f = 1\ kHz$.

Output voltage $v_B = v_{c1-cm}$ $7\ mV_{peak}\ arg(180^o)$.

$$A_{v-cm1} \approx \frac{-0.007}{1.4} = -0.005$$

$1\ kHz$ common mode results almost exactly same as those for $r_o = 100\,k\,\Omega$ model.

Simulation with Current Mirror - III



Matched 2N2222 BJTs (Q1, Q2, Q3 and Q4).

$$I_{C3} \approx 10\,mA$$

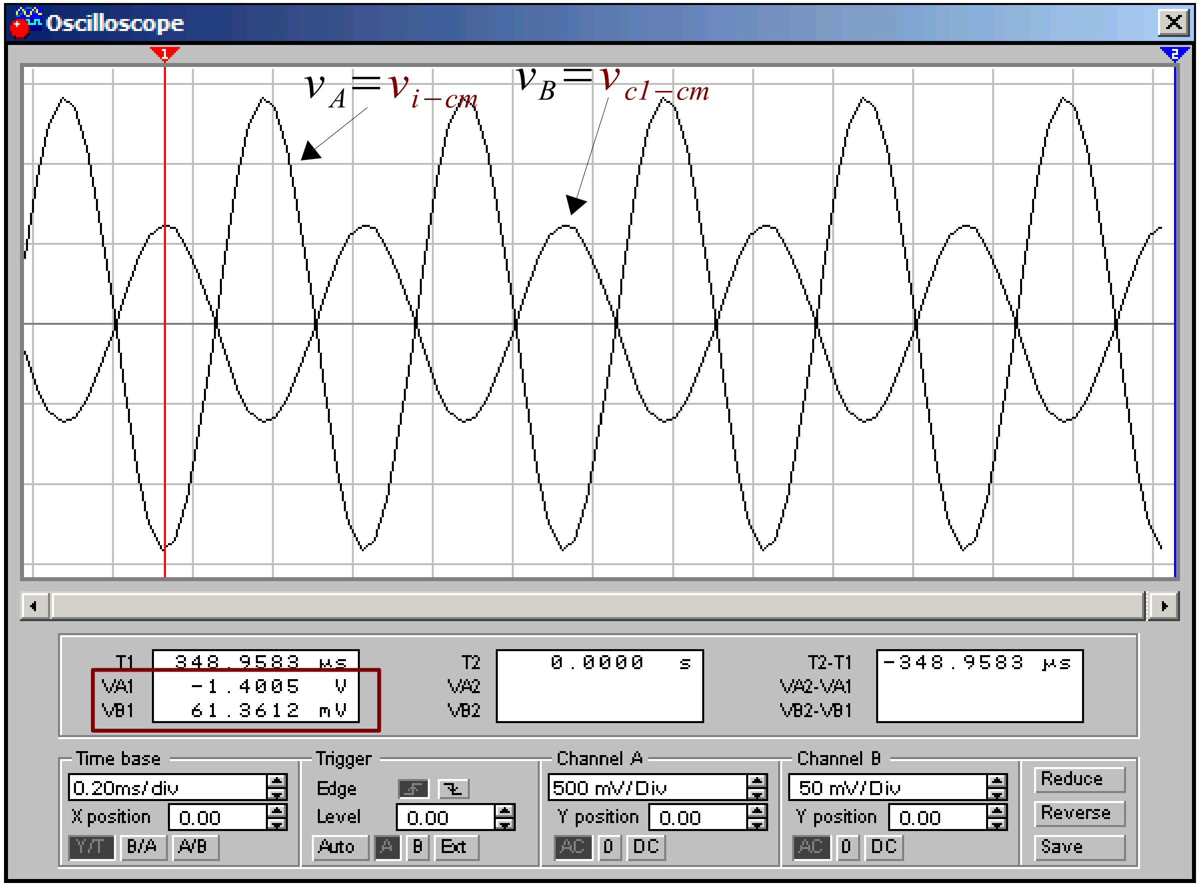
$$\Rightarrow I_{C1} = I_{C2} \approx 5\,mA$$

$$R_{ref} = 2.33\,k\,\Omega$$

$$I_{REF} = \frac{V_{CC} - V_{BE4} - V_{EE}}{R_{ref}} \approx 10\,mA$$

NOTE: - The zero-to-peak ac voltage swing across each R_C increased to $5\ V$!

Simulation with Current Mirror - III



$$A_{v-cm1} \approx \frac{-0.06}{1.4} = -0.043$$

Input voltage $v_A = v_{i-cm}$
$1.4\ V_{peak}\ arg\ (0^o)$ at $f = 1\ kHz$.

Output voltage $v_B = v_{c1-cm}$
$60\ mV_{peak}\ arg\ (180^o)$.

$$A_{v-cm1} \approx -0.043$$

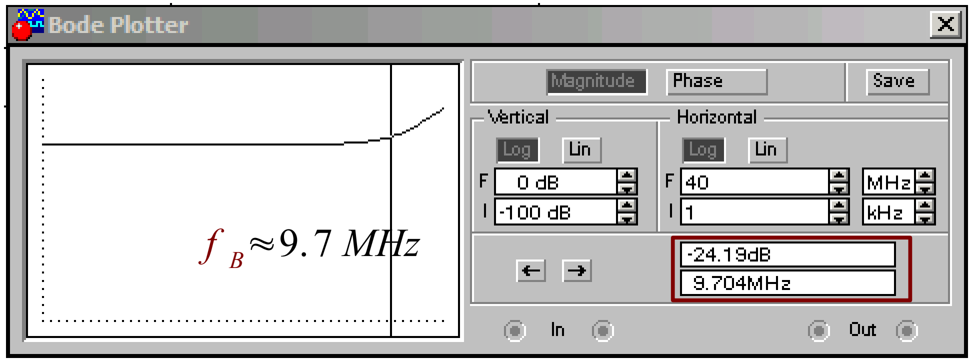
Common mode output now about $10X$ its previous value with $0.5\ mA$. collector current.

Why? Early effect!

$$r_o = \frac{V_A}{I_C} \approx 10\, k\,\Omega$$

10 times the current means $1/10$ the value of r_o!

Simulation with Current Mirror - Bode Plots



5 mA current: $A_{v\text{-}cm1(dB)}$ + *3 dB* frequency

$r_o \approx 10k\,\Omega \quad (I_{REF} = 10\ mA)$

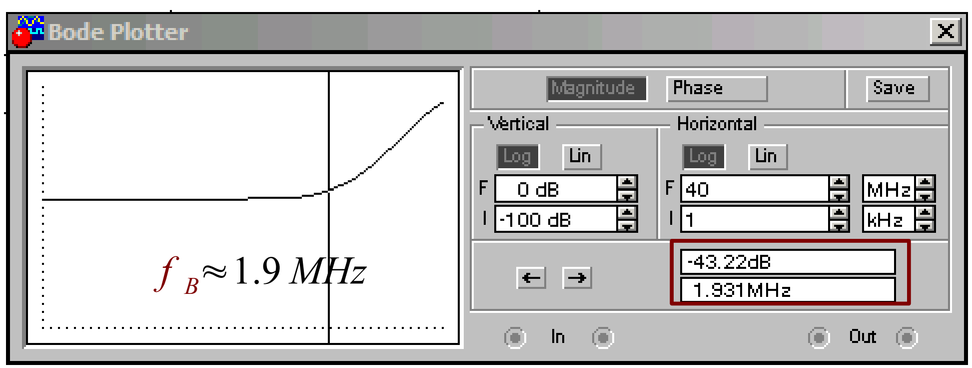
$A_{v-cm1(dB)}(f=1\,kHz) \approx 20\log_{10}(\frac{0.06}{1.4}) = -27.3\,dB$

$A_{v-cm1(dB)}(f=9.7\ MHz) = -24.2\,dB \quad (+\,3dB)$

$$f_B \approx \frac{1}{2\pi r_o C_o} \Rightarrow$$

theory $\quad \frac{f_{B(1\,mA)}}{f_{B(10\,mA)}} \approx \frac{r_{o(10\,mA)}}{r_{o(1\,mA)}} = \frac{10k}{100k} = 0.1$

simulation $\quad \frac{f_{B(1\,mA)}}{f_{B(10\,mA)}} = \frac{1.9\ MHz}{9.7\ MHz} = 0.2$



0.5 mA current: $A_{v\text{-}cm1(dB)}$ + *3 dB* frequency

$r_o \approx 100k\,\Omega \quad (I_{REF} = 1\ mA)$

$A_{v-cm1(dB)}(f=1\,kHz) \approx 20\log_{10}(\frac{0.007}{1.4}) = -46\,dB$

$A_{v-cm1(dB)}(f=1.9\ MHz) = -43.2\,dB \quad (+\,3dB)$

Summary & Comparison

$I_{REF}=1\,mA$

$$V_{RC1}\approx\frac{I_{REF}}{2}R_{C1}=0.5\,V$$

$$r_o\approx\frac{V_A}{I_{REF}/2}=100\,k\,\Omega$$

$$A_{v-cm1}=\frac{-R_{C1}}{2\,r_o}\approx\frac{-0.007}{1.4}=-0.005$$

$$f_B\approx1.9\,MHz$$

$$A'_{v-dm1}=-9.5$$

$I_{REF}=10\,mA$

$$V_{RC1}\approx\frac{I_{REF}}{2}R_{C1}=5\,V$$

$$V_{RC1}\approx\frac{I_{REF}}{2}R_{C1}=5\,V$$

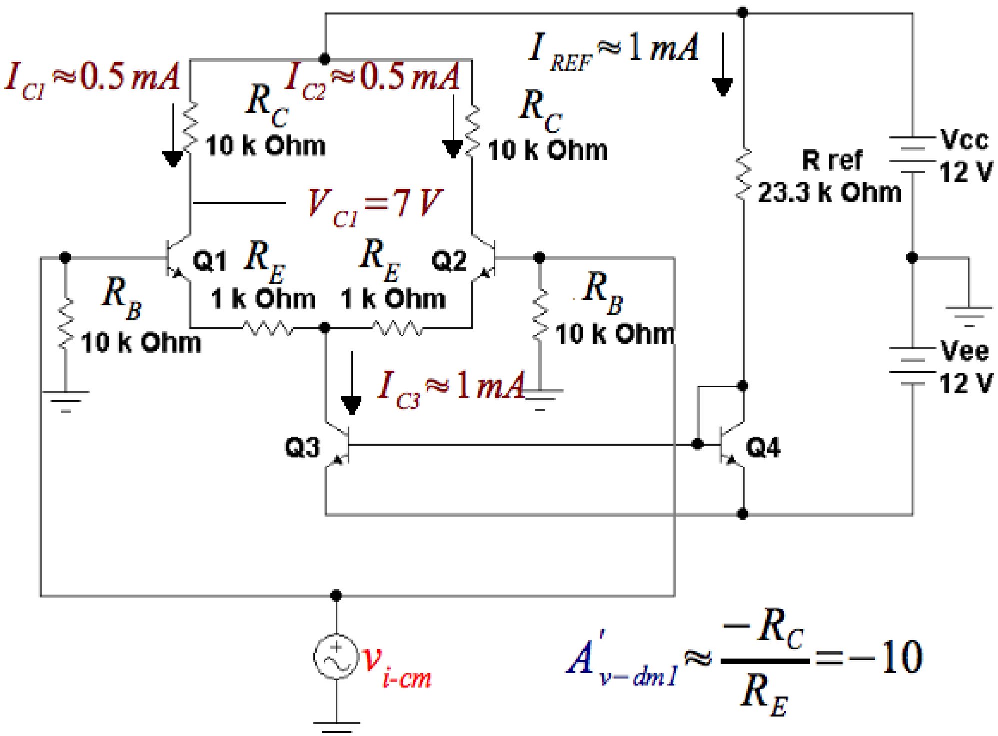
$$A_{v-cm1}=\frac{-R_{C1}}{2\,r_o}\approx\frac{-0.06}{1.4}=-0.043$$

$$f_B\approx9.7\,MHz$$

$$A'_{v-dm1}=-9.5$$

Try Redesign for Reasonable Differential Mode Voltage Swing & large r_o

$I_{C3}=1\,mA \Rightarrow r_o \approx 100\,k\Omega$



$A'_{v-dm1} \approx \frac{-R_C}{R_E} = -10$

$A_{v-cm1} \approx -\frac{R_C}{2 r_o}$

Can we beat the r_o trade-off?

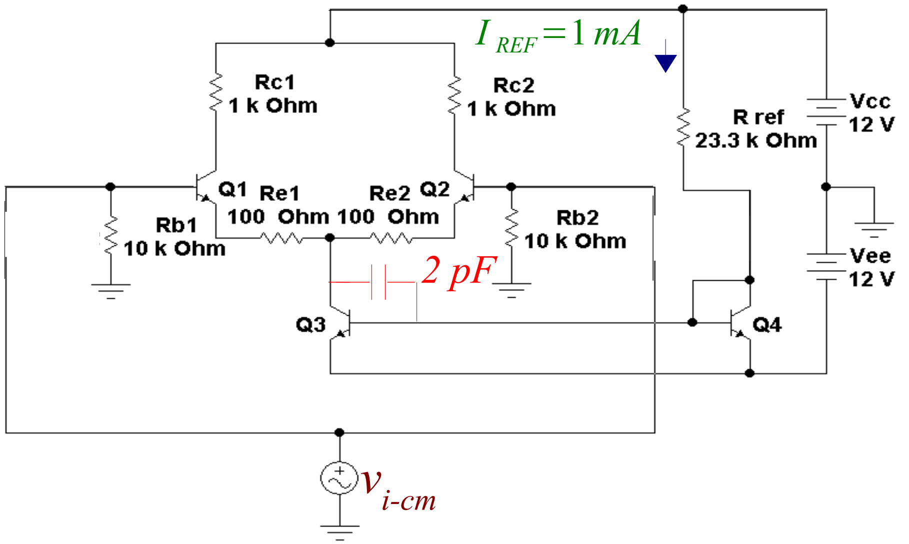
IDEA:

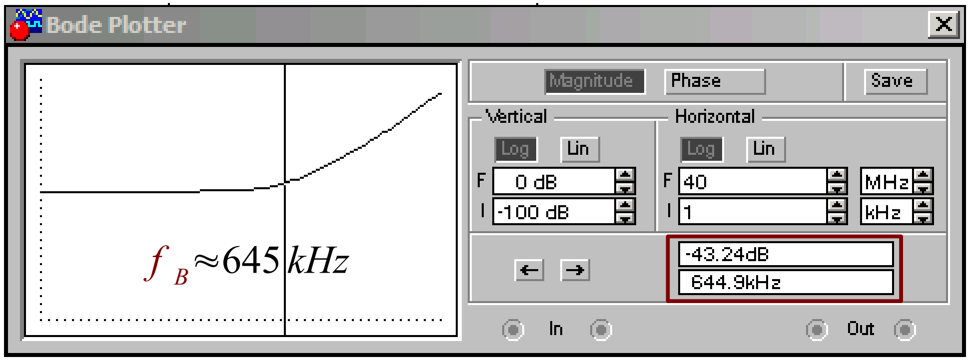
1. Reduce I_{REF} to increase r_o.
$$r_o \approx \frac{V_A}{I_{REF}}$$
2. Increase R_C to increase V_{RC1}.
$$V_{RC1} = R_C \frac{I_{REF}}{2}$$
3. Increase R_E to retain desired A'_{v-dm1}.
$$A'_{v-dm1} = \frac{R_C}{R_E}$$

$$A_{v-cm1} \approx -\frac{R_C}{2 r_o} = -\frac{V_{RC1}}{I_{REF}/2}\frac{I_{REF}}{2 V_A} = -\frac{V_{RC1}}{V_A}$$

RESULT: No help!

Simulations with Parasitic Caps





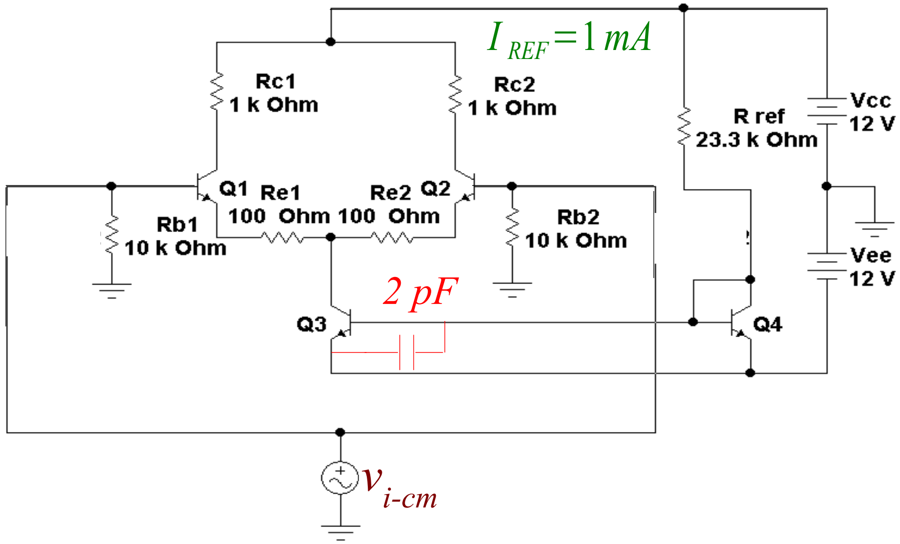
$$A_{v-cm1(dB)}(f=1\ kHz)\approx 20\log_{10}\left(\frac{0.007}{1.4}\right)=-46\ dB$$

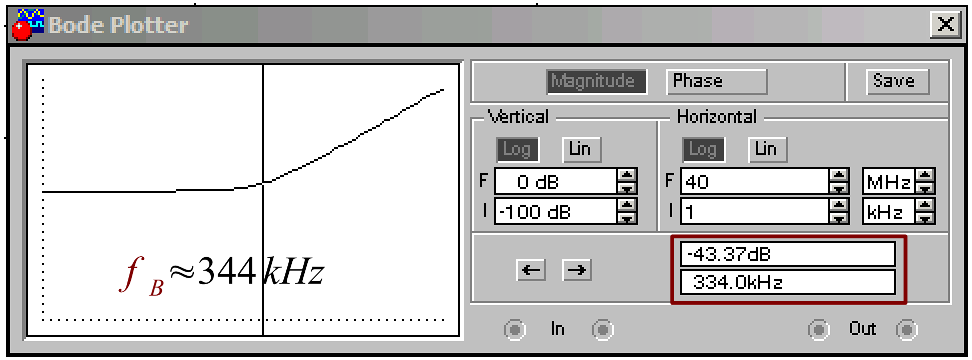
$$A_{v-cm1(dB)}(f=645\ kHz)=-43.2\ dB$$

Results with $2\ pF$ capacitance added from collector-to-base of mirror transistor in the "$I_{C1} = I_{C2} = 0.5\ mA$ amplifier" emitter return path.

This drops the amplifier $A_{v\text{-}cm1(dB)}$ $+\ 3\ dB$ frequency from $1.9\ MHz$ to about $645\ kHz$!

Simulations with Parasitic Caps - cont.





$$A_{v-cm1(dB)}(f=1\,kHz)\approx 20\log_{10}\left(\frac{0.007}{1.4}\right)=-46\,dB$$

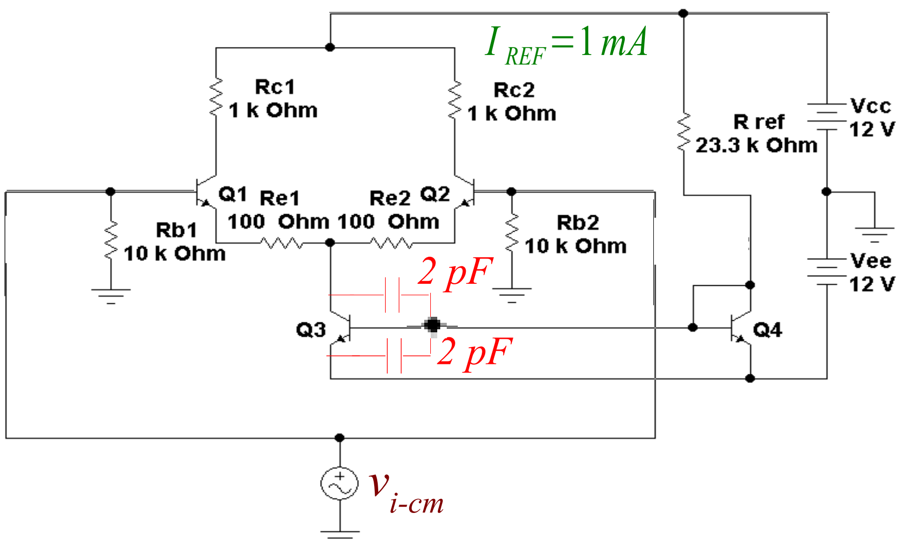
$$A_{v-cm1(dB)}(f=334\,kHz)=-43.2\,dB$$

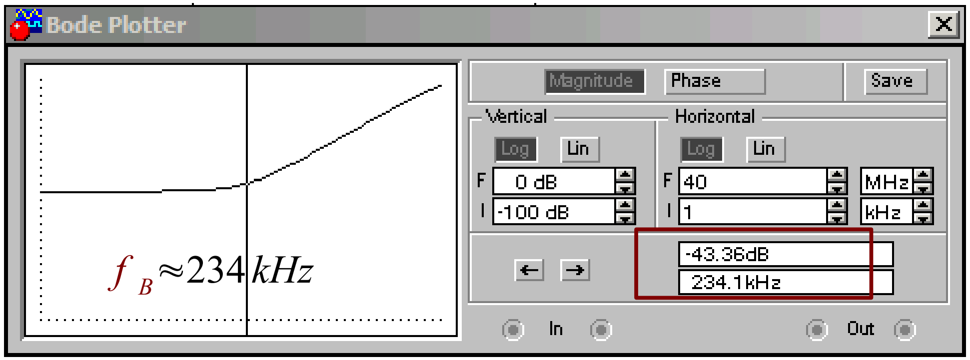
Results with $2\ pF$ capacitance added from base-to-emitter of mirror transistor.

This drops the amplifier $A_{v\text{-}cm1(dB)}$ $+3\ dB$ frequency from $1.9\ MHz$ to about $334\ kHz$!

RECALL: $2\ pF$ is about the capacitance between 2 rows of Protoboard pins!

Simulations with Parasitic Caps - cont.



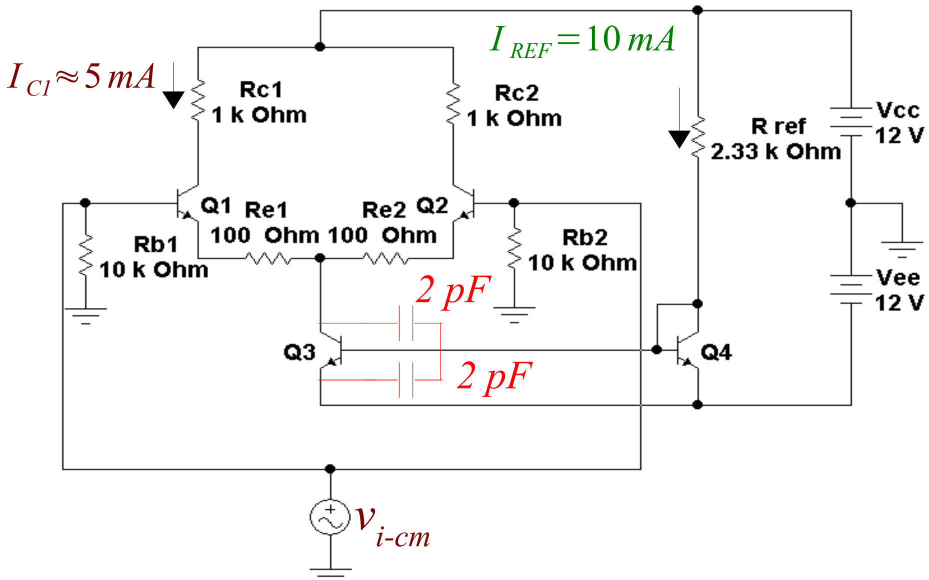


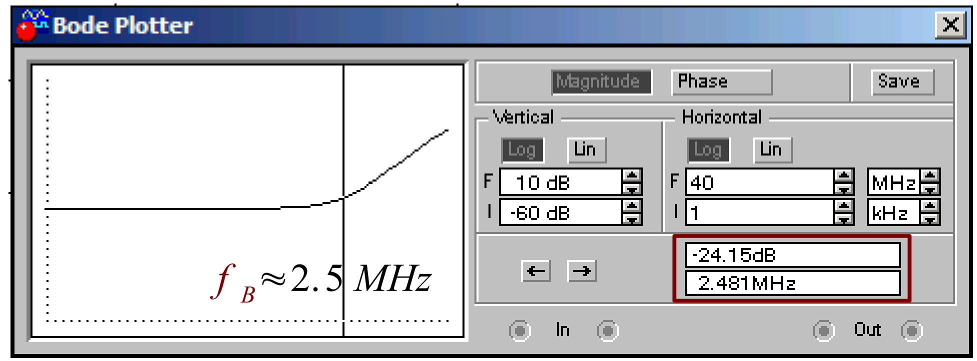
$$A_{v-cm1(dB)}(f = 1\,kHz) \approx 20\log_{10}\left(\frac{0.007}{1.4}\right) = -46\,dB$$

$$A_{v-cm1(dB)}(f = 234\,kHz) = -43.2\,dB$$

Drops amplifier $A_{v\text{-}cm1(dB)}$ break frequency from $1.9\ MHz$ to about $234\ kHz$!

Simulate the $5\ mA$ Design with $2\ pF$ Parasitics





$$A_{v-cm1(dB)}(f=1\ kHz) \approx -27\ dB$$

$$A_{v-cm1(dB)}(f=2.5\ MHz) = -24.2\ dB$$

Parasitic caps drop amplifier $A_{v\text{-}cm(dB)}$ break frequency from $9.7\ MHz$ to about $2.5\ MHz$!

3dB common mode bandwidth with $2\ pF$ base-emitter and base collector capacitances.

	$I_{REF}=10\ mA$	$I_{REF}=1\ mA$
f_B	$2.5\ MHz$	$234\ kHz$
$A_{v-cm1(dB)}(f=1\ kHz)$	$-27\ dB$	$-46\ dB$
$A'_{v-dm1(dB)}(f=1\ kHz)$	$+20\ dB$	$+20\ dB$

About *10X* the bandwidth as the $I_{REF} = 1\ mA$ design.

Observations

1). For best common mode rejection use small collector currents i.e. increase r_o.

2). For best bandwidth use large collector currents, i.e. decrease r_o.

3). Minimize parasitic capacitance around mirror transistor to increase common mode rejection bandwidth.

4). Since no differential mode current flows through the mirror transistor (Q3, i.e. r_o), it should have no effect on differential mode performance.

5). Observations 1) and 2) force a trade-off in selecting the bias current.

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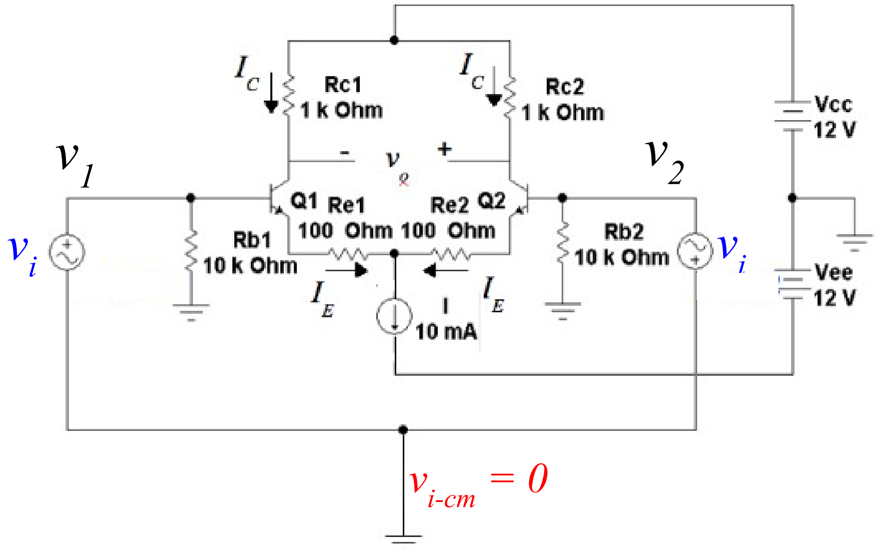

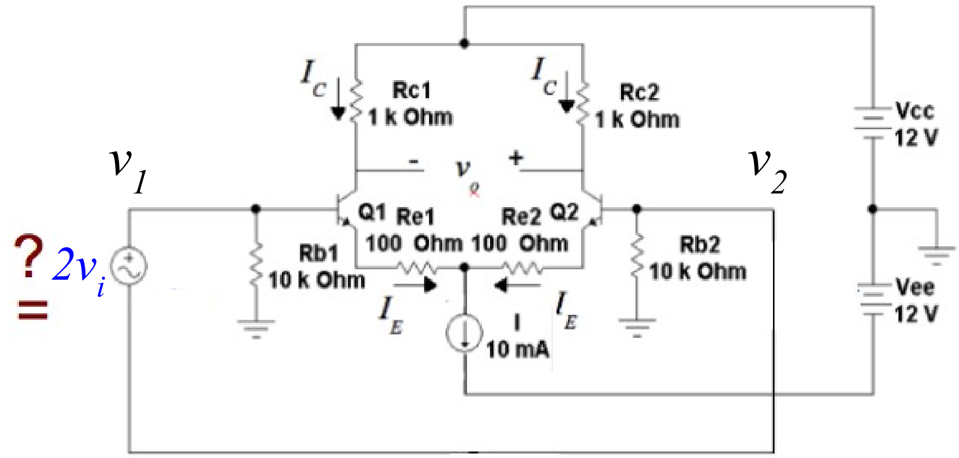

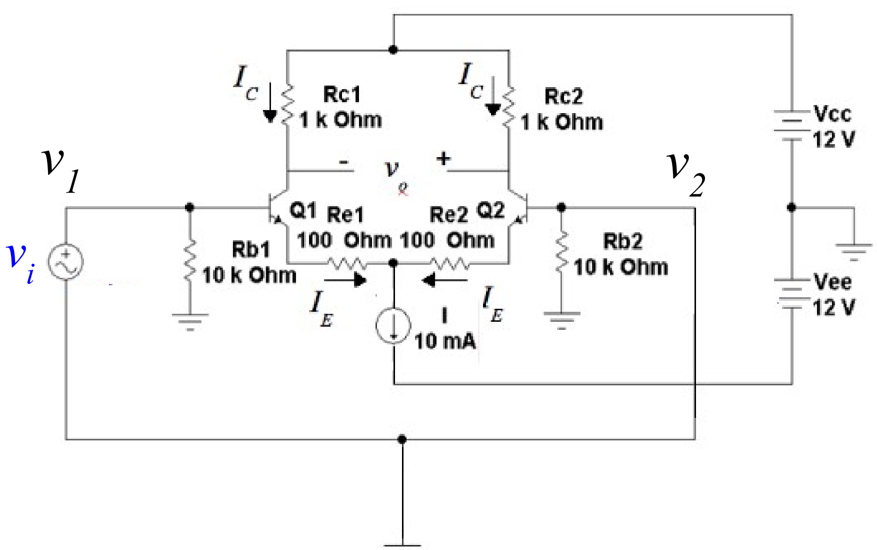

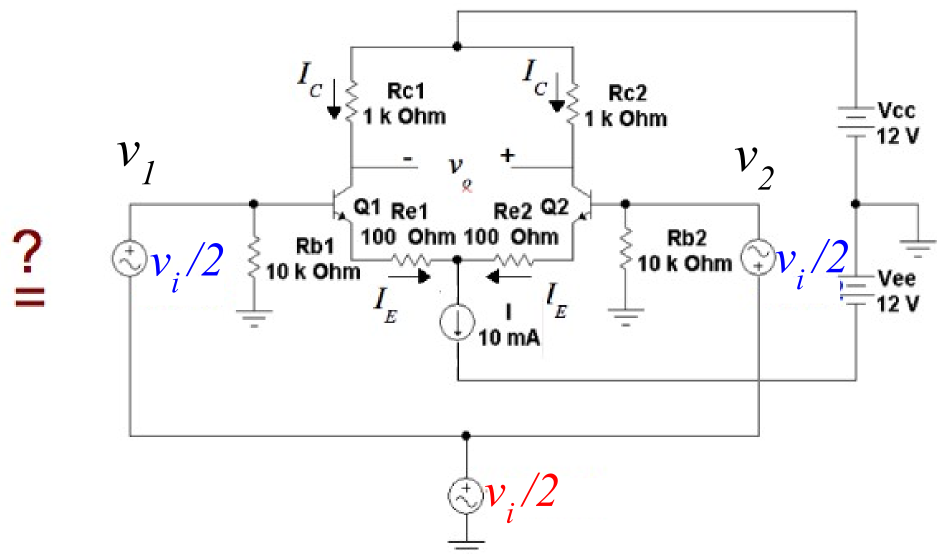

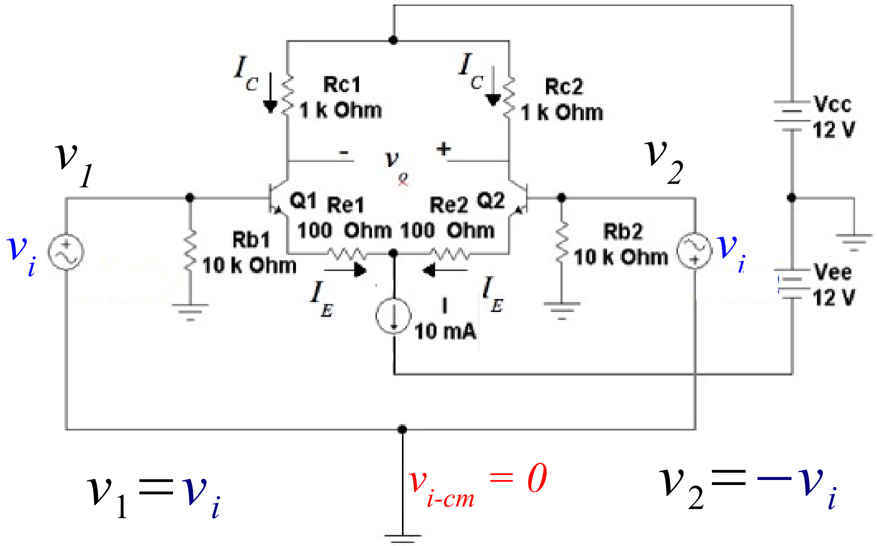

$v_1 = v_i$ $\quad$ $v_2 = -v_i$

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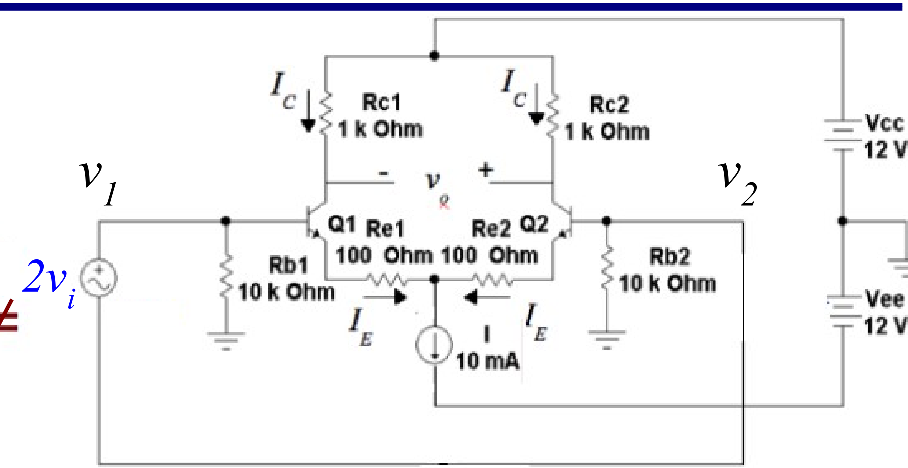
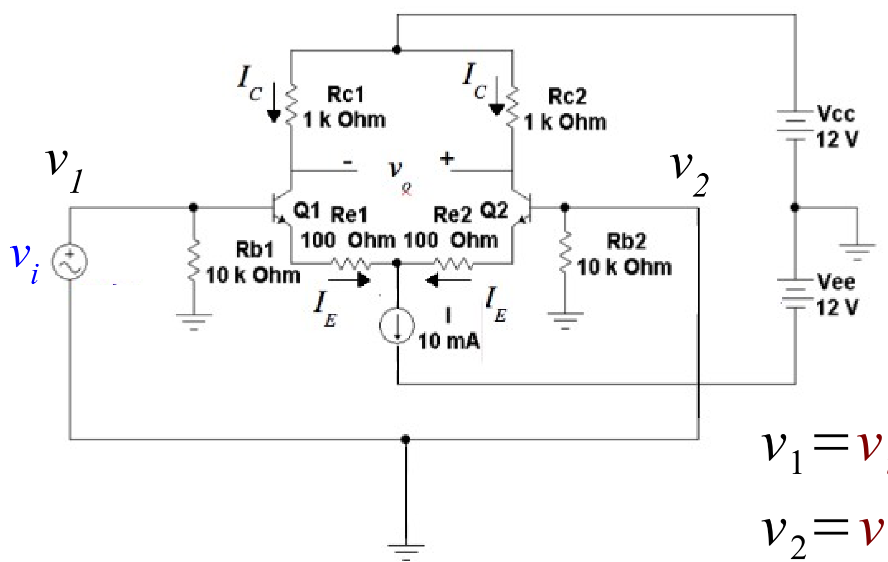


$v_1 - v_2 = 2\, v_i$ $\quad$ $v_1 \neq v_i$ $\quad$ $v_2 \neq -v_i$



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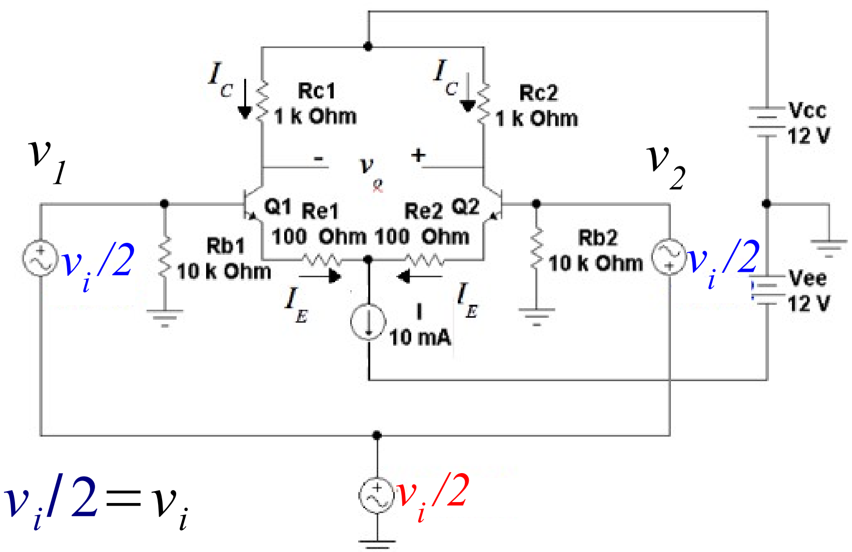

$$v_1 = v_i/2 + v_i/2 = v_i$$

$$v_2 = v_i/2 - v_i/2 = 0$$