



## Brief Review

### Comparison of 1 mA & 10 mA CM Results

$$I_{REF} = 1 \text{ mA}$$

$$r_o \approx \frac{V_A}{I_{REF}/2} = 100 \text{ k}\Omega$$

$$A_{v-cm1} = \frac{-R_{Cl}}{2r_o} \approx \frac{-0.007}{1.4} = -0.005$$

$$f_B \approx 1.9 \text{ MHz}$$

$$A'_{v-dm1} = -9.5$$

$$I_{REF} = 10 \text{ mA}$$

$$V_{RC1} \approx \frac{I_{REF}}{2} R_{Cl} = 5 \text{ V}$$

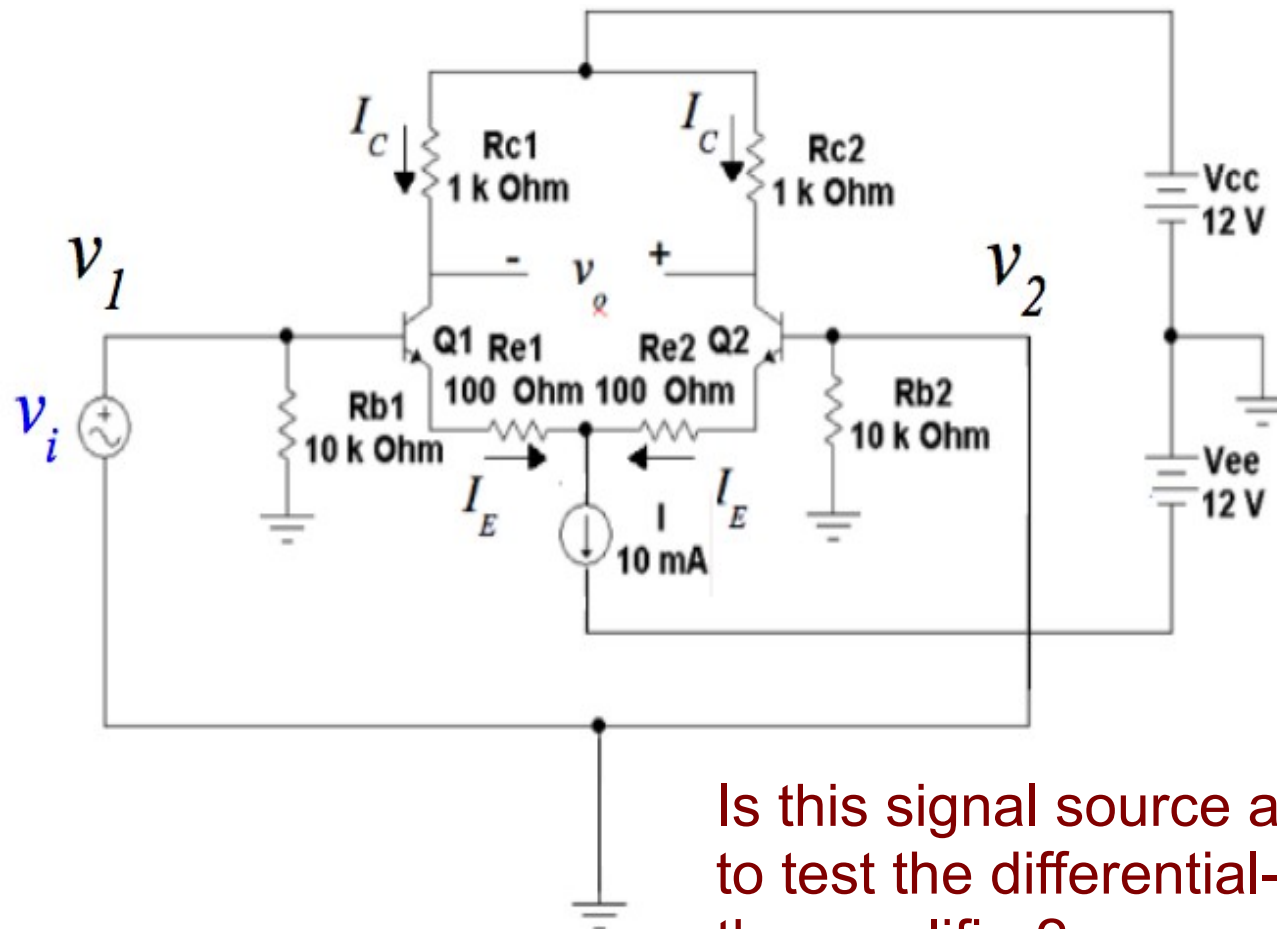
$$A_{v-cm1} = \frac{-R_{Cl}}{2r_o} \approx \frac{-0.06}{1.4} = -0.043$$

$$f_B \approx 9.7 \text{ MHz}$$

$$A'_{v-dm1} = -9.5$$

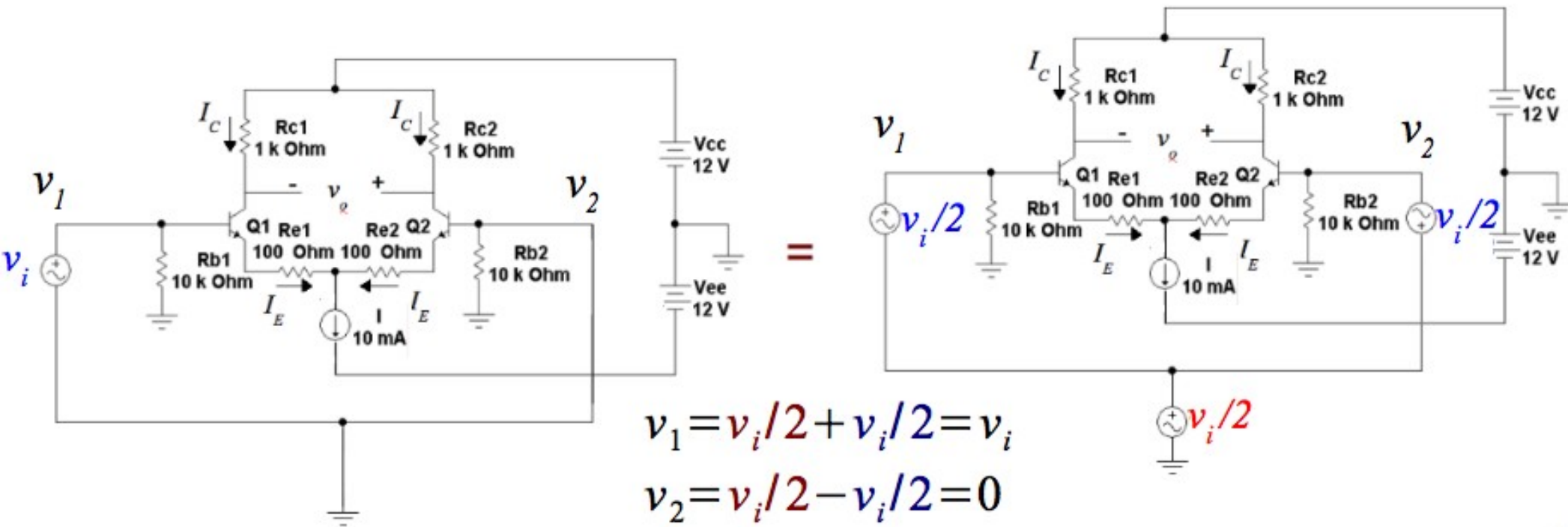
$$A_{v-cm1} \approx -\frac{V_{RC1}}{V_A}$$

## Brief Review



Is this signal source arrangement a suitable to test the differential-mode performance of the amplifier?

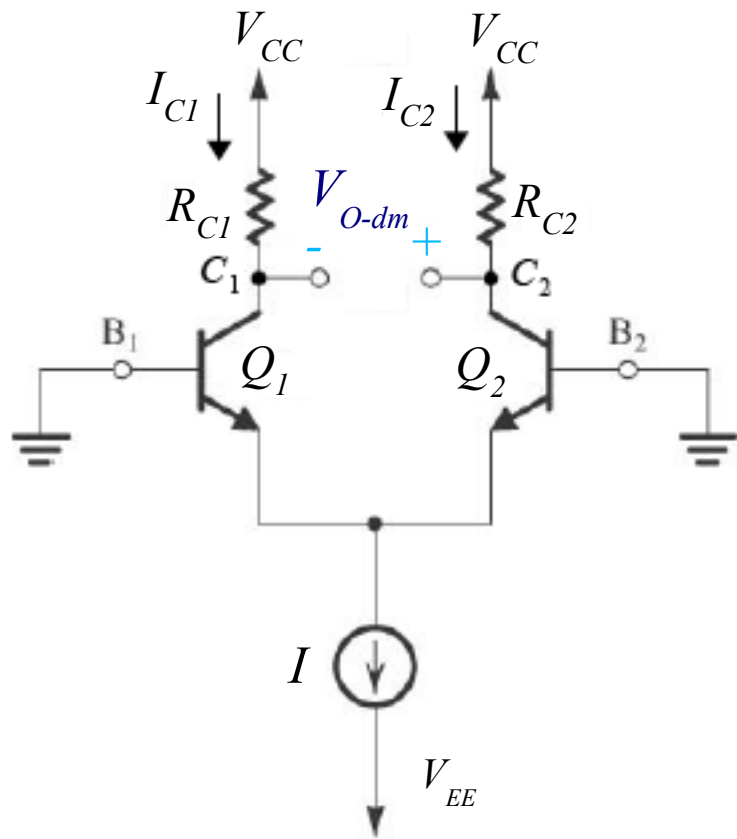
## Brief Review



## *Differential Amplifier Offset*

- Causes of dc voltage and current offset
- Modeling dc offset
  - $R_C$  mismatch
  - $I_S$  mismatch
  - $\beta$  mismatch
- dc offsets in differential amplifiers due to component mismatch can be modeled as **differential** phenomena

transistor mismatch



1. Consider the emitter-current bias case where bases of matched Q1 and Q2 are connected to ground.
2. To further simplify, let there be no external base and emitter resistors.
3. Let the mismatch be in  $R_C$  where  $R_{C1} \neq R_{C2}$ .

$$V_{C1} = V_{CC} - R_{C1} I_{C1}$$

$$V_{C2} = V_{CC} - R_{C2} I_{C2}$$

$$V_{O-dm} = V_{C2} - V_{C1} \quad (= 0 \text{ ideally})$$

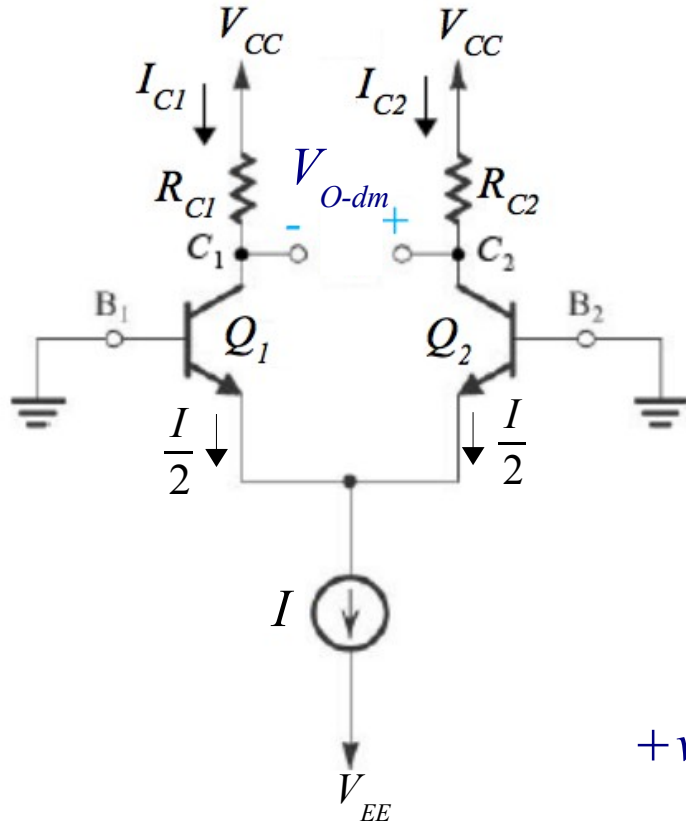
Since  $Q1=Q2$  and  $I$  is fixed, currents are matched i.e.

$$I_{C1} = I_{C2} = \frac{\beta}{\beta + 1} \frac{I}{2} = \alpha \frac{I}{2}$$

$$V_{O-dm} = -R_{C2} I_{C2} - (-R_{C1} I_{C1}) = R_{C1} I_{C1} - R_{C2} I_{C2}$$

$$\text{if } V_{O-dm} = 0 \Rightarrow R_{C1} I_{C1} = R_{C2} I_{C2}$$

$$\Rightarrow R_{C1} = R_{C2}$$



Let:  $R_{C1} \neq R_{C2}$  s.t.  $R_{C2} > R_{C1}$

Split the mismatch between both collector resistors, and decompose into **common** and **differential** components:

$$R_C = \frac{R_{C2} + R_{C1}}{2} \quad (\text{common})$$

$$\Delta R_C = R_{C2} - R_{C1} \quad (\text{differential})$$

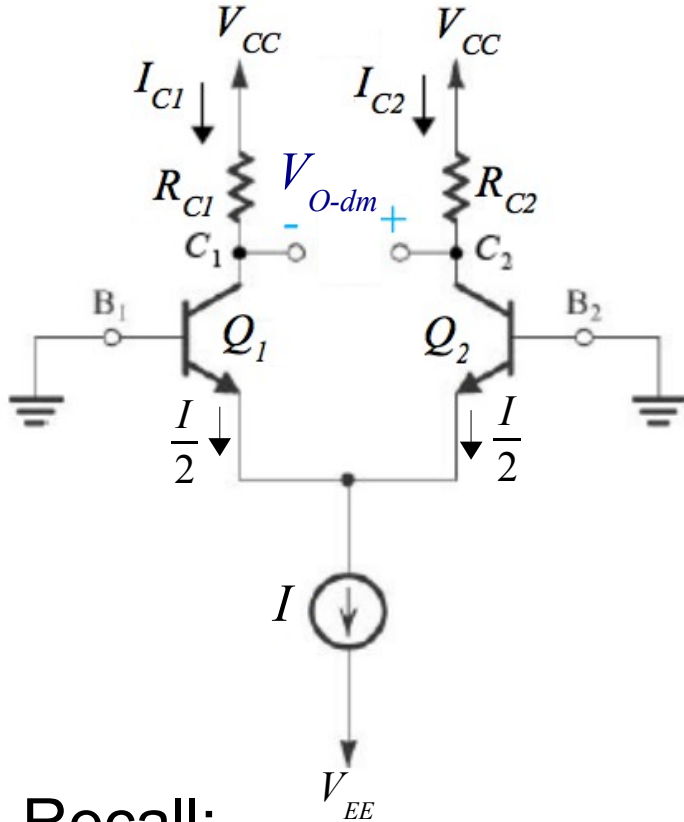
Then, it can be shown that:

$$R_{C2} = R_C + \frac{\Delta R_C}{2} = R_C \left( 1 + \frac{1}{2} \frac{\Delta R_C}{R_C} \right)$$

$$R_{C1} = R_C - \frac{\Delta R_C}{2} = R_C \left( 1 - \frac{1}{2} \frac{\Delta R_C}{R_C} \right)$$

Assume matched currents:

$$I_{C1} = I_{C2} = \alpha \frac{I}{2}$$



Hence

$$V_{O-dm} = \left( R_C + \frac{\Delta R_C}{2} \right) I_{C2} - \left( R_C - \frac{\Delta R_C}{2} \right) I_{C1}$$

$$V_{O-dm} = \left( R_C + \frac{\Delta R_C}{2} \right) \alpha \frac{I}{2} - \left( R_C - \frac{\Delta R_C}{2} \right) \alpha \frac{I}{2}$$

or:

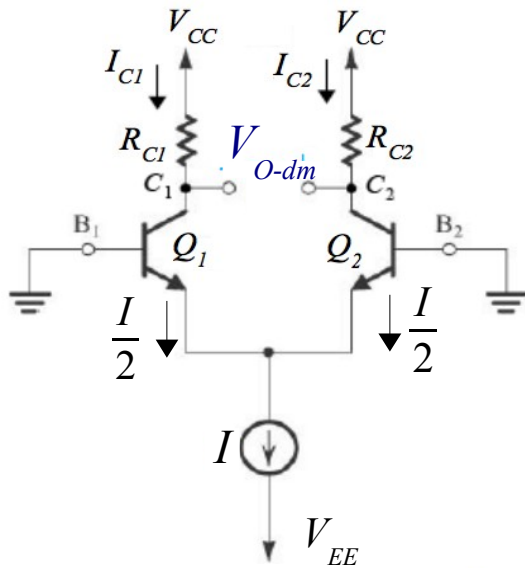
$$V_{O-dm} = \alpha \frac{I}{2} \boxed{\Delta R_C}$$

random variable (rv)  
output offset voltage

Recall:

$$V_{O-dm} = R_{C2} I_{C2} - R_{C1} I_{C1}$$

$$I_{C1} = I_{C2} = \alpha \frac{I}{2} \quad R_{C1} \neq R_{C2}$$



Collector-collector voltage due to resistor mismatch:

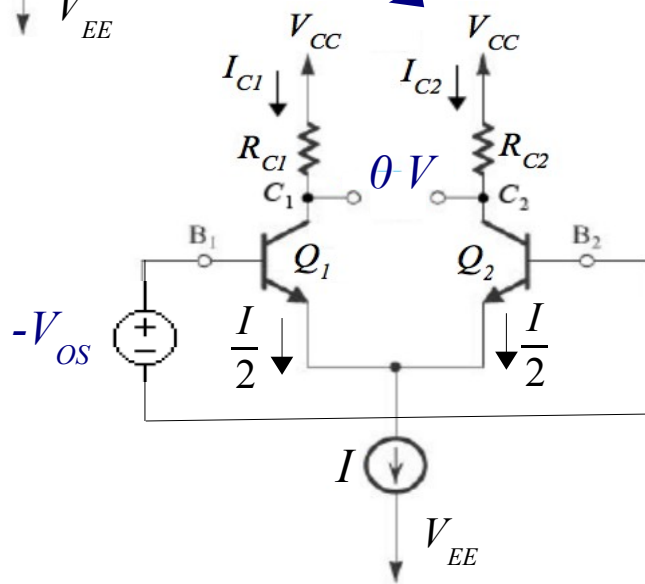
$$V_{O-dm} = \alpha \frac{I}{2} \Delta R_C$$

Define the **input offset voltage** as that input voltage that will cancel  $V_{O-dm}$ . If the amplifier differential gain

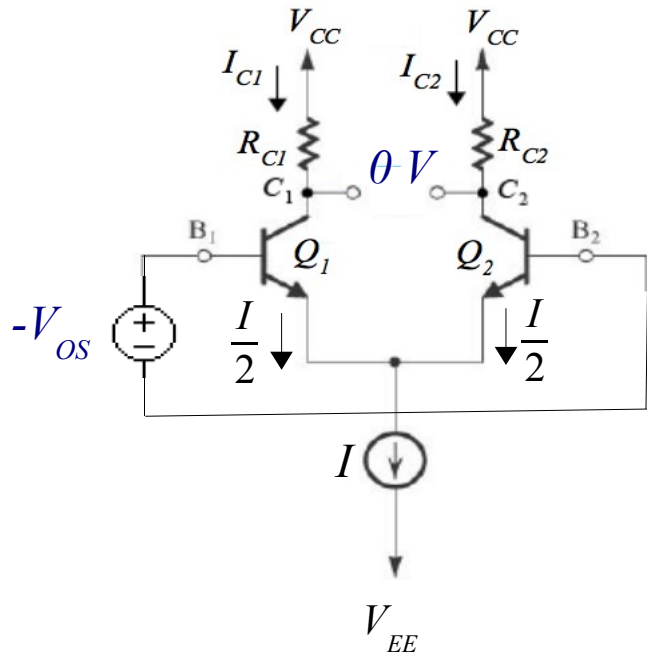
is  $A_{v-dm}$ :

$$V_{OS} \equiv \frac{V_{O-dm}}{A_{v-dm}}$$

$V_{OS}$  is highly variable, rv & can be + or -



Input offset voltage is the output offset voltage referred to the input due to **mismatch**  $\Delta R_C$ .



$$V_{OS} = \frac{\alpha \frac{I}{2} \Delta R_C}{g_m R_C}$$

$$g_m = \frac{I_C}{V_T} = \alpha \frac{I}{2} \frac{1}{V_T}$$

Input referred offset due to  $\Delta R_C$  mismatch:

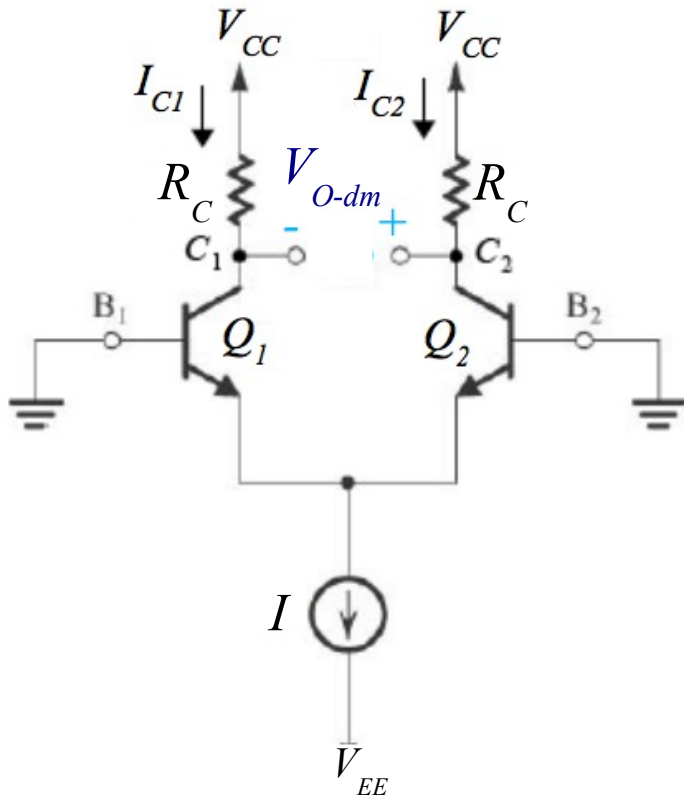
$$V_{OS} = \frac{V_{O-dm}}{A_{v-dm}} \quad \text{where} \quad V_{O-dm} = \alpha \frac{I}{2} \Delta R_C$$

$$A_{v-dm} = g_m R_C$$

$$V_{OS(\Delta R_C)} = V_T \frac{\Delta R_C}{R_C}$$

random variable

## Offset Voltage From Transistor Mismatch



Perfect balance requires:

$$V_{O-dm} = 0 \Rightarrow R_{C1} I_{C1} = R_{C2} I_{C2}$$

Previous case considered  $R_{C1} \neq R_{C2}$   
&  $Q1 = Q2 \Rightarrow I_{C1} = I_{C2}$ .

Consider now  $Q1 \neq Q2 \Rightarrow I_{C1} \neq I_{C2}$ .

ASSUME: 1.  $R_{C1} = R_{C2} = R_C$

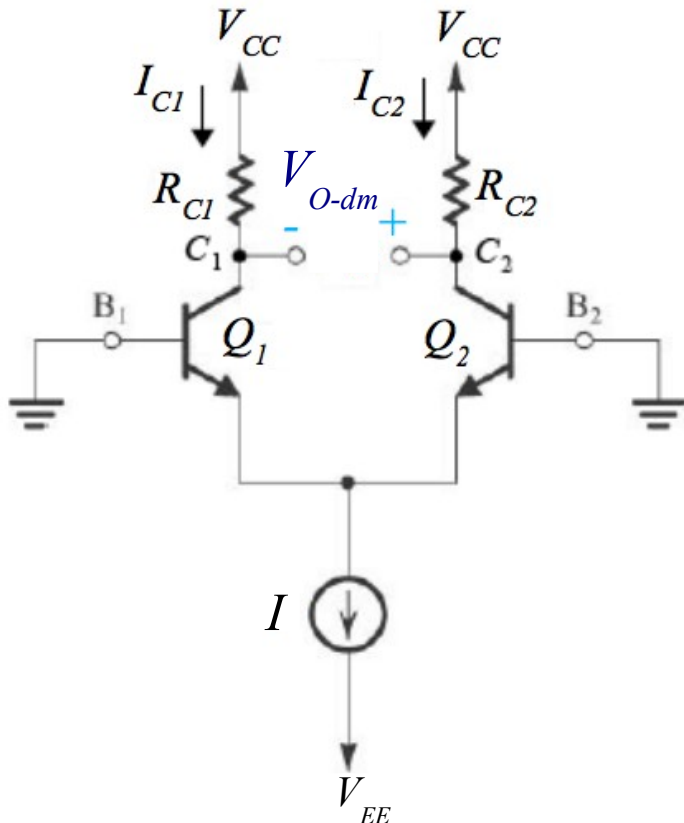
2.  $V_{BE1} = V_{BE2}$

3.  $V_{T1} = V_{T2}$

Only difference is in the saturation currents of the transistors, i.e.

$$I_{S1} \neq I_{S2}$$

Again using **common** and **differential** mode concepts:



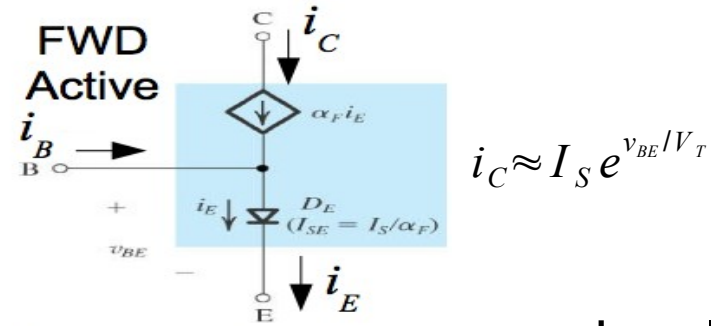
$$I_S = \frac{I_{S2} + I_{S1}}{2}$$

$$\Delta I_S = I_{S2} - I_{S1}$$

The two transistor saturation currents are:

$$I_{S2} = I_S + \frac{\Delta I_S}{2} \quad \leftarrow +v_{i-dm}/2$$

$$I_{S1} = I_S - \frac{\Delta I_S}{2} \quad \leftarrow -v_{i-dm}/2$$



Large signal Model:

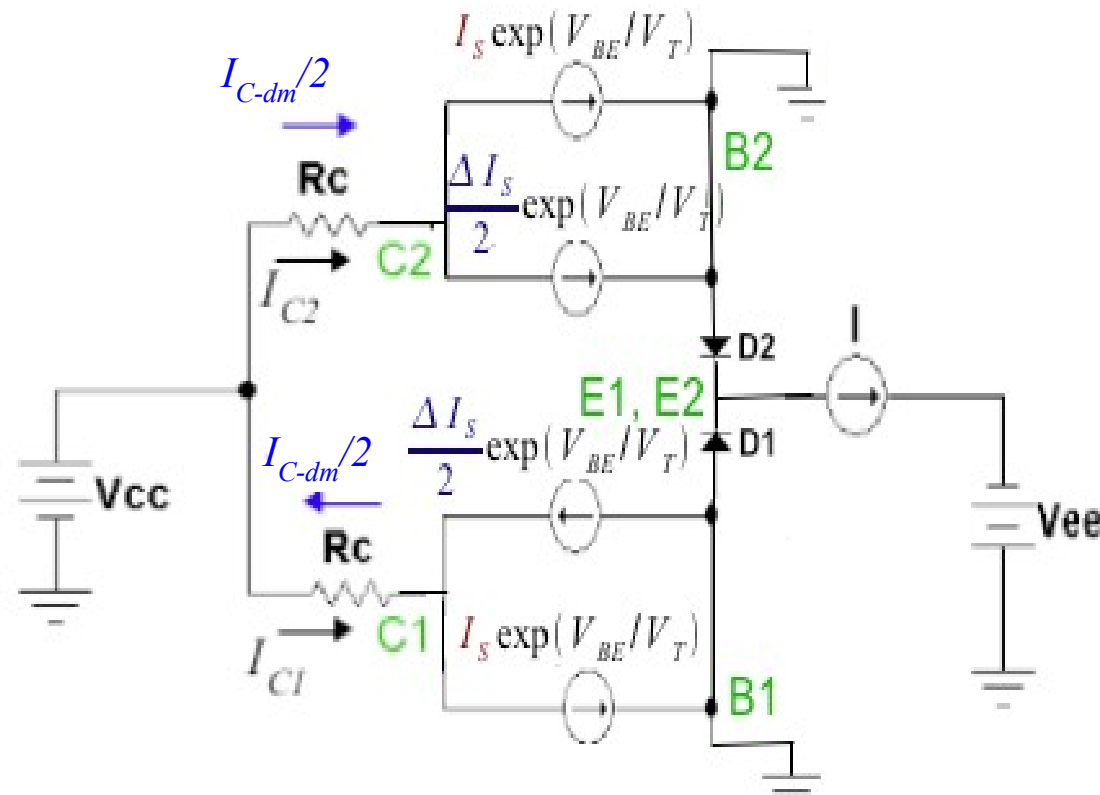
$$I_{C1} = \left( I_S - \frac{\Delta I_S}{2} \right) e^{\frac{V_{BE}}{V_T}}$$

$$I_{C1} = I_S e^{\frac{V_{BE}}{V_T}} - \frac{\Delta I_S}{2} e^{\frac{V_{BE}}{V_T}}$$

also

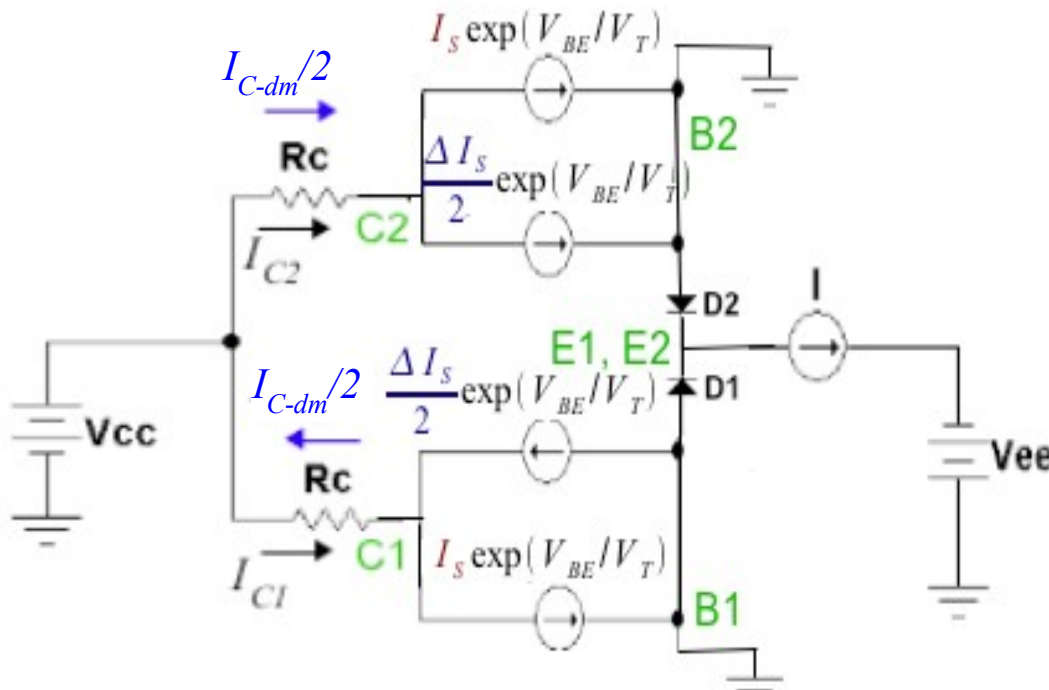
$$I_{C2} = I_S e^{\frac{V_{BE}}{V_T}} + \frac{\Delta I_S}{2} e^{\frac{V_{BE}}{V_T}}$$

The parallel current sources are illustrated in the schematic.





Note: differential  $I_C$  components cause current flow in opposite directions through the  $R_C$ 's resulting in an offset voltage. The common mode  $I_C$  components cause no offset voltage.



$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \approx \frac{I}{2}$$

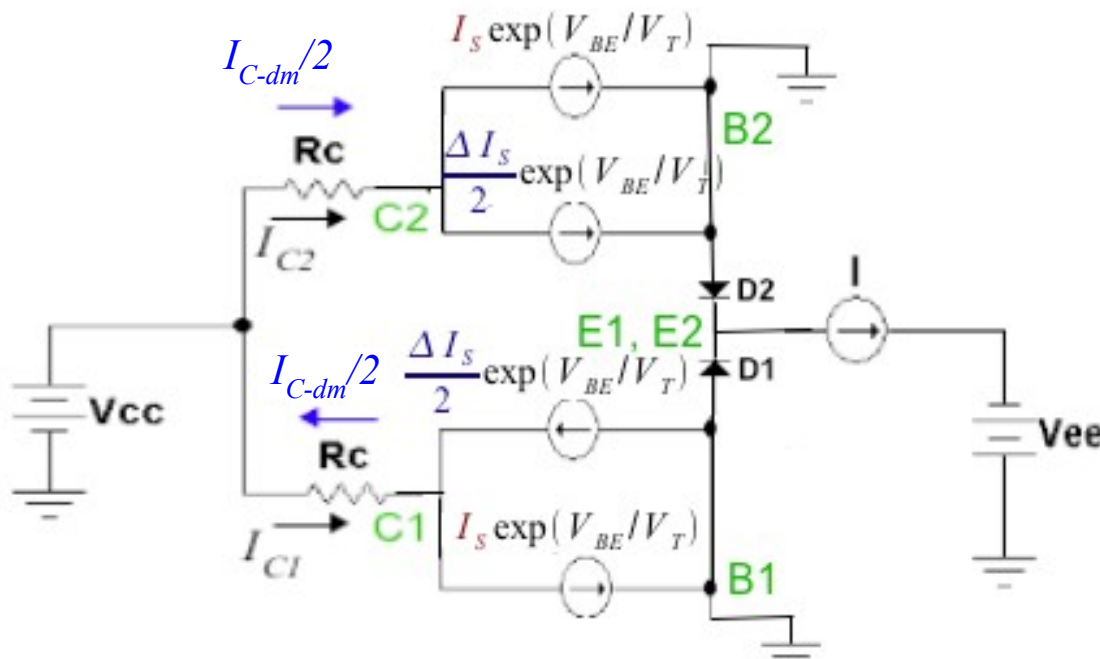
$$I_{C2} = I_S e^{\frac{V_{BE}}{V_T}} + \frac{\Delta I_S}{2} e^{\frac{V_{BE}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{\Delta I_S}{2 I_S}\right)$$

$$\approx \frac{I}{2} \left(1 + \frac{\Delta I_S}{2 I_S}\right)$$

$$I_{C1} = I_S e^{\frac{V_{BE}}{V_T}} - \frac{\Delta I_S}{2} e^{\frac{V_{BE}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} \left(1 - \frac{\Delta I_S}{2 I_S}\right)$$

$$\approx \frac{I}{2} \left(1 - \frac{\Delta I_S}{2 I_S}\right)$$

$$V_{O-dm} = R_C I_{C2} - R_C I_{C1} \approx 2 \frac{I}{2} \frac{\Delta I_S}{2 I_S} R_C = \frac{I}{2} \frac{\Delta I_S}{I_S} R_C$$



$$V_{O-dm} \approx \frac{I}{2} \frac{\Delta I_S}{I_S} R_C$$

$$V_{O-dm} \approx \frac{I}{2} \frac{V_T}{V_T} \frac{\Delta I_S}{I_S} R_C$$

$$V_{O-dm} \approx g_m V_T \frac{\Delta I_S}{I_S} R_C$$

$$V_{OS(\Delta I_S)} = \frac{V_{O-dm}}{A_{v-dm}} = \frac{V_{O-dm}}{g_m R_C} \approx V_T \frac{\Delta I_S}{I_S}$$

Recall:

$$g_m = \frac{I_C}{V_T} \approx \frac{I}{2} \frac{1}{V_T}$$

$$V_{OS(\Delta I_S)} \approx V_T \frac{\Delta I_S}{I_S}$$

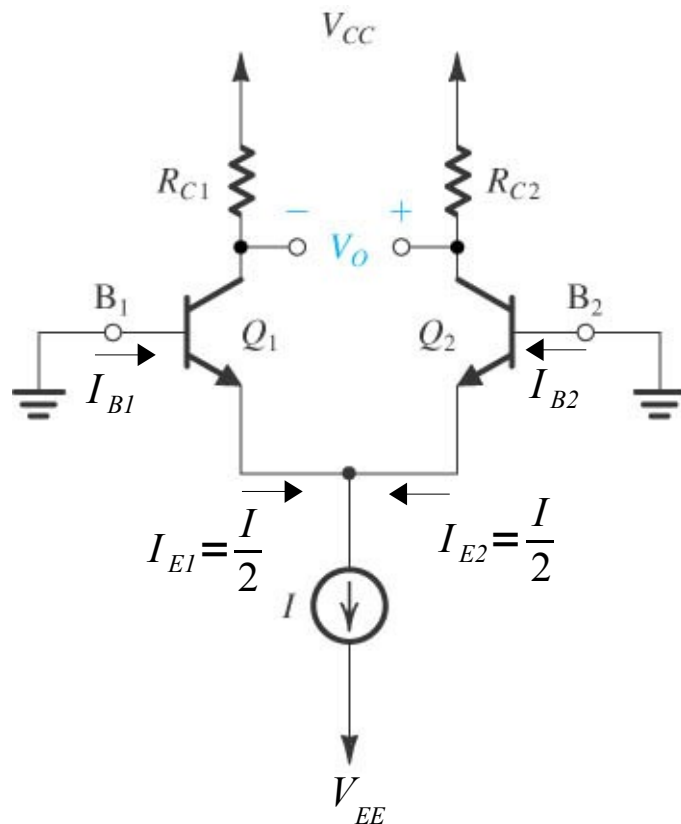
← random variable

## Offset Voltage Summary

1. We considered two sources of offset voltage:
  - a. Unbalanced collector resistors
  - b. Unbalanced saturation currents
    - i. Due to mismatched transistor geometries
2. We ignored base or emitter circuit unbalance
3. Since the relationship between resistor and current unbalances are statistically random and assumed independent, we combine their effect as an rms quantity:

$$V_{OS(rms)} = \sqrt{(V_{OS-\Delta R_C})^2 + (V_{OS-\Delta I_S})^2} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2}$$

## Average & Offset Base (input) Bias Currents



Consider the case where the base currents differ  $I_{B1} \neq I_{B2}$ .

Since  $I_{B1}$  &  $I_{B2}$  are related to bias current  $I$ , their mismatch is due to  $\beta_1 \neq \beta_2$ .

Let's use **differential**-**common** mode models for beta mismatch:

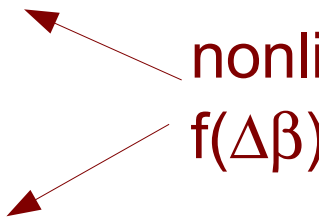
$$\beta_1 = \beta + \frac{\Delta\beta}{2} \quad \leftarrow +v_{i-dm}/2$$

$$\beta_2 = \beta - \frac{\Delta\beta}{2} \quad \leftarrow -v_{i-dm}/2$$

Using this notation, the two base currents are:

$$I_{B1} \approx \frac{I}{2} \frac{1}{\beta_1} = \frac{I}{2} \frac{1}{\beta + \frac{\Delta\beta}{2}} = \frac{I}{2} \frac{1}{\beta} \frac{1}{\left(1 + \frac{\Delta\beta}{2\beta}\right)}$$

$$I_{B2} \approx \frac{I}{2} \frac{1}{\beta_2} = \frac{I}{2} \frac{1}{\beta - \frac{\Delta\beta}{2}} = \frac{I}{2} \frac{1}{\beta} \frac{1}{\left(1 - \frac{\Delta\beta}{2\beta}\right)}$$


  
nonlinear  
f(Δβ)

For  $x < 1$  we can expand the fraction as the series:

$$\frac{1}{1+x} = 1 - x + x^2 - x^3 + \dots$$

where  $x \approx \pm \frac{\Delta\beta}{2\beta}$

Using the expansion and approximating  $\beta + 1 \approx \beta$ :

$$I_{B1} \approx \frac{I}{2} \frac{1}{\beta} \left( 1 - \frac{1}{2} \frac{\Delta\beta}{\beta} \right) \quad I_{B2} \approx \frac{I}{2} \frac{1}{\beta} \left( 1 + \frac{1}{2} \frac{\Delta\beta}{\beta} \right)$$

$$I_{OS} \equiv |I_{B1} - I_{B2}| = \frac{I}{2\beta} \frac{\Delta\beta}{\beta} \quad (\text{input offset current})$$

Since the input bias current  $I_B$  is defined as:  $I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{I}{2\beta}$

The base or input offset current can also be written as:

$$I_{OS(\Delta\beta)} = I_B \left( \frac{\Delta\beta}{\beta} \right)$$

## *DC Offset Voltage & Current Summary*

1. DC offset voltage and current occur due to mismatches in the BJT differential amplifier external resistors and transistor parameters ( $I_s$  and  $\beta$ ).
2. They are imperfections that are inherent to all differential amplifiers and their applications (e.g. op amps).
3. DC offset voltage and current are statistical quantities, i.e. no two differential amplifiers will have the same offset voltage and current.
4. MOS differential amplifiers have zero offset current.