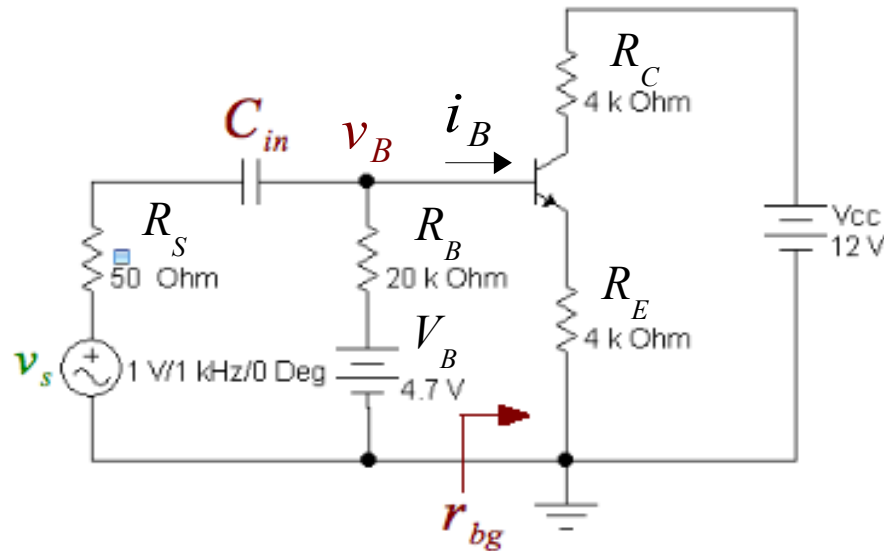
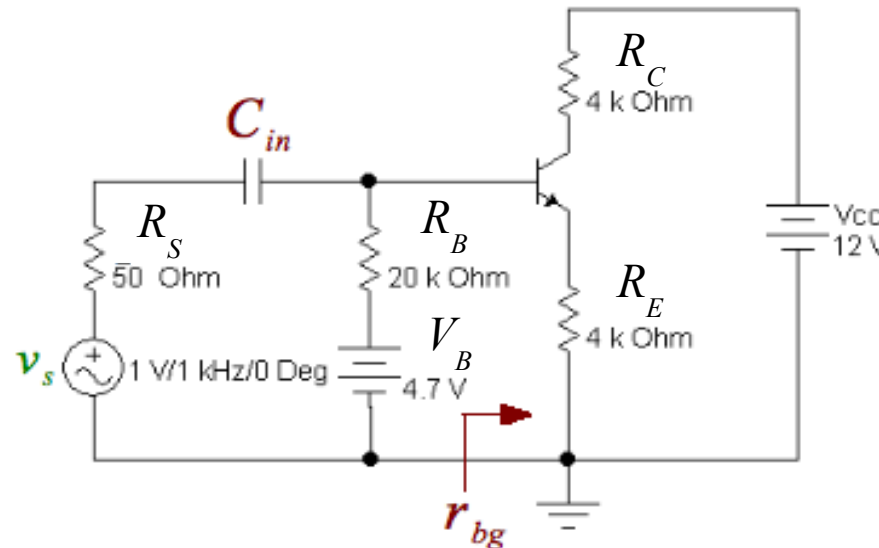


## Quick Review



DESIGN GOAL: What is the design goal for setting the value of  $C_{in}$ ?

## Quick Review

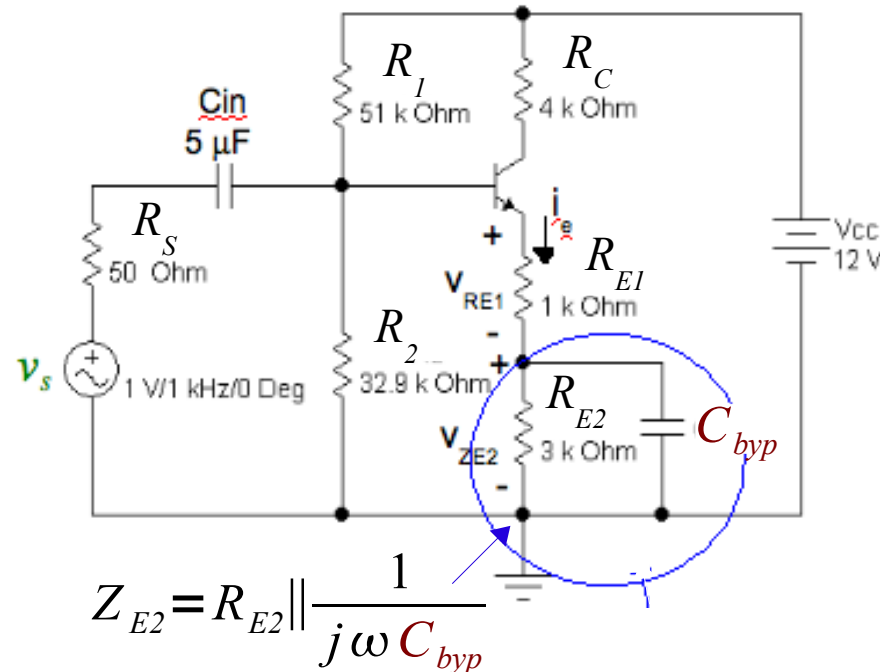


DESIGN GOAL: for  $f \geq f_{min}$ , set the value of  $C_{in}$  so that the ac base voltage

$$v_b \approx v_s.$$

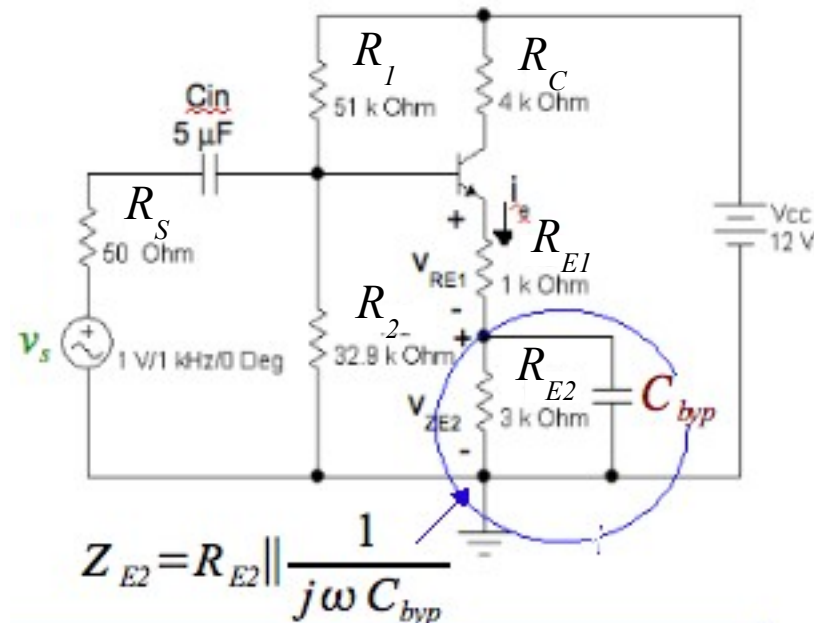
$$R_B \gg \left| \frac{1}{j 2 \pi f C_{in}} \right|$$

## Quick Review



DESIGN GOAL: What is the design goal for setting the value of  $C_{byp}$  ?

## Quick Review



DESIGN GOAL: for  $f \geq f_{min}$ , set the value of  $C_{byp}$  s.t.  $|v_{ZE2}| \ll |v_{RE1}|$ .

$$R_{E1} \gg \frac{1}{2\pi f_{min} C_{byp}}$$



# ***Common Emitter BJT Amplifier Design***

## ***Current Mirror Design***

## Some Observations

- Conditions for stabilized voltage source biasing.
  - Emitter resistance,  $R_E$ , is needed.
  - Base voltage source will have finite resistance,  $R_B$ , *i.e.*  
 $(1 + \beta) R_E \gg R_B \gg R_S$  .
  - **Small  $R_B$  - relative to  $R_S$  - will attenuate input signal.**
  - **Larger  $R_E$  permits larger  $R_B$ , but results in lower gain.**
    - Gain =  $-R_C/R_E$  for  $R_E \gg r_e$ .
  - Split  $R_E$  with bypass capacitor increases gain.
    - Requires large bypass capacitor.
    - Limiting case - entire  $R_E$  bypassed: Gain =  $-g_m R_C$ .
- Ideally  $V_C = V_{CG} = V_{CC} - I_C R_C = V_{CC}/2$ , or conservatively use “1/3, 1/3, 1/3” rule.  $R_C$  determines bias and gain.

## Design Example

Design an amplifier to meet the following specifications:

Electrical specifications:

$$v_{s-max} = 0.1 V \text{ pk}$$

$$R_s = 50 \Omega$$

$$V_{CC} = 12 V$$

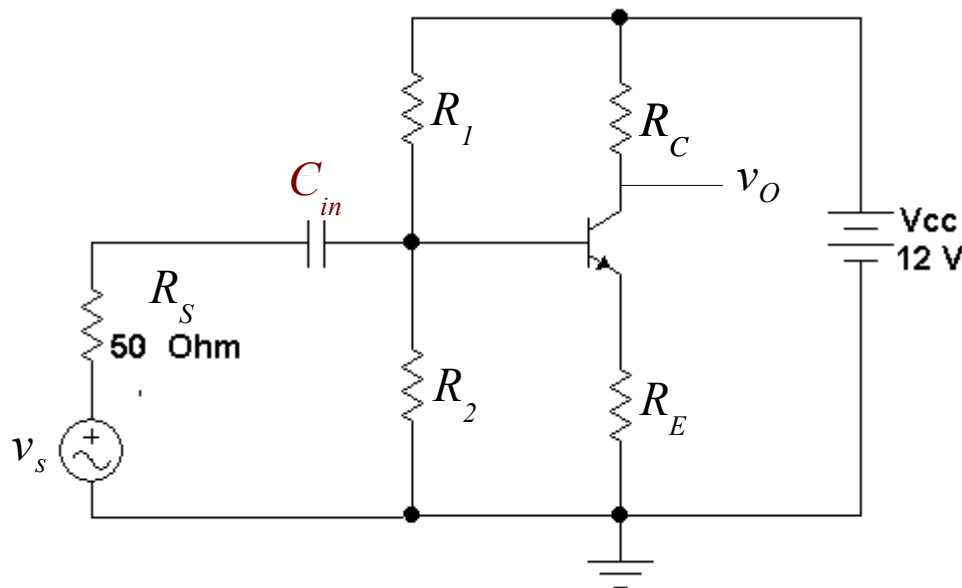
$0 C < T < 40 C \rightarrow$  Requires simulation to verify.

$$|A_V| = \left| \frac{v_{o-max}}{v_{s-max}} \right| \approx 10 \quad @ \text{ midband}$$

More typical gain spec:  
 $9.5 \leq |A_V| \leq 10.5$  or  $10 \pm 5\%$

$$f_{min} = 20 \text{ Hz}$$

## Design Step 1 (Set $R_B$ and $R_E$ )



$$\beta \approx 100$$

Choose an  $R_B \gg 10R_S$ :

$$R_B = 5000 \Omega$$

$(1 + \beta)R_E$  must be  $\geq 10R_B$ :

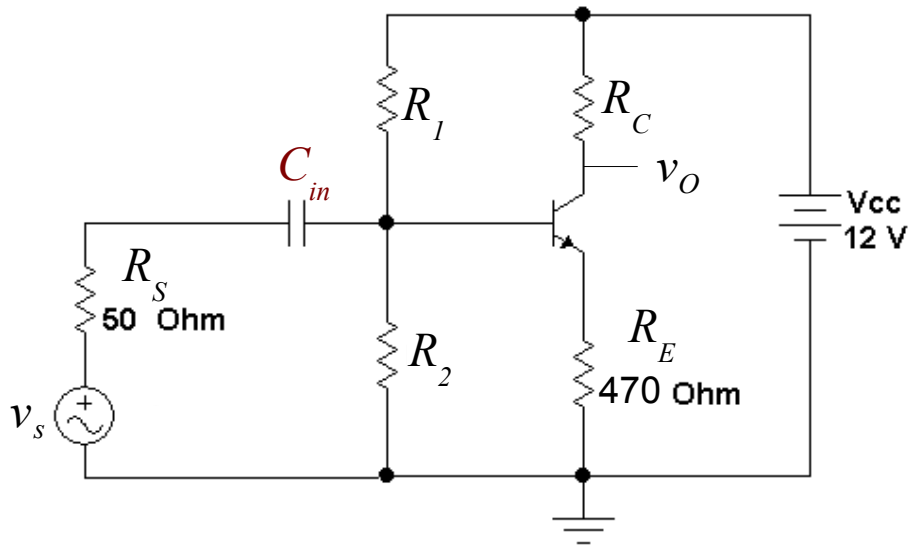
$$R_E = \frac{10 \cdot 5000}{100} = 500 \Omega$$

Nearest standard size\*: 470  $\Omega$

$$R_E = 470 \Omega$$

\*RCA Lab: <http://www.ese.upenn.edu/rca/components/passive/listcomponents.html#resistors>

## Design Step 2 (Set $R_C$ )



$$\beta = 100 \quad R_B = R_1 \parallel R_2 = 5 \text{ k}\Omega$$

$$R_E = 470 \Omega$$

For a gain of about  $-10$ :

$$R_C = 10 R_E = 4.7 \text{ k}\Omega$$

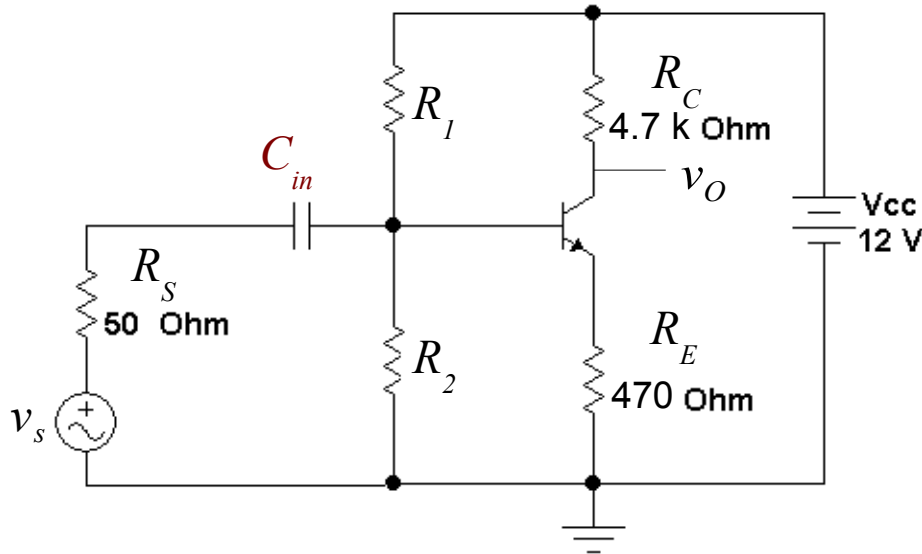
Nearest standard size\*:

$$R_C = 4.7 \text{ k}\Omega$$

SPEC:  $v_{s-max} = 0.1 \text{ V pk}$

For a gain of  $-10$ , the collector voltage  $v_o$  swings to  $1 \text{ V}$  max, so the  $R_C$  drop from dc bias could “in principle” be as little as  $1 \text{ V}$ .

## Design Step 3 (Set bias point neglecting $I_B$ )



$$\beta = 100 \quad R_B = 5 \text{ k} \Omega$$

$$R_E = 470 \Omega \quad R_C = 4.7 \text{ k} \Omega$$

Recall  $v_{sig-max} = 0.1 \text{ V pk}$

We have plenty of room - choose the collector drop conservatively to allow for bias point changes with temperature - let's use:

$$V_{R_C} = 4.7 \text{ V} \approx \frac{V_{CC}}{3}$$

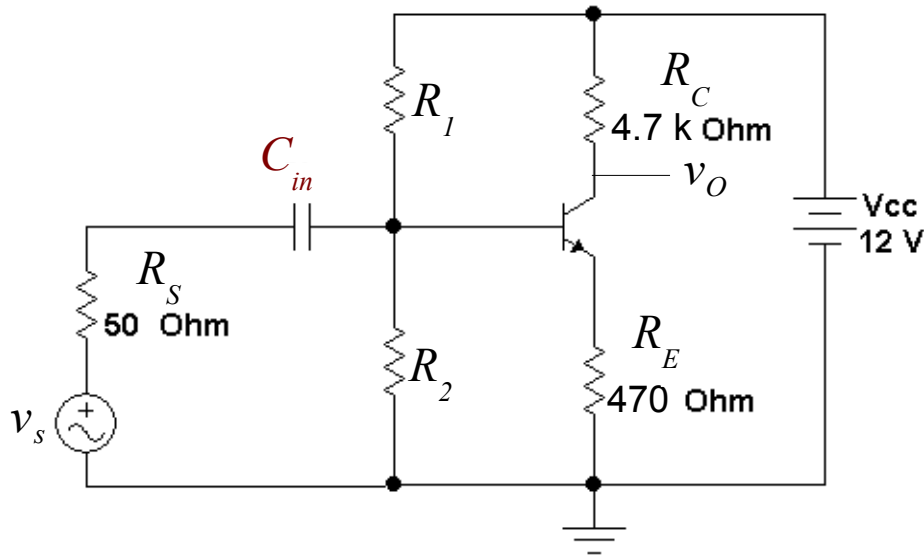
Thus:

$$I_C = 4.7 / 4700 = 1 \text{ mA} \Rightarrow g_m = 40 \text{ mS}$$

And (ignoring  $I_B$ ):

$$V_B \approx I_C R_E + 0.7 = 0.47 + 0.7 = 1.17 \text{ V}$$

## Design Step 4 (Set $R_1$ and $R_2$ )



$$\beta = 100 \quad R_B = 5 \text{ k} \Omega$$

$$R_E = 470 \Omega \quad R_C = 4.7 \text{ k} \Omega$$

Recall:

$$R_B = R_1 \parallel R_2 = R_1 \frac{R_2}{R_1 + R_2} = 5 \text{ k} \Omega$$

And:

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = 1.17 \text{ V}$$

Or:

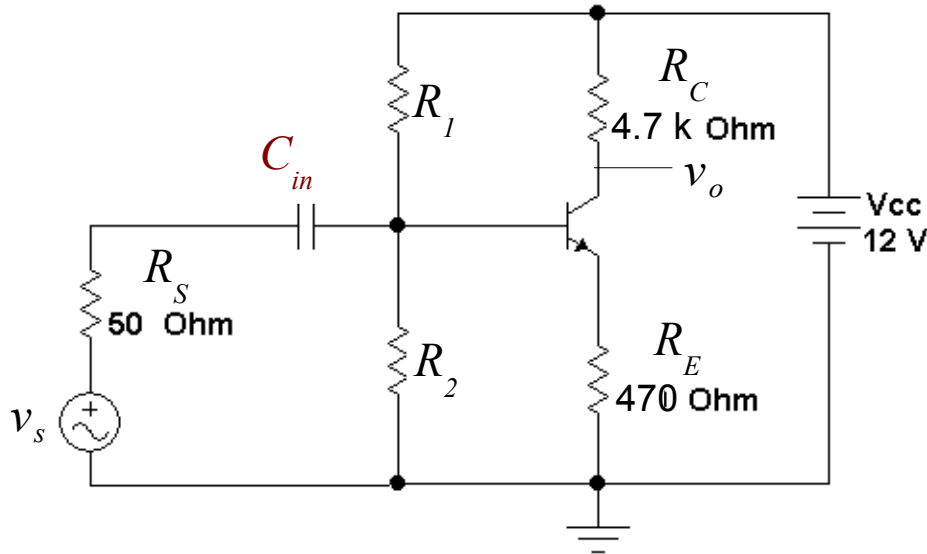
$$\frac{R_2}{R_1 + R_2} = \frac{V_B}{V_{CC}} = \frac{1.17}{12} = 0.098 \approx 0.1$$

## Design Step 4 cont. (Set $R_1$ and $R_2$ )

Substituting:

$$R_1 \parallel R_2 = R_1 \frac{R_2}{R_1 + R_2} = R_1 \cdot 0.1 = 5 \text{ k} \Omega$$

$$R_1 = 50 \text{ k} \Omega$$



$$\beta = 100 \quad R_B = 4.6 \text{ k} \Omega$$

$$R_E = 470 \Omega \quad R_C = 4.7 \text{ k} \Omega$$

**NOTE:**  $(1 + \beta) R_E \approx 47 \text{ k} \Omega \geq 10 R_B = 46 \text{ k} \Omega$

Standard size:

$$R_1 = 47 \text{ k} \Omega$$

Finally:

$$\frac{R_2}{47 \text{ k} + R_2} = 0.1$$

$$0.9 R_2 = 0.1 (47 \text{ k}) \Rightarrow R_2 = 5222 \Omega$$

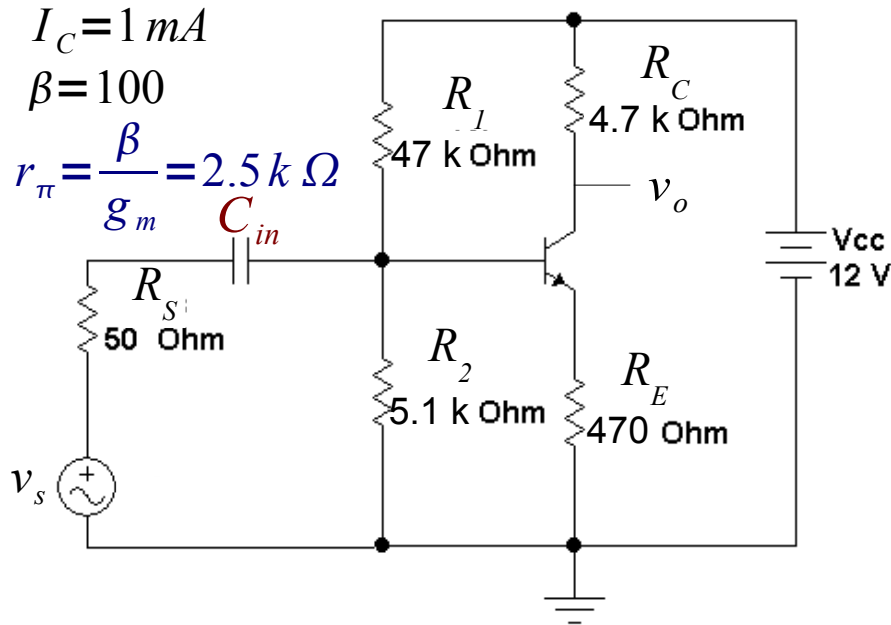
Standard size:

$$R_2 = 5.1 \text{ k} \Omega$$

Revised  $R_B$ :

$$R_B = R_1 \parallel R_2 = \frac{(47 \text{ k}) 5.1 \text{ k}}{52.1 \text{ k}} = 4.6 \text{ k} \Omega$$

## Design Step 5 (set $C_{in}$ ) - Close to the Finish!



$$I_C = 1 \text{ mA}$$

$$\beta = 100$$

$$r_{\pi} = \frac{\beta}{g_m} = 2.5 \text{ k}\Omega$$

$R_B$  in parallel with  $r_{bg} \Rightarrow R_B$  dominates.  
 Estimate  $R_B || r_{bg} \approx R_B = 4.6 \text{ k}\Omega$ . Coupling capacitor reactance, then, should be about  $460 \Omega$  at  $f = f_{min}$ .

$$\left| \frac{1}{j 2 \pi f_{min} C_{in}} \right| = 460 \Omega \quad C_{in} = \frac{1}{2 \pi f_{min} 460 \Omega}$$

$$C_{in} = \frac{1}{460 \cdot 2 \pi 20} = \frac{1.09 \cdot 10^{-4}}{2 \pi} \approx 17 \mu F$$

Estimate  $R_{in}$ :

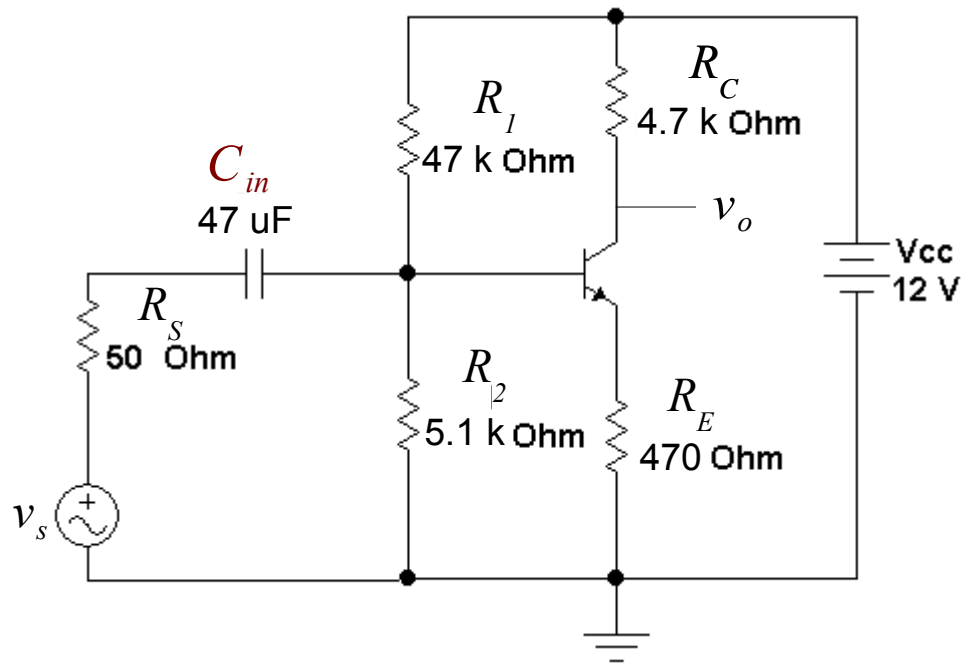
$$r_{bg} = r_{\pi} + (\beta + 1) R_E = 50 \text{ k}\Omega$$

$$R_B || r_{bg} = 4.2 \text{ k}\Omega$$

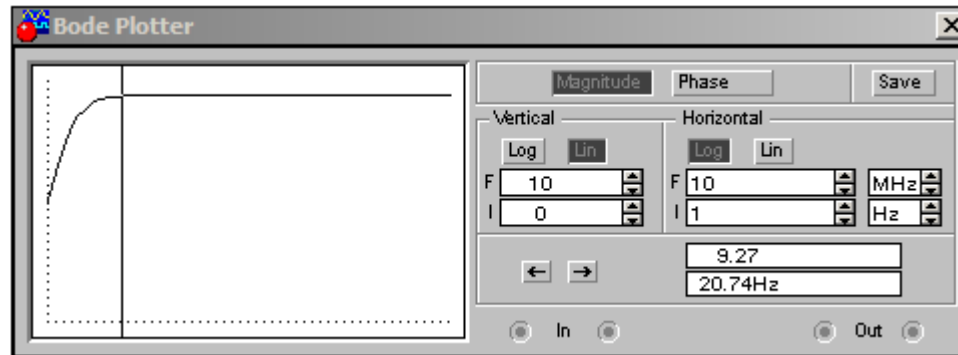
Using the RCA Lab Component List

$$C_{in} = 47 \mu F$$

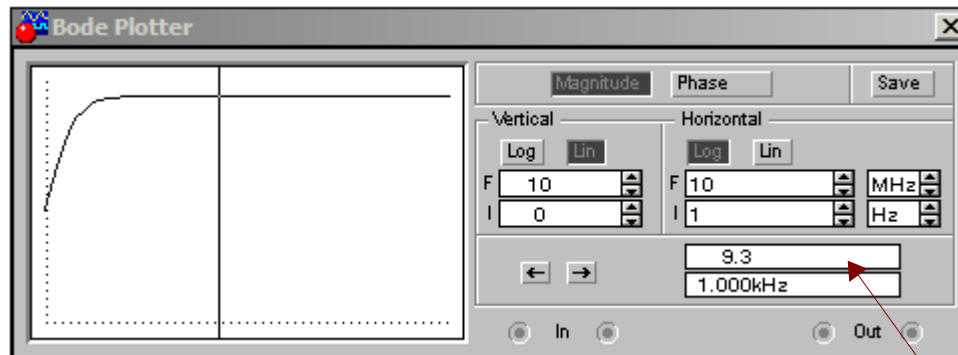
## Final Design



## Multisim Simulation



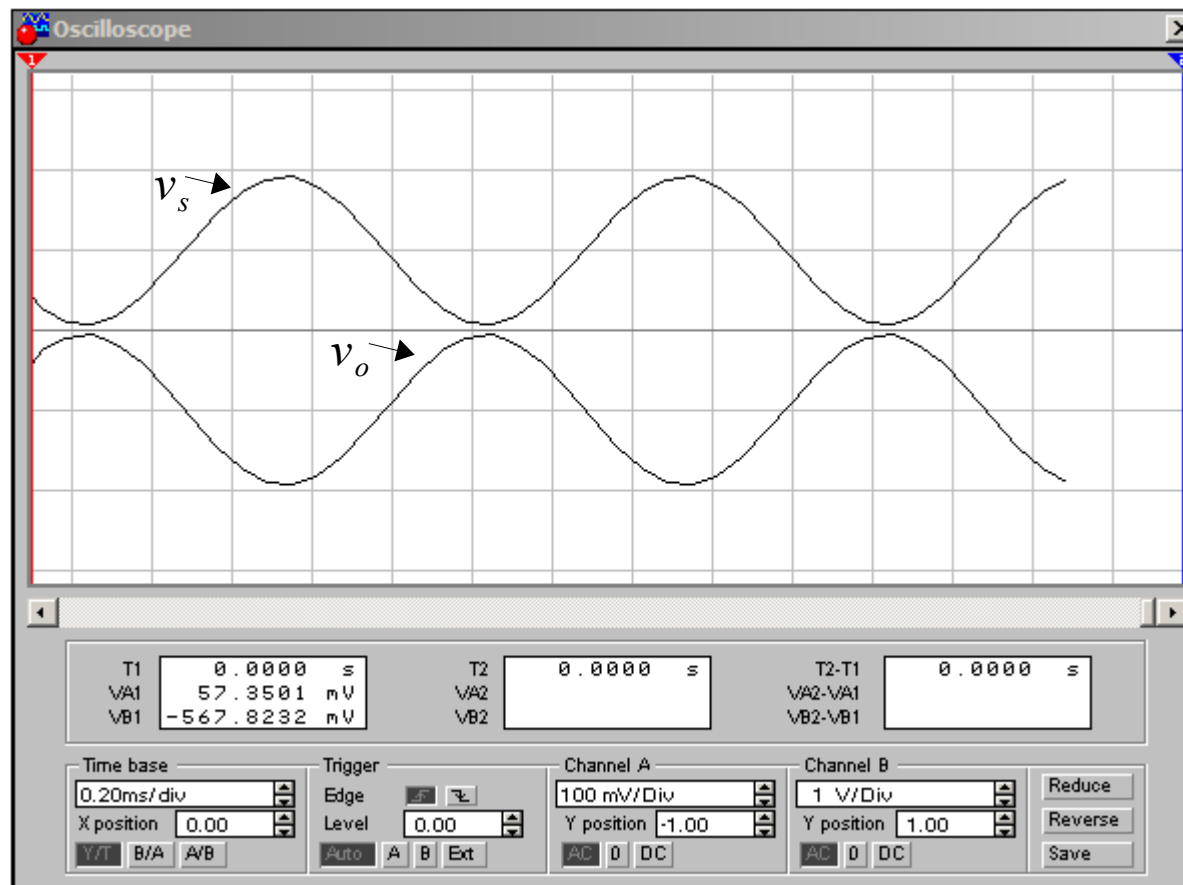
20 Hz Gain



1 Khz Gain

Actual  $|A_V| = 9.3 < 10$

## *Multisim Oscilloscope Plots*



## Discussion

1. We neglected  $r_e$ . Including the internal emitter resistance, the simulated gain becomes:

$$A_V = -\frac{R_C}{R_E + r_e} = -\frac{4700}{470 + 25} = -9.5$$

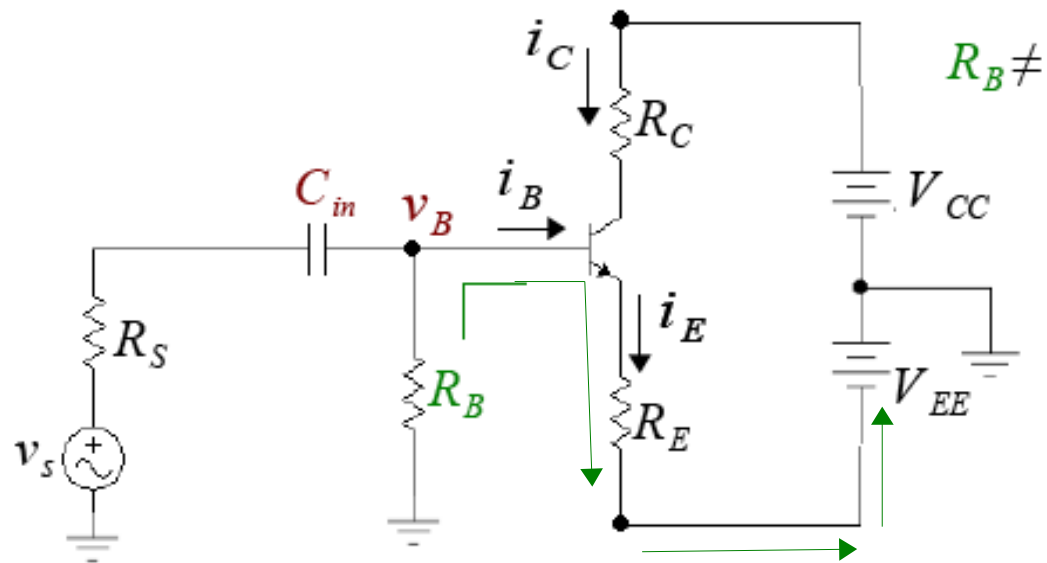
2. There is some attenuation of the signal voltage at the base. A more accurate calculation of the input attenuation:

$$R_B \parallel r_{bg} = 4.2 \text{ k}\Omega \Rightarrow v_{bg} \approx \frac{R_B \parallel r_{bg}}{R_B \parallel r_{rg} + R_S} v_{sig} = \frac{4200}{4250} v_{sig} = 0.988 v_{sig}$$

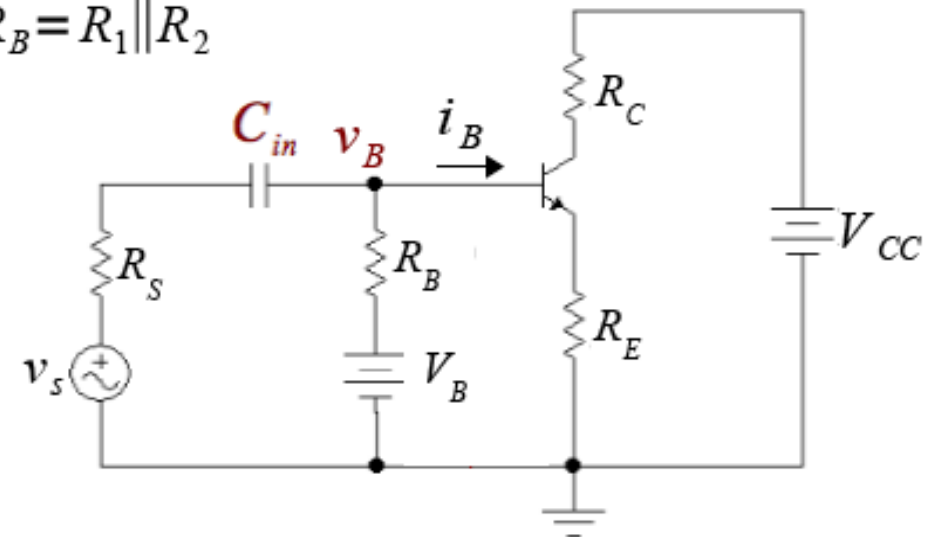
Multiplying the two quantities:  $A_v = -9.5 \cdot 0.988 = -9.4$  **Close to 9.3!**

This fine-tuning of the estimate may not be all that helpful – since we will be using 5% components to build the circuit!

## Alternative Two Supply Biasing Scheme



$$R_B \neq R_B = R_1 \parallel R_2$$



$$-I_B R_B = V_{BE} + I_E R_E - V_{EE}$$

$$-I_B R_B = V_{BE} + (\beta + 1) I_B R_E - V_{EE}$$

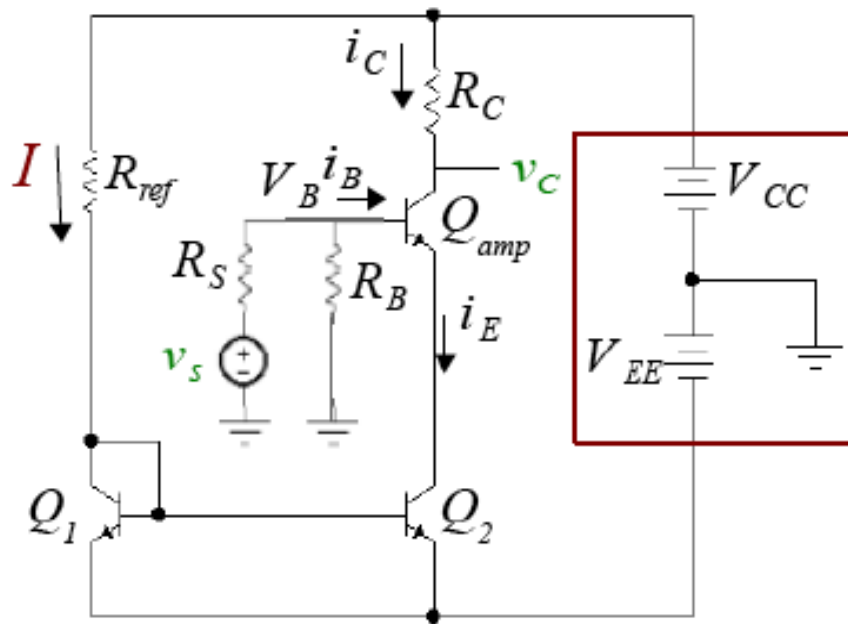
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$R_B \ll (\beta + 1) R_E \quad V_{EE} \gg V_{BE}$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$R_B \ll (\beta + 1) R_E \quad V_B \gg V_{BE}$$

## Common Emitter Amplifier - Current Source Biasing



$$v_c = -i_c R_C + V_{CC}$$

1. The current mirror sets  $I_E (I_C)$ .

2.  $R_B$  serves the purpose to provide a high impedance looking into the base and  $I_B = I_E / (\beta + 1)$  and  $V_B = -I_B R_B$ .

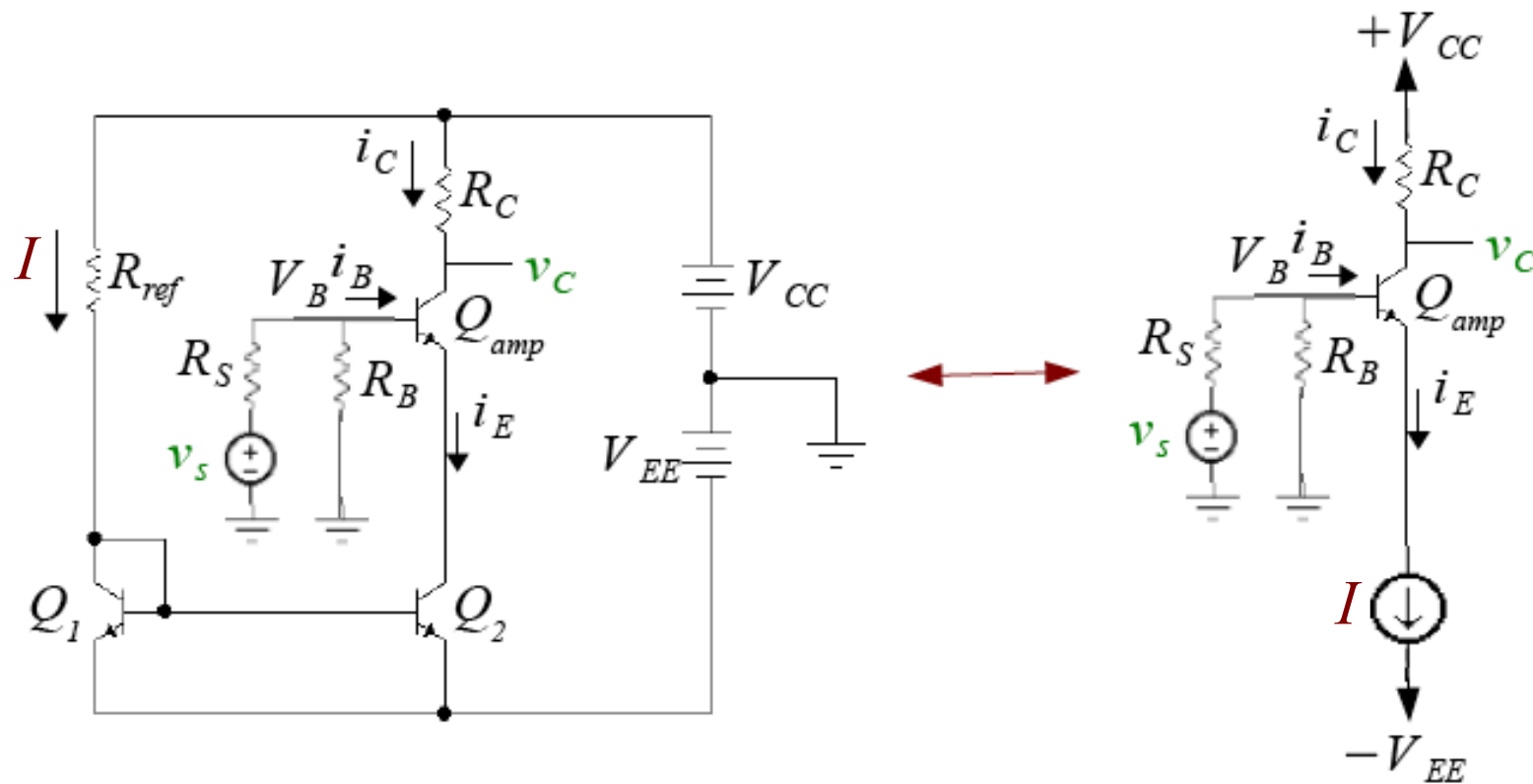
3. We want to limit  $V_B$  to enable a larger  $v_o$  signal swing, i.e. maintain fwd. act.

$$v_{BC} = V_B - v_C < 0.7V \Rightarrow$$

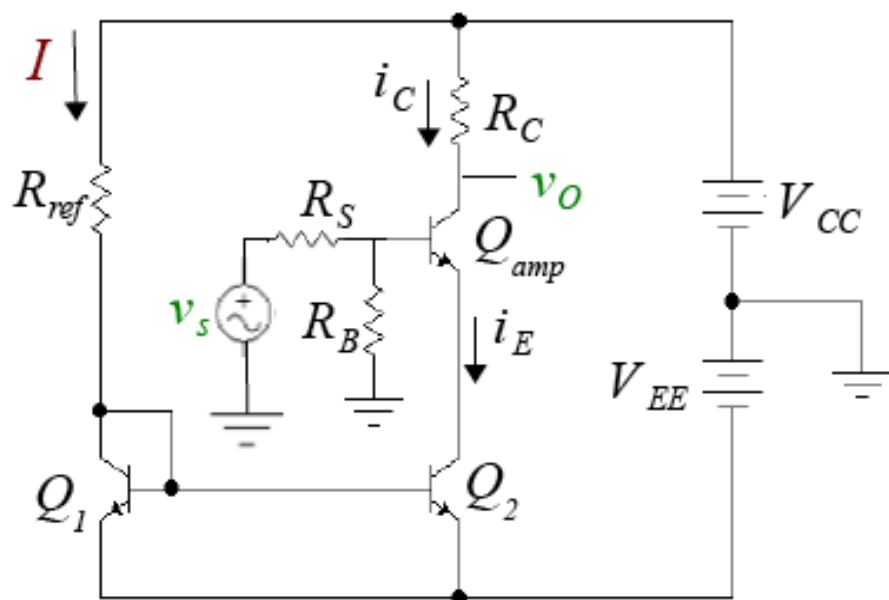
$$v_C = V_C + v_c > -0.7V + V_B$$

4.  $v_s$  is the signal source.

## Schematic Representations

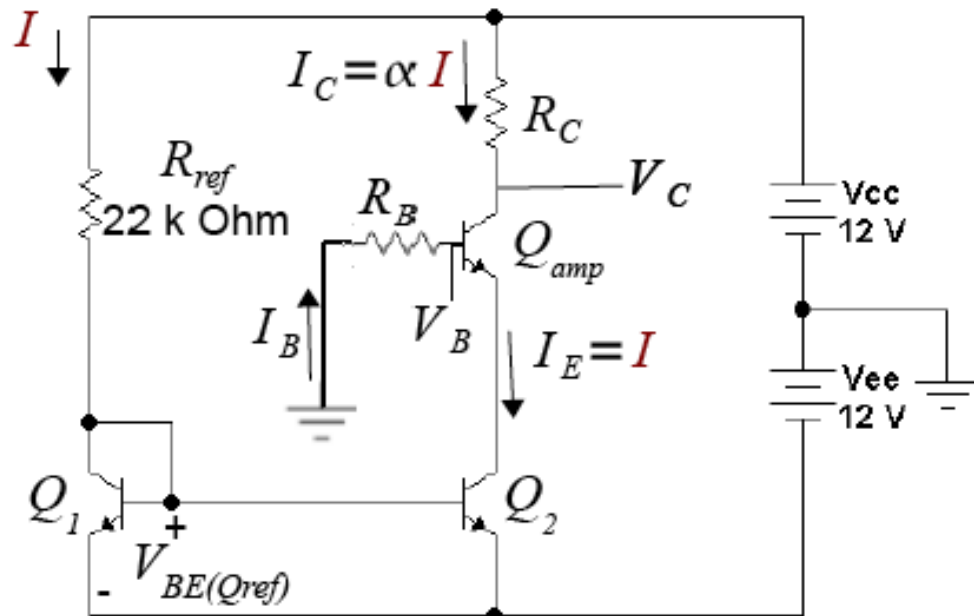


## Bias Setting



1. Since  $R_B$  does not interfere with the bias, the signal source can “usually” be connected to the base without need for a blocking capacitor.
2. Choose  $R_B$  “large” compared to  $R_S$  to avoid attenuating  $v_s$ .
3. Choose  $R_{ref}$  to set  $I_E = I$ .

## Bias Setting - Continued



For dc bias set  $v_s = 0$

Choose:

$$I_C \approx I_E \approx I = 1 \text{ mA}$$

$$I_B \approx I / (1 + \beta)$$

$$V_{CC} = I R_{ref} + V_{BE(Q_{ref})} - V_{EE}$$

$$I = \frac{V_{CC} + V_{EE} - 0.7}{R_{ref}}$$

$$R_{ref} = \frac{23.3}{10^{-3}} = 23.3 \text{ k} \Omega$$

Choose standard size:  
(Detkin Lab Comp List)

$$R_{ref} = 22 \text{ k} \Omega$$

## Bias Setting - Completed

With the base  $I_B \approx 0$  through  $R_B$ :

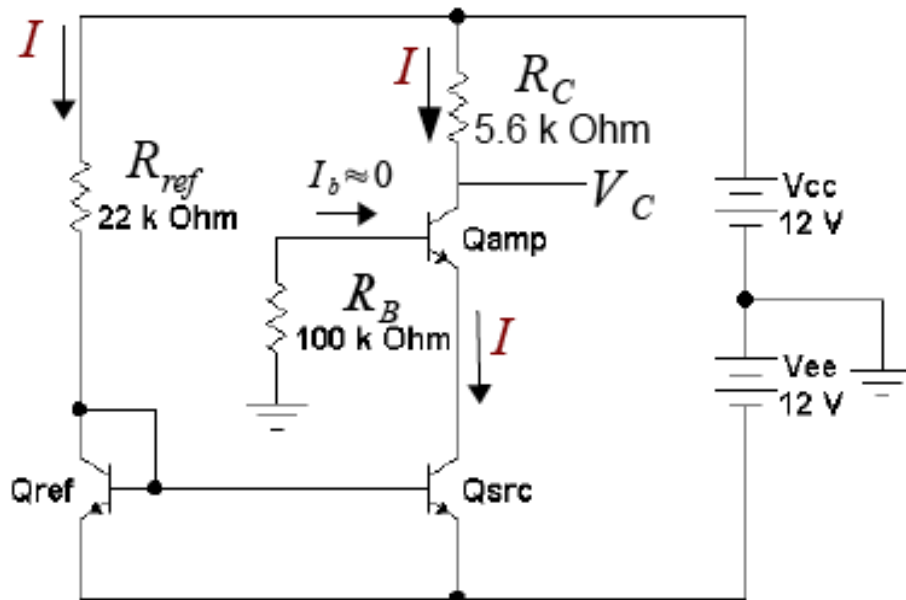
$$V_C = -I R_C + V_{CC}$$

This implies that there is about a 12 V drop to split across  $R_C$  and  $V_{CB}$ . Choose 6 V each.

$$R_C = \frac{V_C}{I} = \frac{6}{10^{-3}} = 6 \text{ k}\Omega$$

Choose standard size:  
(Detkin Lab Comp List)

$$R_C = 5.6 \text{ k}\Omega$$

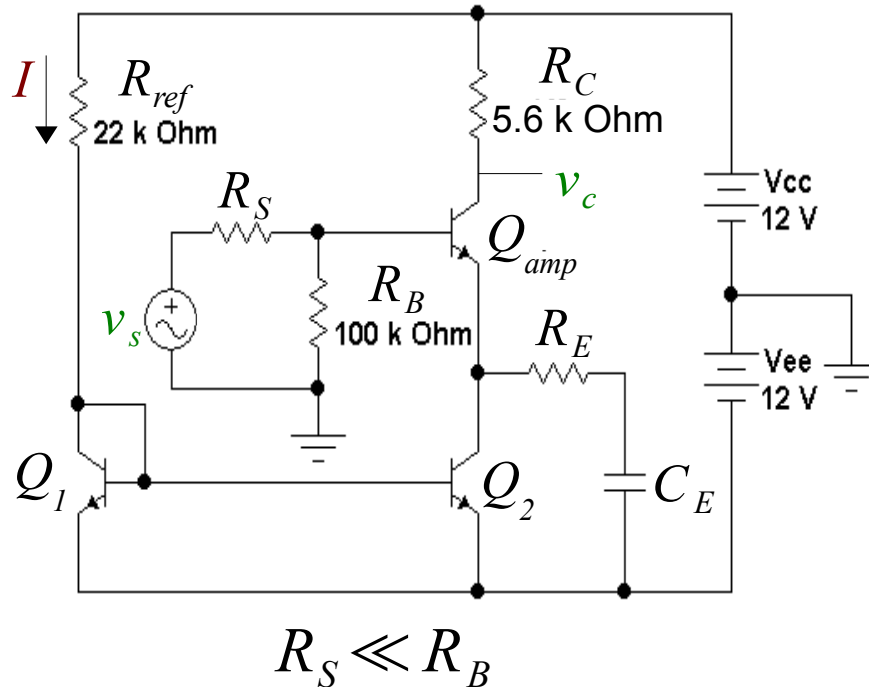


Neglect the base current through  $R_B$

$$I_C = I_E = I = 1 \text{ mA}$$

$$I_B = 0$$

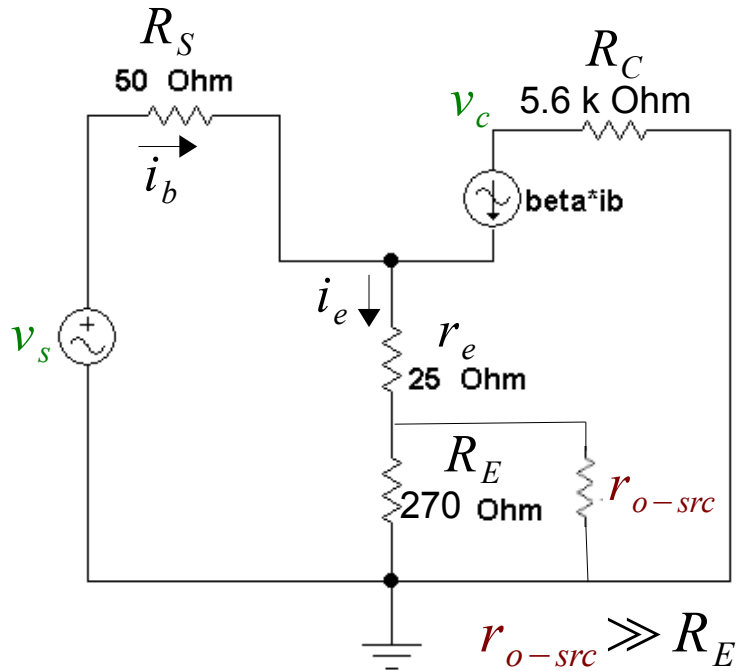
## Gain Setting



1. Connect the source to the base.  
 $C_{in}$  not needed iff  $v_s$  is ac only.
2. Provide  $R_E$  path for the small-signal emitter current.
3. Choose  $R_E$  for the desired gain ( $A_v = -R_C/R_E$ ).
4.  $C_E$  is nearly a short circuit for  $f \geq f_{min}$

Calculate  $C_E$  s.t.  $\left| \frac{1}{j2\pi f C_E} \right| \ll R_E$   
at  $f \geq f_{min}$ .

## Gain Setting - Continued



Design for  $|A_V| = 20$ : Typical  
 $18 \leq |A_V| \leq 22$

Choose the nearest standard size resistors for  $R_C$  and  $R_E$ .

$$R_E = \frac{R_C}{20} = \frac{5600}{20} \approx 270 \Omega$$

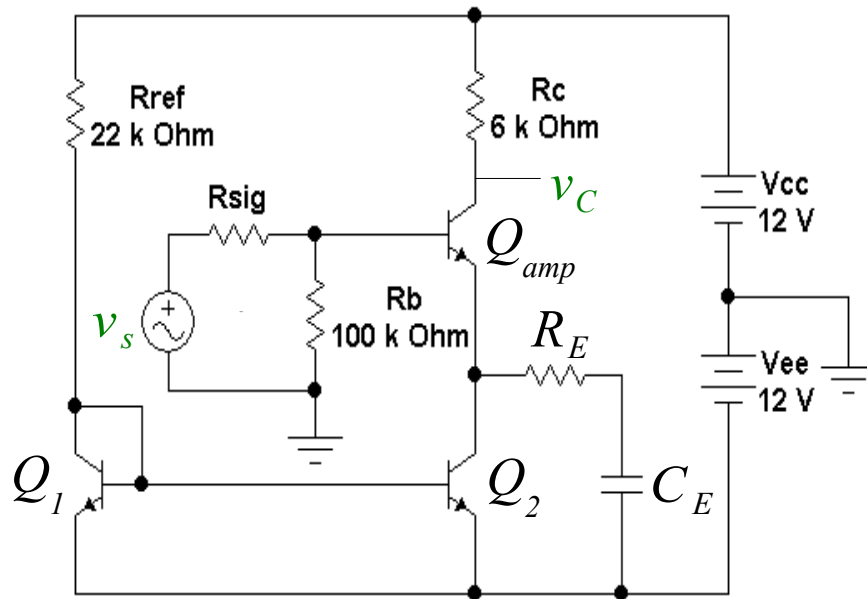
Gain check:

$$i_b = \frac{v_s}{R_S + (\beta + 1)(r_e + R_E)}$$

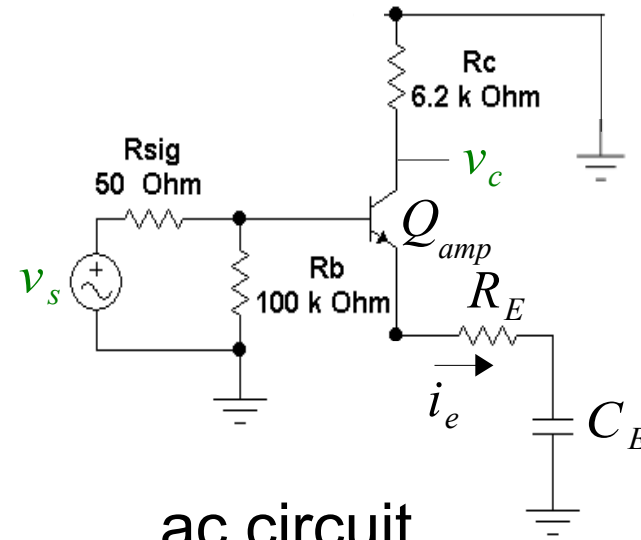
$$v_c = -R_C i_c = -R_C \beta i_b$$

$$|A_V| = \left| \frac{v_c}{v_s} \right| \approx \frac{\beta}{\beta + 1} \frac{R_C}{r_e + R_E} \approx \frac{5600}{295} = 19 \text{ or } 25.57 \text{ dB}$$

## $R_E$ and $C_E$



overall circuit with bias



ac circuit

$$\left| \frac{1}{j2\pi f C_E} \right| \ll R_E \Rightarrow \frac{1}{2\pi f_{min} C_E} = \frac{R_E}{10} \Rightarrow C_E = \frac{10}{2\pi f_{min} R_E} \approx 300 \mu F \quad @ f_{min} = 20 \text{ Hz}$$

$C_E = 300 \mu F$  too conservative!

## Complete the Design

$$\left| \frac{1}{j2\pi f C_E} \right| \ll R_E \Rightarrow \frac{1}{2\pi f_{min} C_E} = \frac{R_E}{10} \Rightarrow C_E = \frac{10}{2\pi f_{min} R_E} \approx 300 \mu F \quad @ f_{min} = 20 \text{ Hz}$$

$C_E = 300 \mu F$  too large!

Less Conservative Design:

$$C_E = \frac{1}{2\pi f_{min} R_E} \quad \text{where} \quad f_{min} \approx f_{-3dB}$$

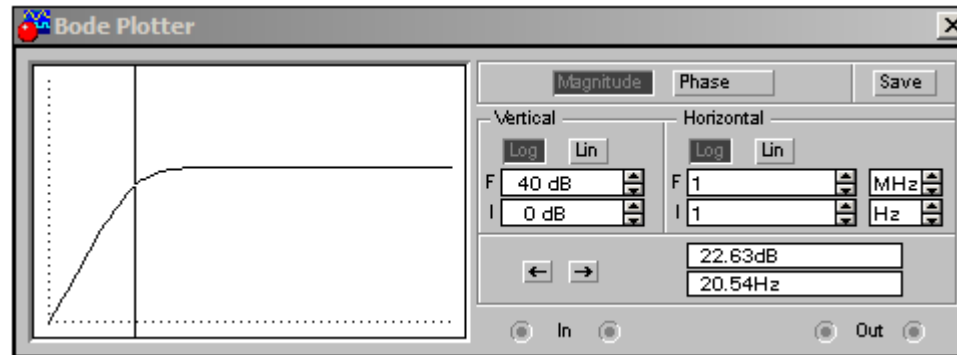
$$C_E = \frac{1}{2\pi f_{min} R_E} \approx 30 \mu F \quad \text{for} \quad f_{min} = 20 \text{ Hz}$$

If we choose standard size (RCA Lab Comp List):

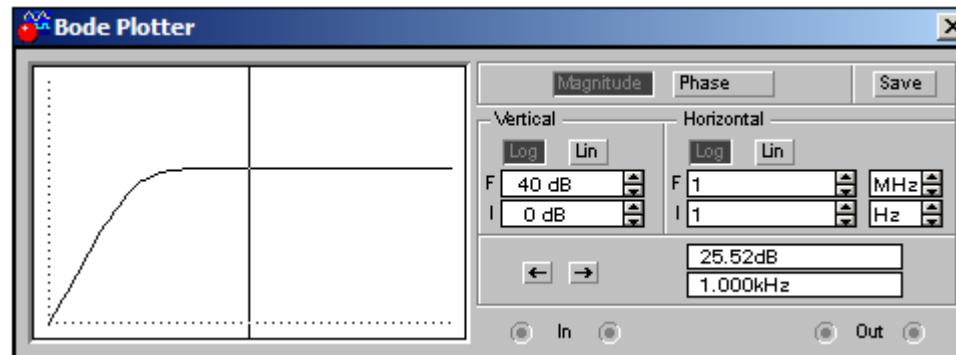
$$\boxed{C_E = 47 \mu F} \Rightarrow f_{-3dB} = 11.5 \text{ Hz}$$

## Multisim Bode Plots

$$C_E = 30 \mu F$$



20 Hz. Gain



1 kHz. Gain