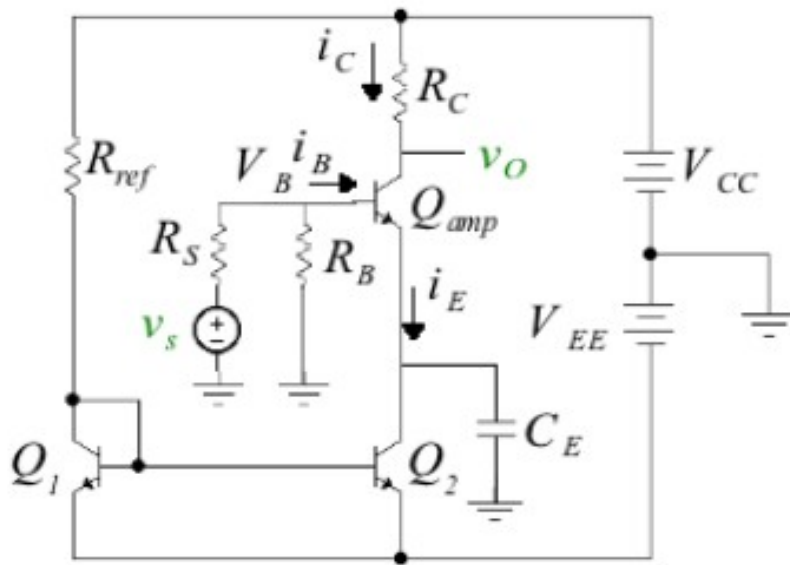
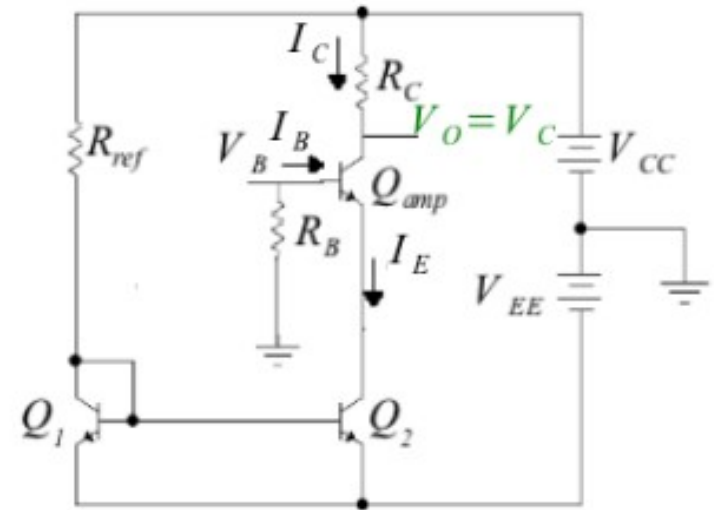


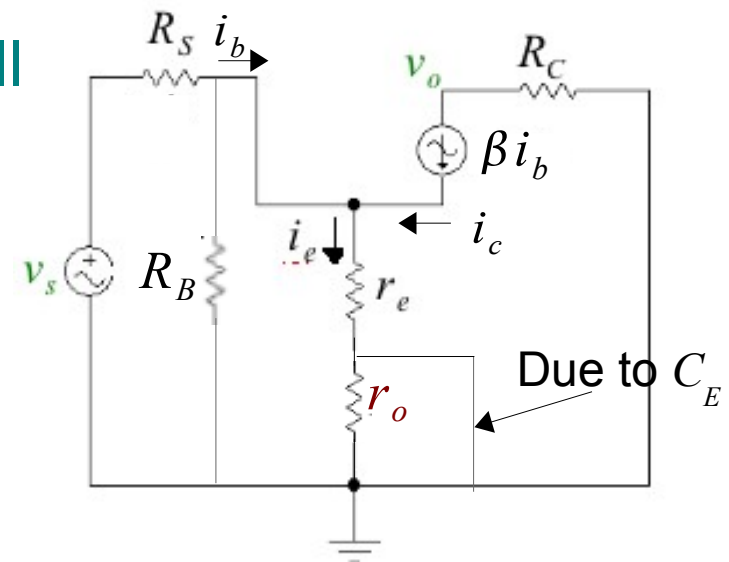
Quick Review



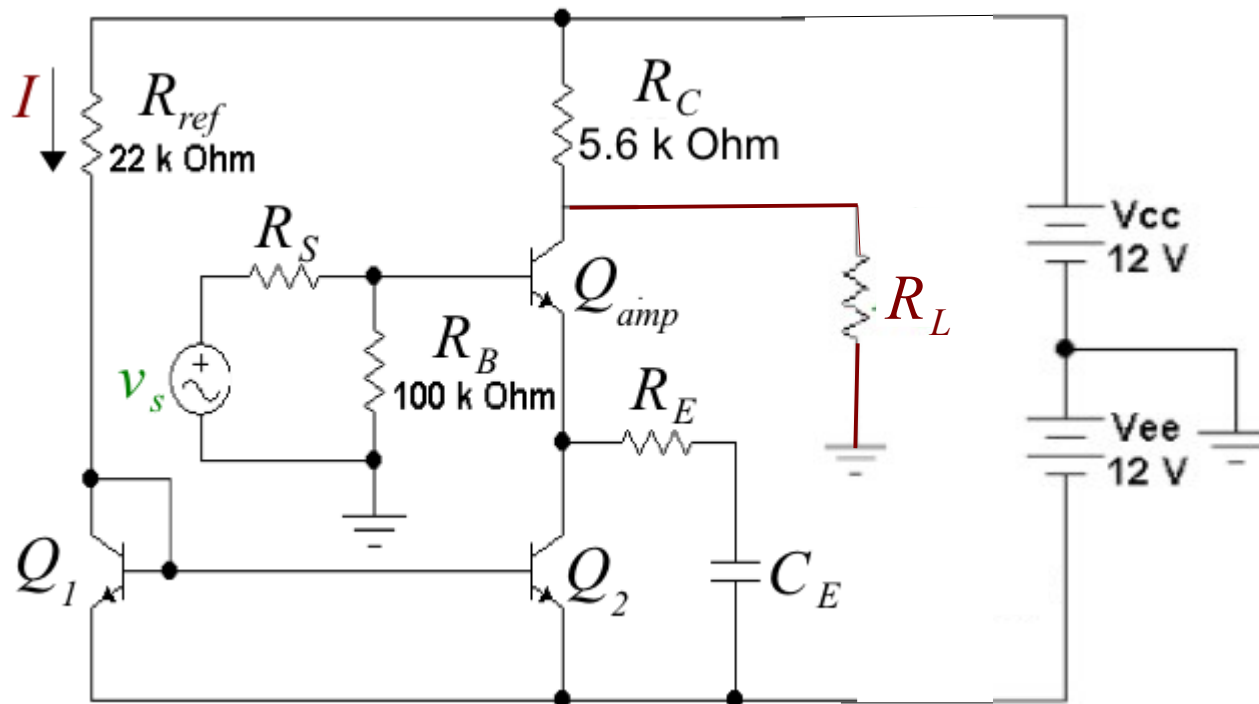
dc



small
ac

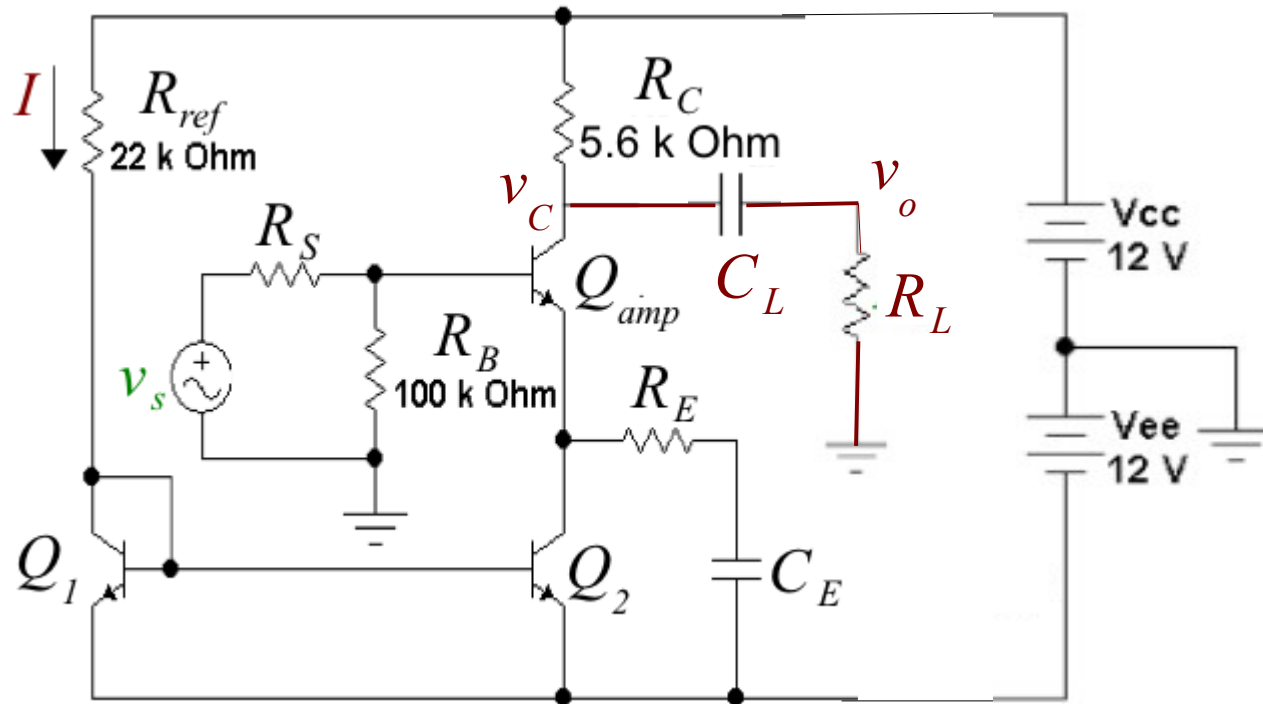


What About Interface to the Output Load (R_L)?



Is the above interface to R_L OK?

What About Interface to the Output Load (R_L)?

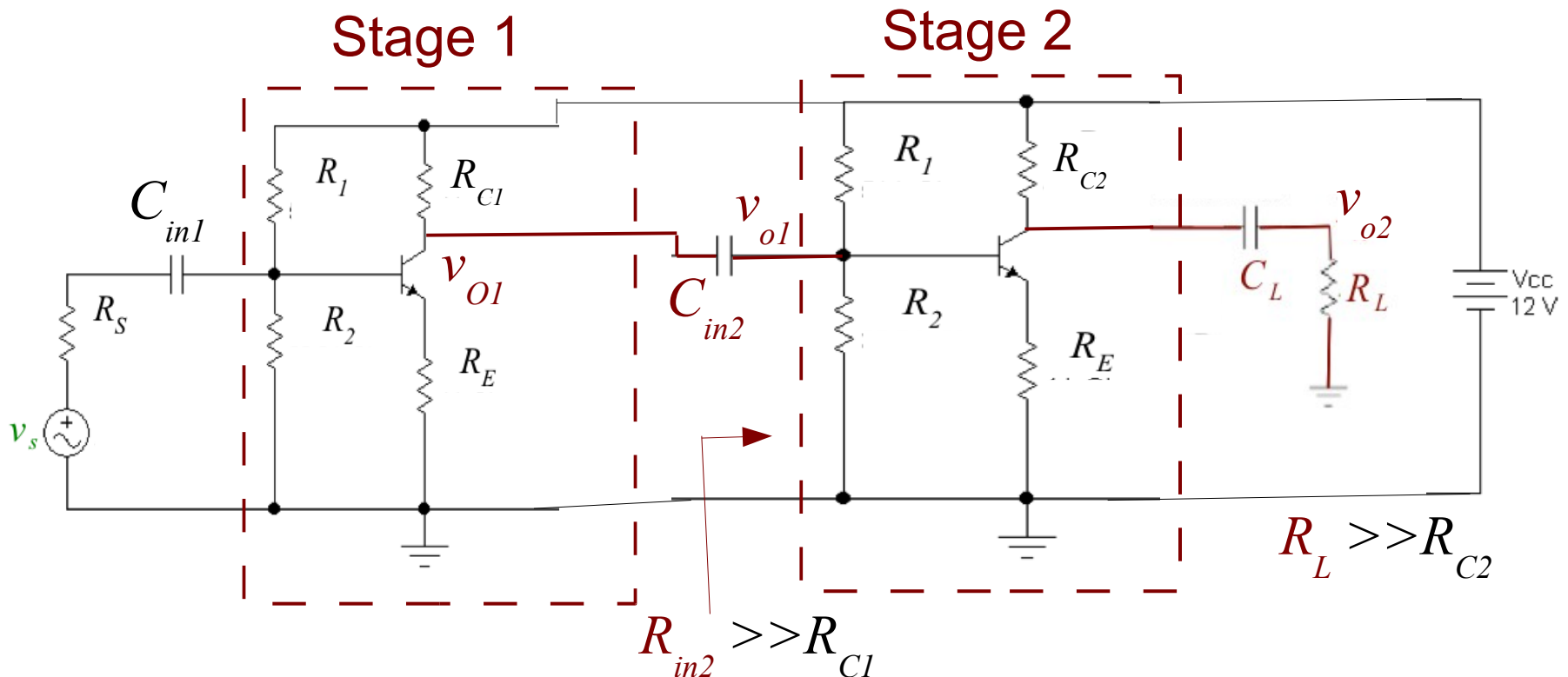


Is the above interface to R_L OK? - No

1. Need C_L to block dc bias on v_C , i.e. v_o is small signal only.

2. For ac ($f \geq f_{min}$) $R'_L = R_C \parallel R_L \Rightarrow R_L \gg R_C$

Multi-Stage Amplifier



$$A_v = \left(\frac{v_{o1}}{v_s} \right) \left(\frac{v_{o2}}{v_{o1}} \right) = \frac{v_{o2}}{v_s} = \left(-\frac{R_{C1}}{R_E} \right) \left(-\frac{R_{C2}}{R_E} \right)$$

Common Base BJT Amplifier

Common Collector BJT Amplifier

- Common Collector (Emitter Follower) Configuration
- Common Base Configuration
- Small Signal Analysis
- Design Example
- Amplifier Input and Output Impedances

Basic Single BJT Amplifier Features

	<u>CE Amplifier</u>	<u>CC Amplifier</u>	<u>CB Amplifier</u>
Voltage Gain (A_V)	moderate ($-R_C/R_E$)	low (about 1)	high
Current Gain (A_I)	moderate (β)	moderate ($\beta + 1$)	low (about 1)
Input Resistance	high	high	low
Output Resistance	high	low	high

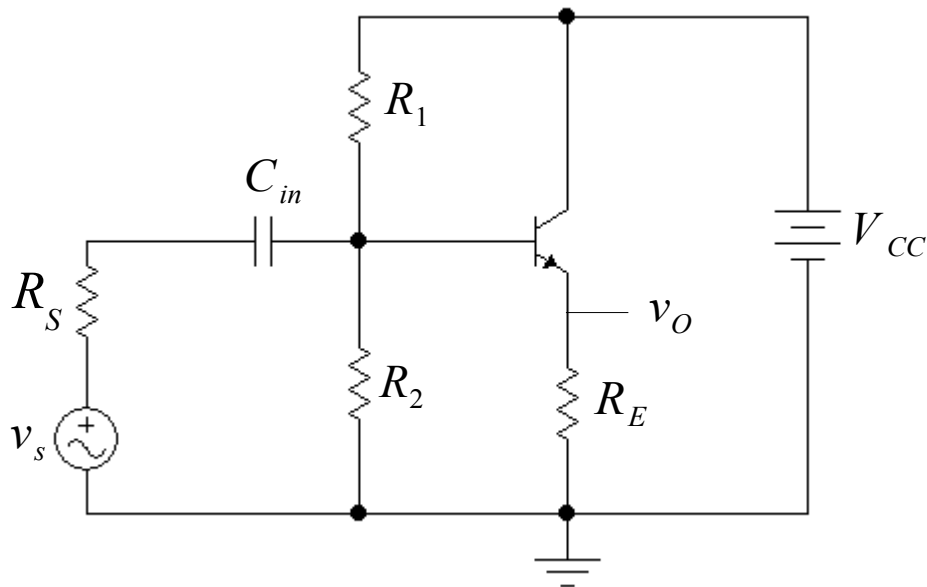
VCVS
CCCS

CE BJT amplifier => CS MOS amplifier

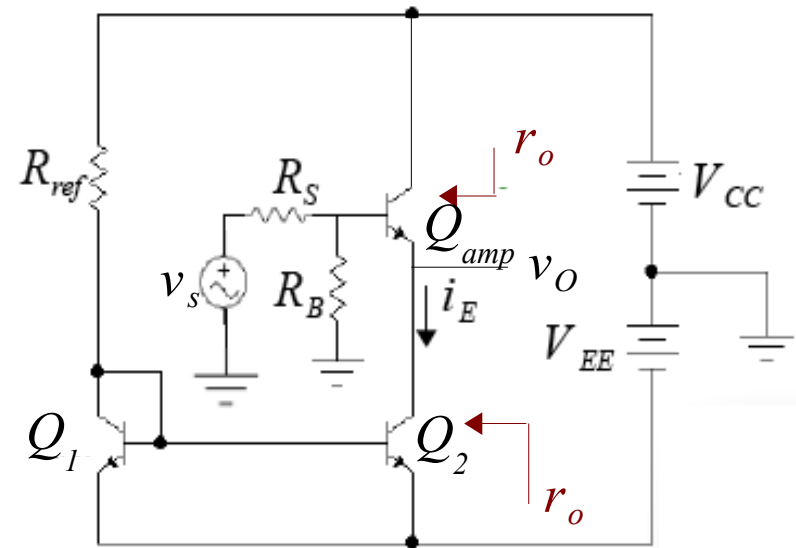
CC BJT amplifier => CD MOS amplifier

CB BJT amplifier => CG MOS amplifier

Common Collector (Emitter Follower) Amplifier



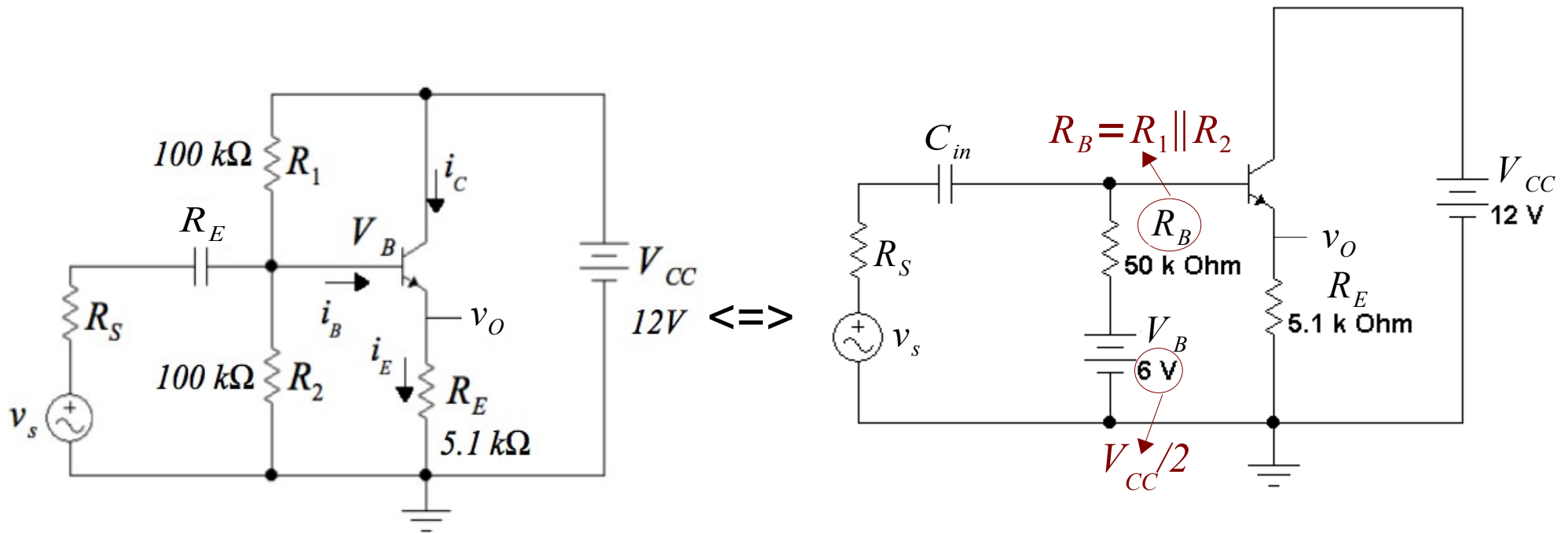
Voltage Bias Design



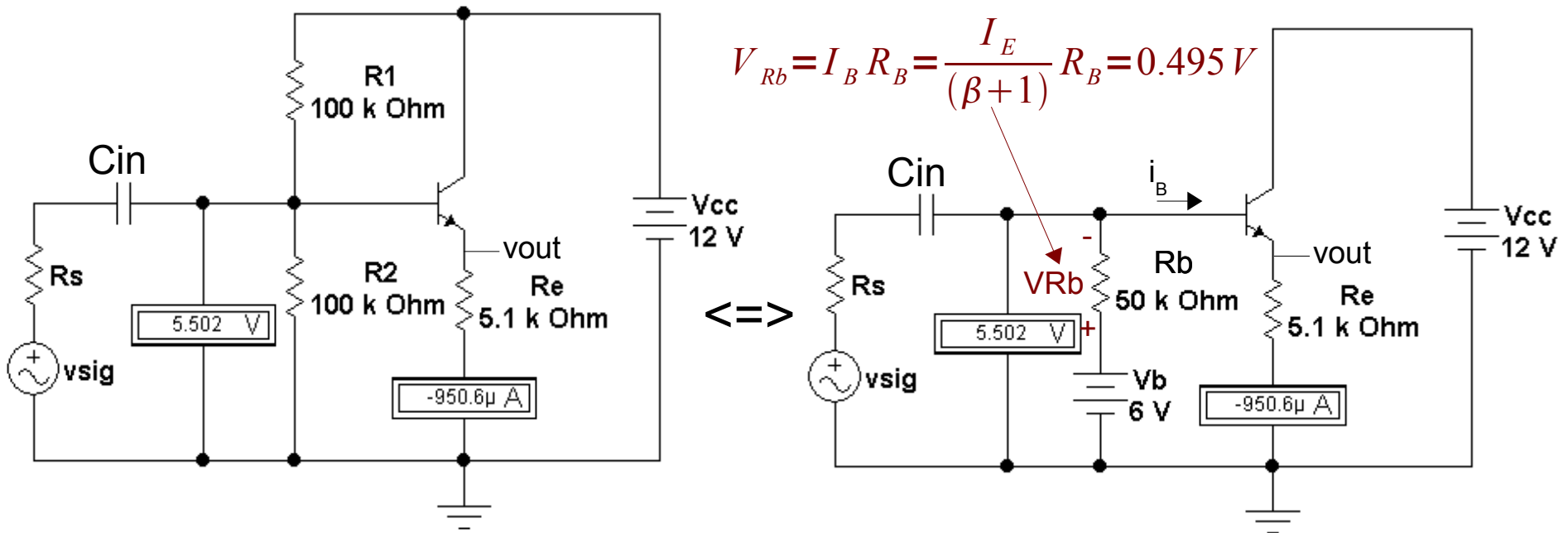
Current Bias Design

In the emitter follower, the output voltage is taken between emitter and ground. The voltage gain of this amplifier is nearly one – the output “follows” the input - hence the name: emitter “follower.”

Equivalent Circuits



Multisim Bias Check



Identical results – as expected!

Follower Small Signal Analysis - Voltage Gain

Circuit analysis:

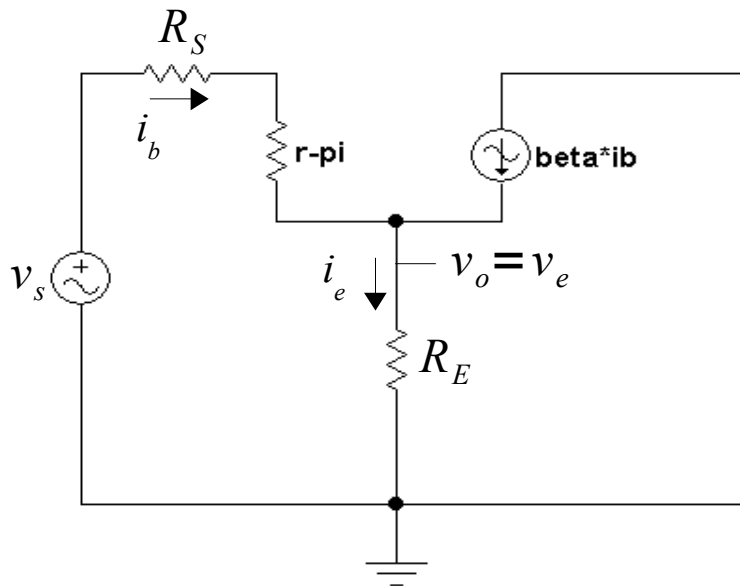
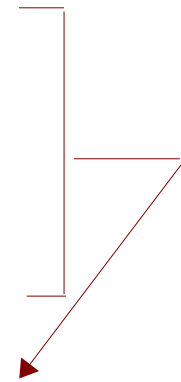
$$v_s = (R_S + r_\pi) i_b + R_E i_e = (R_S + r_\pi + (\beta + 1) R_E) i_b$$

Solving for i_b

$$i_b = \frac{v_s}{R_S + r_\pi + (\beta + 1) R_E}$$

$$v_o = R_E i_e = R_E (1 + \beta) i_b$$

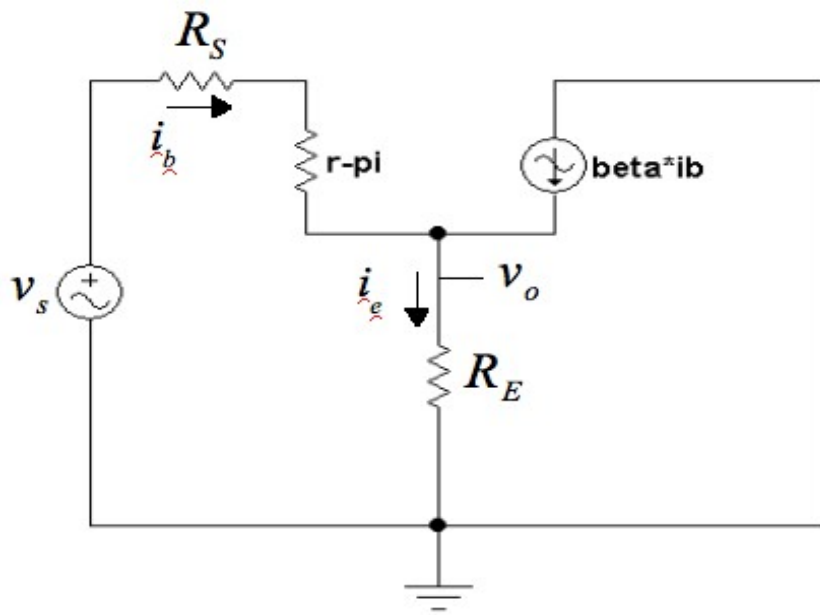
$$v_o = \frac{R_E (\beta + 1) v_s}{R_S + r_\pi + (\beta + 1) R_E}$$



for Current Bias Design
replace R_E with $r_o \parallel r_o = r_o/2 \gg R_E$

$$A_V = \frac{v_o}{v_s} = \frac{R_E \parallel r_o \parallel r_o}{\frac{R_S + r_\pi}{\beta + 1} + R_E \parallel r_o \parallel r_o} \approx 1$$

Small Signal Analysis – Voltage Gain - cont.



$$\frac{v_o}{v_s} = \frac{R_E}{\frac{R_S + r_{\pi}}{(\beta + 1)} + R_E}$$

Since, typically:

$$\frac{R_S + r_{\pi}}{(\beta + 1)} \ll R_E \quad (\text{or } r_o \parallel r_o = r_o/2)$$

$$A_V = \frac{v_o}{v_s} \approx \frac{R_E}{R_E} = 1$$

Note: A_V is non-inverting

Quick Review

CE Amplifier

CC Amplifier

CB Amplifier

Voltage Gain (A_V)

Current Gain (A_I)

Input Resistance

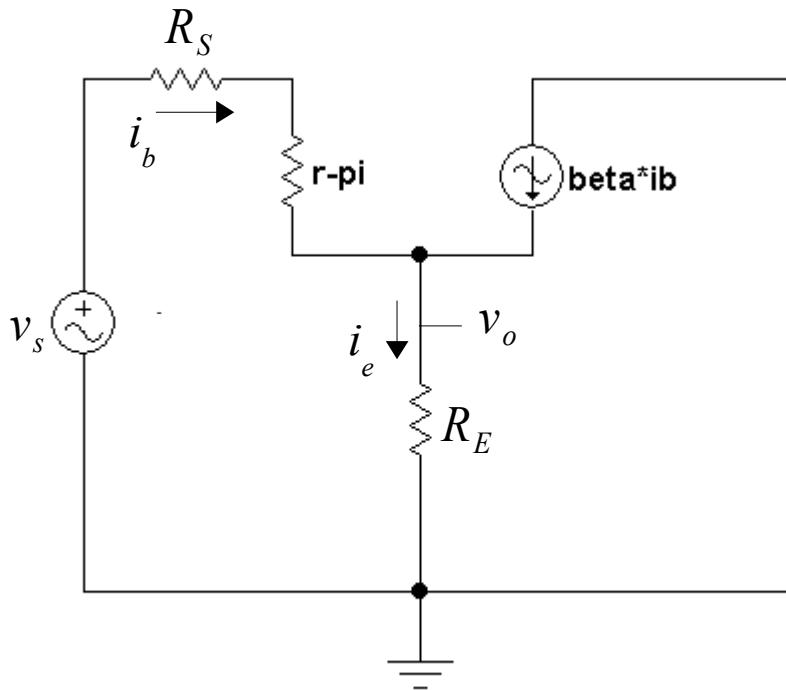
Output Resistance

ANSWERS: Low, Moderate or High

Quick Review cont.

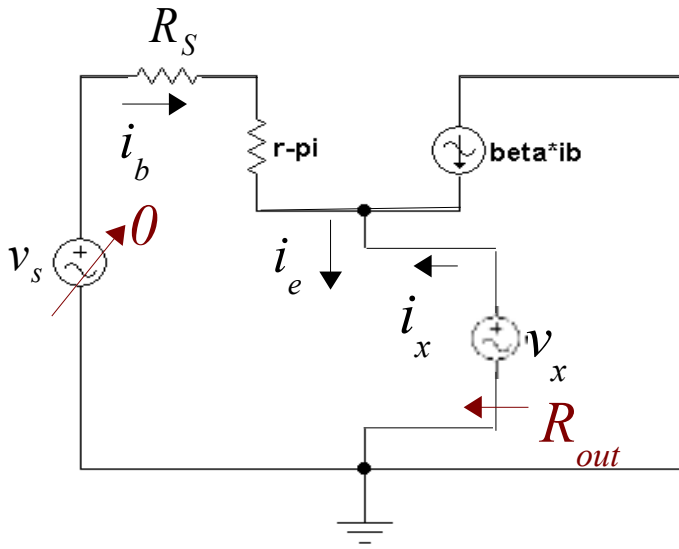
	<u>CE Amplifier</u>	<u>CC Amplifier</u>	<u>CB Amplifier</u>
Voltage Gain (A_V)	moderate ($-R_C/R_E$)	low (about 1)	high (R_C/R_S)
Current Gain (A_I)	moderate (β)	moderate ($\beta + 1$)	low (about 1)
Input Resistance	high ($R_B \beta R_E$)	high ($R_B \beta R_E$)	low (r_e)
Output Resistance	high ($R_C r_o$)	low (r_e)	high ($R_C r_o$)
		VCVS	CCCS

Of What value is a Unity Gain Amplifier?



To answer this question, we must examine the small-signal *output impedance* of the amplifier and its *power gain*.

Emitter Follower Output Resistance



$$i_x = -i_e = -i_b - \beta i_b = -(1 + \beta) i_b \Rightarrow i_b = \frac{-i_x}{(1 + \beta)}$$

$$v_x = -i_b (R_S + r_\pi) = \frac{R_S + r_\pi}{1 + \beta} i_x$$

$$R_{out} = \frac{v_x}{i_x} = \frac{R_S + r_\pi}{1 + \beta} \approx \frac{r_\pi}{1 + \beta} = r_e = \frac{1}{g_m} = \frac{V_T}{I_C}$$

Assume:

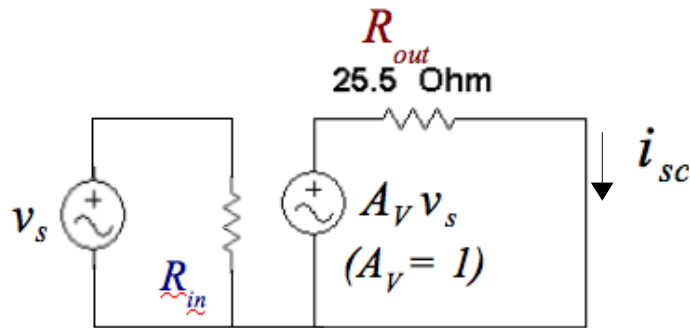
$$I_C = 1 \text{ mA} \Rightarrow r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} = 2500 \Omega$$

$$\beta = 100 \quad R_S = 50 \Omega$$

$$R_{out} \approx r_e = \frac{2550}{100} = 25.5 \Omega$$

Recall $R_{in} = r_{bg} = r_\pi + (\beta + 1) R_E$

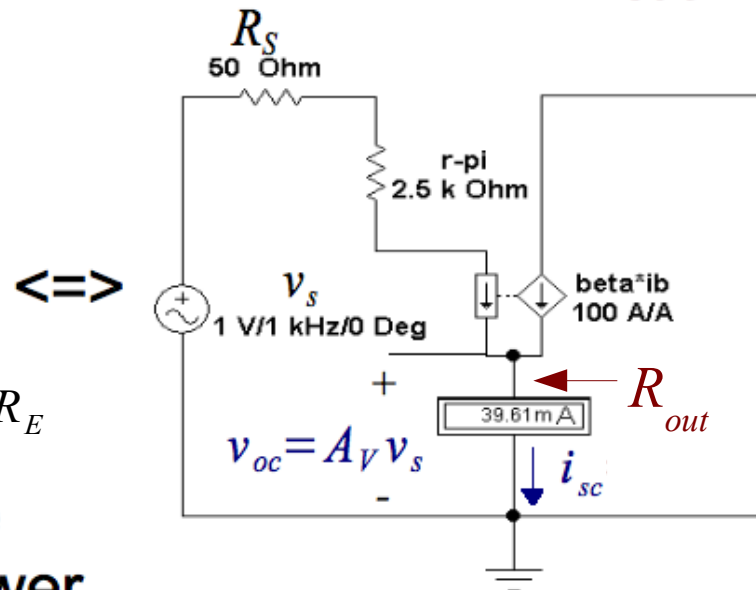
Multisim Verification of R_{out}



$$R_{in} = r_{bg} = R_S + r_{\pi} + (\beta + 1) R_E \approx (\beta + 1) R_E$$

Thevenin equivalent for the short-circuited emitter follower.

If $\beta = 200$, as for most good NPN transistors, R_{out} would be lower - close to 12Ω .



$$R_{out} = \frac{v_{oc}}{i_{sc}}$$

$$i_{sc} = (1 + \beta) i_b$$

$$v_s = R_S i_b + r_{\pi} i_b$$

$$R_{out} = \frac{A_V v_s}{i_{sc}} = \frac{R_S + r_{\pi}}{1 + \beta}$$

$$\beta = 100$$

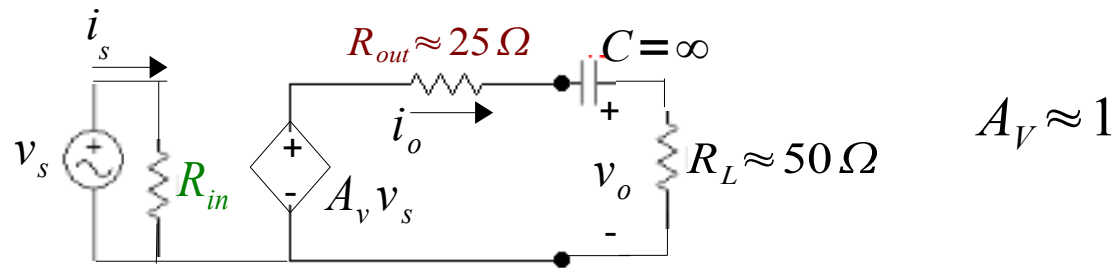
Multisim short circuit check

($\beta = 100, v_o = v_s$):

$$R_{out} = \frac{v_{oc}}{i_{sc}} = \frac{A_V v_{s(rms)}}{i_{sc(rms)}} = \frac{1}{0.0396} = 25.25 \Omega$$

Emitter Follower Power Gain

Consider the case where a $R_L = 50\Omega$ load is connected through an infinite capacitor to the emitter of the follower we designed. Using its Thevenin equivalent:



$$v_o = \frac{R_L A_V v_s}{R_L + R_{out}} = \frac{50}{75} v_s = \frac{2}{3} v_s$$

$$i_o = \frac{A_V v_s}{R_{out} + R_L} = \frac{v_s}{75}$$

$$p_o = v_o i_o = \frac{2}{225} v_s^2$$

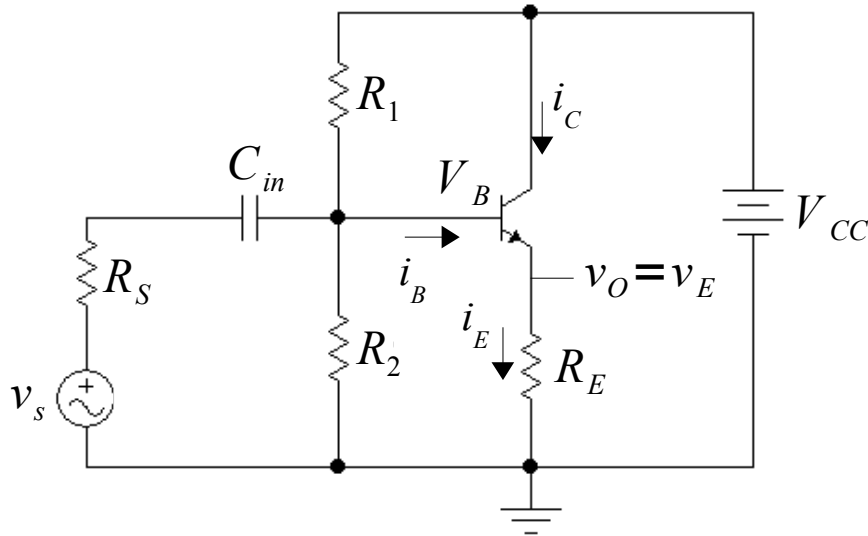
$$R_E \parallel R_L = 5.1 k\Omega \parallel 50\Omega \approx 50\Omega$$

$$i_s = i_b = \frac{v_s}{R_{in}} \approx \frac{v_s}{(\beta + 1) R_E \parallel R_L} \approx \frac{v_s}{101 \cdot 50} \approx \frac{v_s}{5000}$$

$$p_s = v_s i_s \approx \frac{1}{5000} v_s^2$$

$$A_{pwr} = \frac{p_o}{p_s} = \frac{2(5000)}{225} = 44.4 \gg 1$$

Emitter Follower Biasing – Typical Design



Split bias voltage drops about equally across the transistor V_{CE} (or V_{CB}) and V_{Re} (or V_B).

For simplicity, choose:

$$V_B = \frac{V_{CC}}{2} \Rightarrow R_1 = R_2$$

Then, choose/specified I_E , and the rest of the design follows:

$$R_E = \frac{V_E}{I_E} = \frac{V_{CC}/2 - 0.7}{I_E}$$

For an assumed $\beta = 100$:

As with CE bias design, stable op. pt.

$\Rightarrow R_B \ll (\beta + 1) R_E$, i.e.

$$R_B = R_1 \parallel R_2 = \frac{R_1}{2} = \frac{(\beta + 1)}{10} R_E \approx 10 R_E$$

$$R_1 = R_2 = 20 R_E$$

Typical Design - Cont.

Given: $R_{out} = r_e = 25 \Omega$

$$V_{CC} = 12V$$

And the rest of the design follows

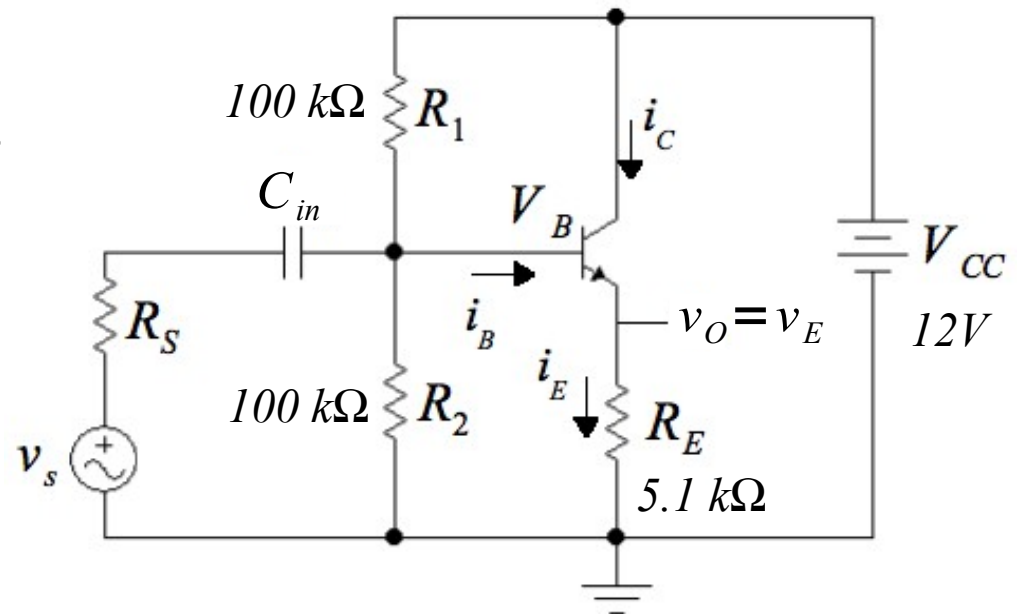
$$I_E \approx I_C = \frac{V_T}{r_e} = 1 \text{ mA}$$

$$R_E = \frac{V_E}{I_E} = \frac{12/2 - 0.7}{10^{-3}} = 5.3 \text{ k}\Omega$$

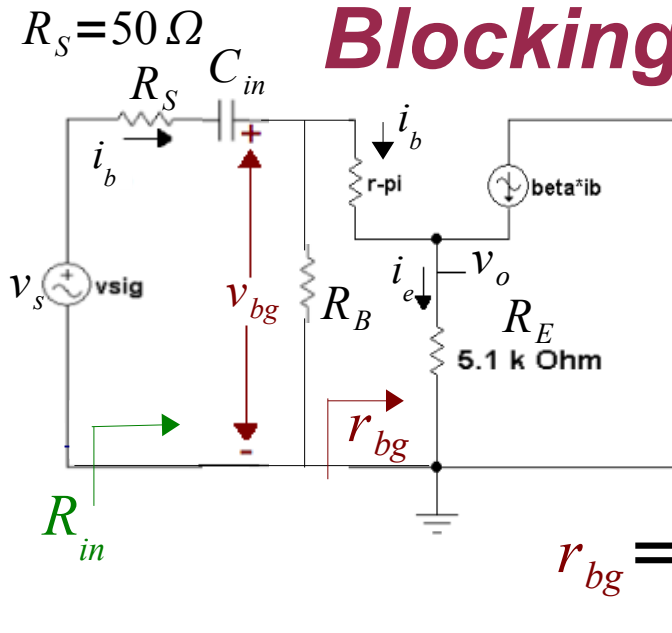
Use standard sizes:

$$R_E = 5.1 \text{ k}\Omega$$

$$R_1 = R_2 = 100 \text{ k}\Omega$$



Blocking Capacitor - C_{in} - Selection



Use the base current expression:

$$v_{bg} = r_{\pi} i_b + R_E i_E = (r_{\pi} + (\beta + 1) R_E) i_b$$

$$i_b = \frac{v_{bg}}{r_{\pi} + (\beta + 1) R_E}$$

$$r_{bg} = \frac{v_{bg}}{i_b} = r_{\pi} + (\beta + 1) R_E \approx (\beta + 1) R_E = 101 \cdot 5.1 k = 515 k \Omega$$

To obtain the base to ground resistance of the transistor:
This transistor input resistance is in parallel with $R_B = 50 k\Omega$,
forming the total amplifier input resistance:

$$R_{in} = R_S + R_B \parallel r_{bg} \approx R_B \parallel r_{bg} = \frac{515}{(515 + 50)} 50 k \Omega = 45.6 k \Omega \approx R_B = 50 k \Omega$$

C_{in} – Selection cont.

Choose C_{in} such that its reactance is $\leq 1/10$ of R_B at f_{min} :

$$\frac{1}{2\pi f C_{in}} = \frac{R_B}{10}$$

$$C_{in} \geq \frac{10}{2\pi f_{min} R_B}$$

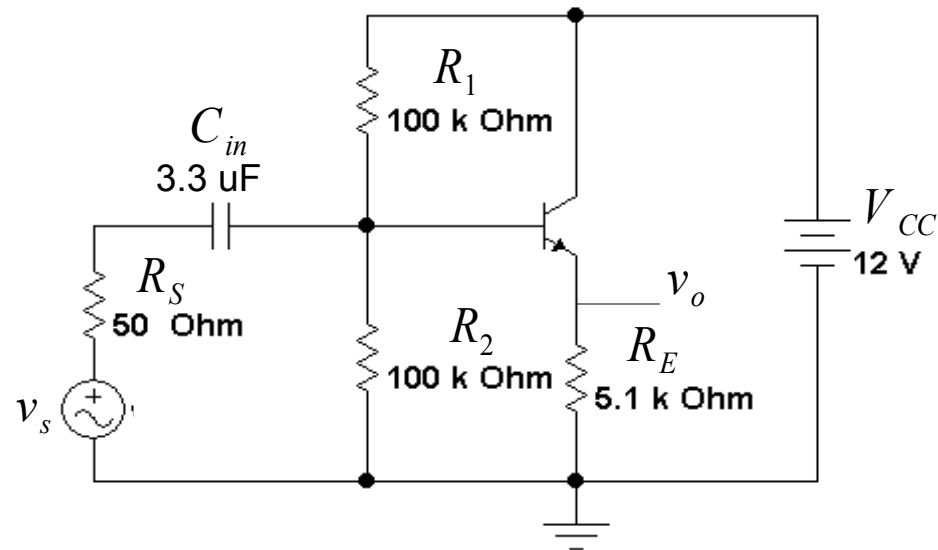
Assume $f_{min} = 20 \text{ Hz}$

with $R_B = 50 \text{ k}\Omega$

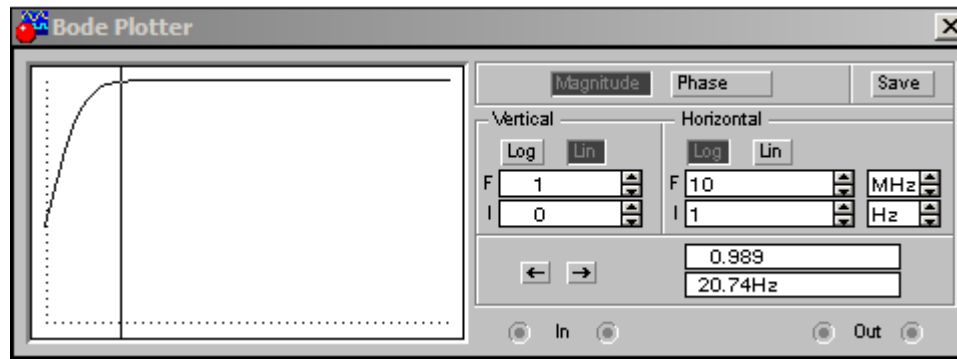
$$C_{in} \geq \frac{10}{2\pi \cdot 20 \cdot 50 \cdot 10^3} = 1.59 \mu F$$

Pick $C_{in} = 3.3 \mu F$, the nearest standard value in the Detkin Lab.
We could be (unnecessarily) more precise and include r_{bg} and R_s as part of the total resistance in the loop.

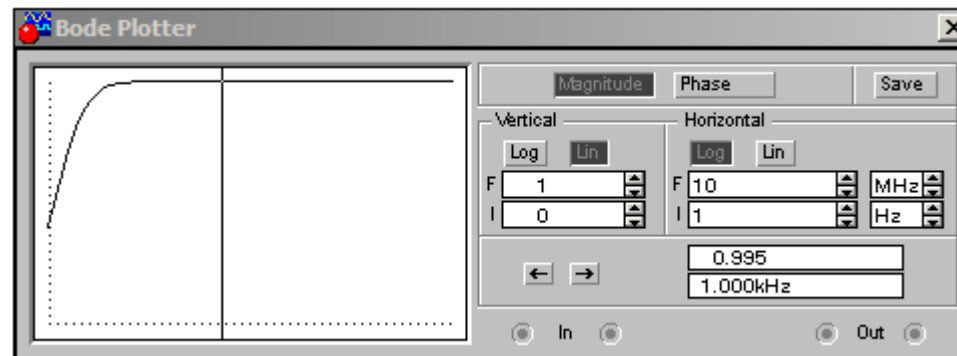
Final Design



Multisim Simulation Results



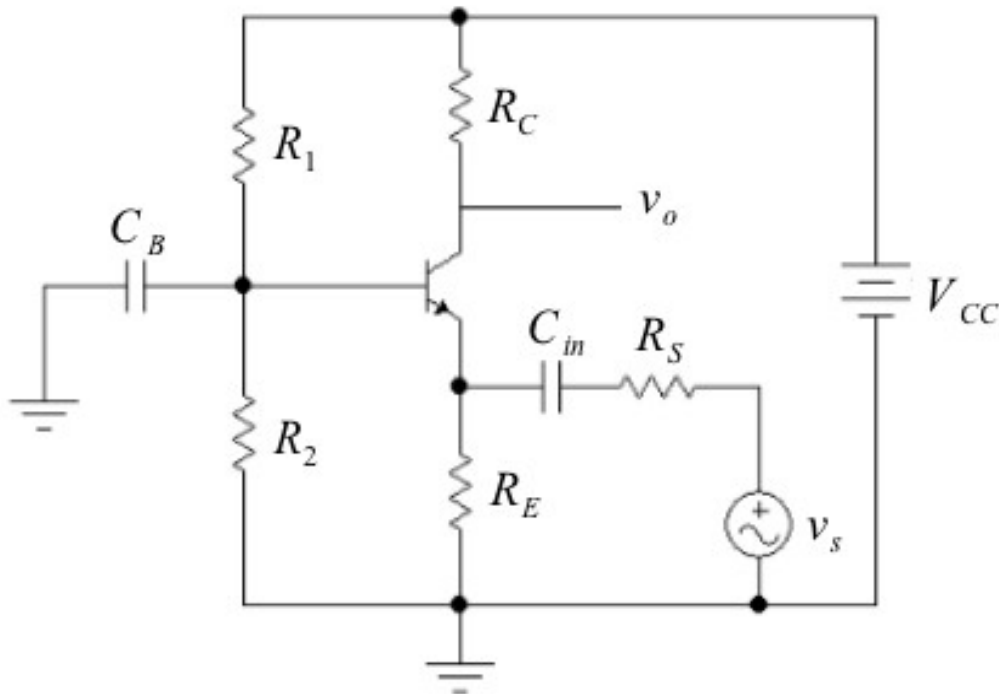
20 Hz Data



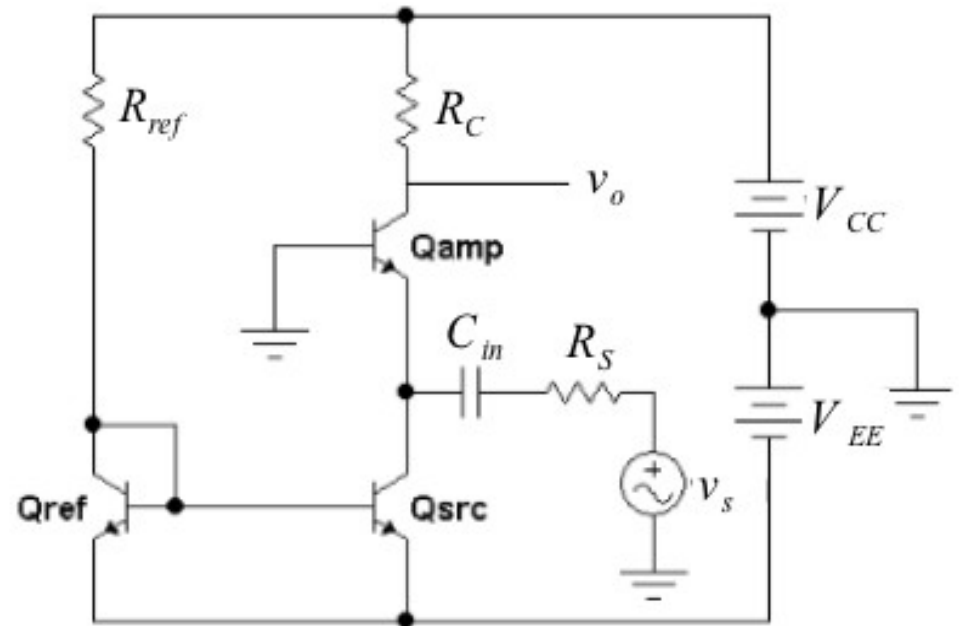
1 kHz Data

$$A_v = 0.995$$

The Common Base Amplifier



Voltage Bias Design



Current Bias Design

Common Base Configuration

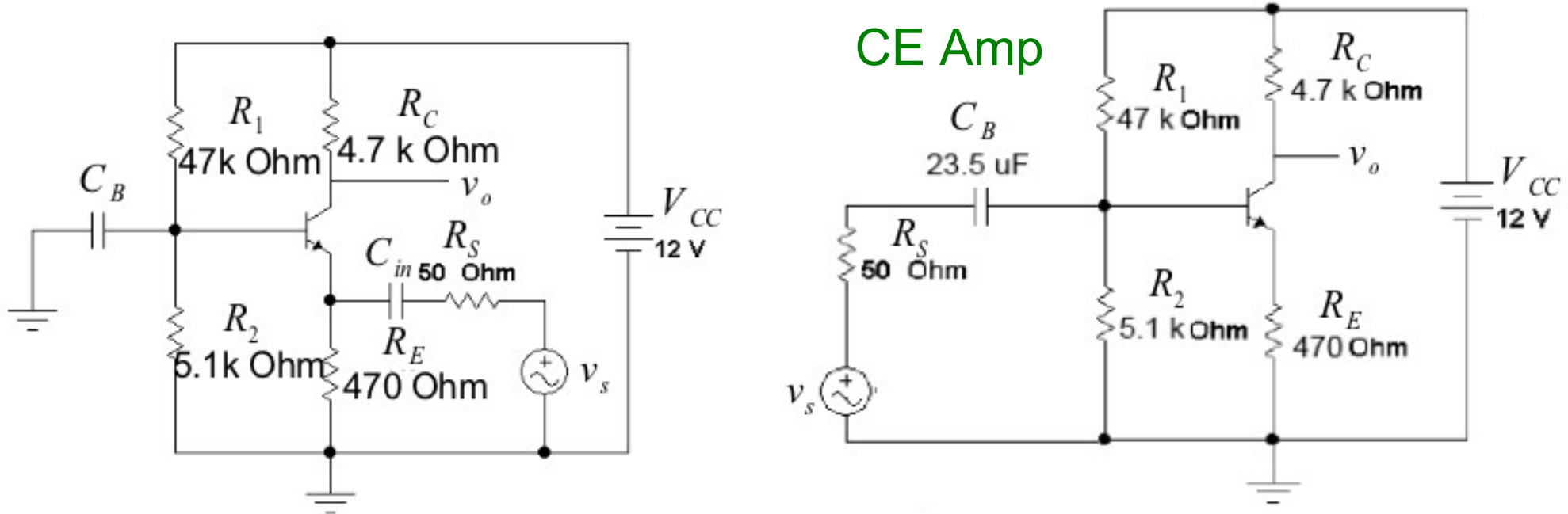
Both voltage and current biasing follow the same rules as those applied to the common emitter amplifier.

As before, insert a blocking capacitor in the input signal path to avoid disturbing the dc bias.

The common base amplifier uses a bypass capacitor – or a direct connection from base to ground to hold the base at ground *for the signal only!*

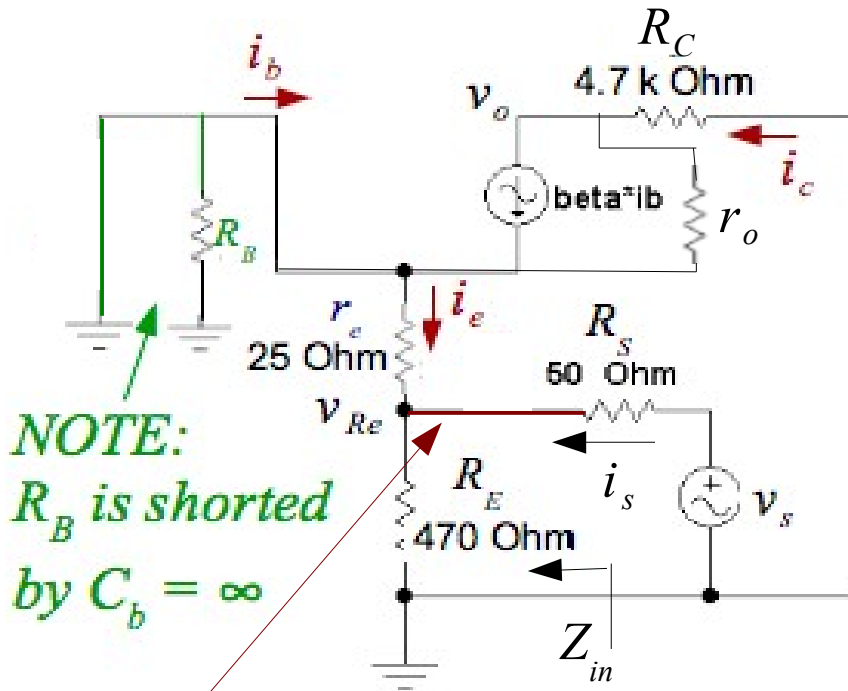
The common emitter amplifier (except for intentional R_E feedback) holds the emitter at signal ground, while the common collector circuit does the same for the collector.

Voltage Bias Common Base Design



- ◆ We keep the same bias that we established for the gain of 10 common emitter amplifier.
- ◆ All that we need to do is pick the capacitor values and calculate the circuit gain.

Mid-band Small Signal Analysis



NOTE:
 R_B is shorted
by $C_b = \infty$

$$C_{in} = \infty$$

Note: $i_s = -i_e$
 $R_E \gg r_e$

Input Impedance

$$v_{Re} = r_e \parallel R_E i_s$$

$$Z_{in} = \frac{v_{Re}}{i_s} = r_e \parallel R_E \approx r_e = \frac{V_T}{I_C}$$

Current Gain

$$A_i = \frac{i_e}{i_c} = \frac{1}{\alpha} \approx 1$$

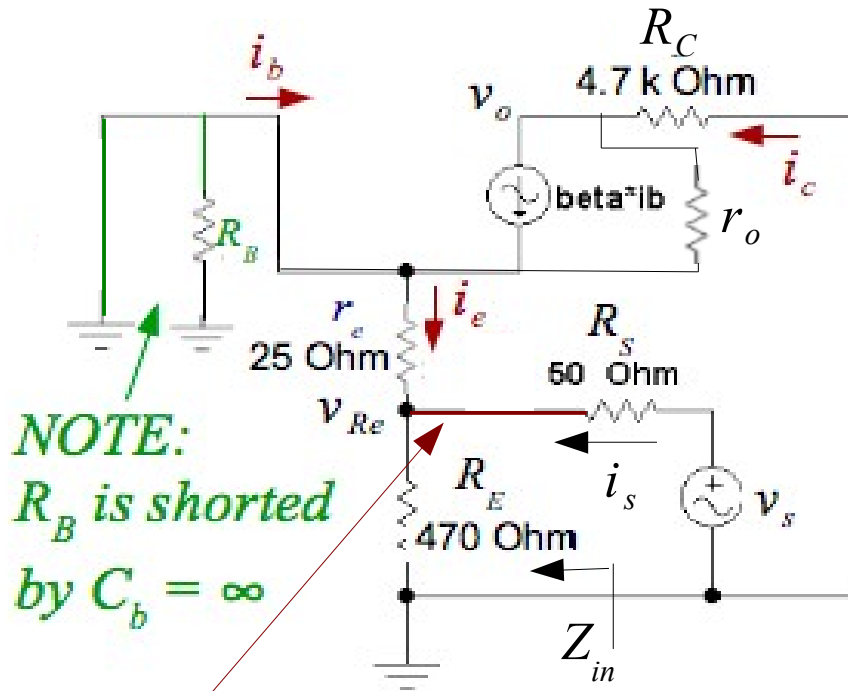
Voltage Gain

$$v_s = -i_e R_S - r_e \parallel R_E i_e$$

$$v_o = -R_C i_c = -\alpha R_C i_e = \frac{1}{\alpha} \frac{R_C}{R_S + r_e \parallel R_E} v_s$$

$$A_v = \frac{v_o}{v_s} \approx \frac{1}{\alpha} \frac{R_C}{R_S + r_e}$$

Review - Mid-band Small Signal Analysis



Input Impedance

$$Z_{in} = ?$$

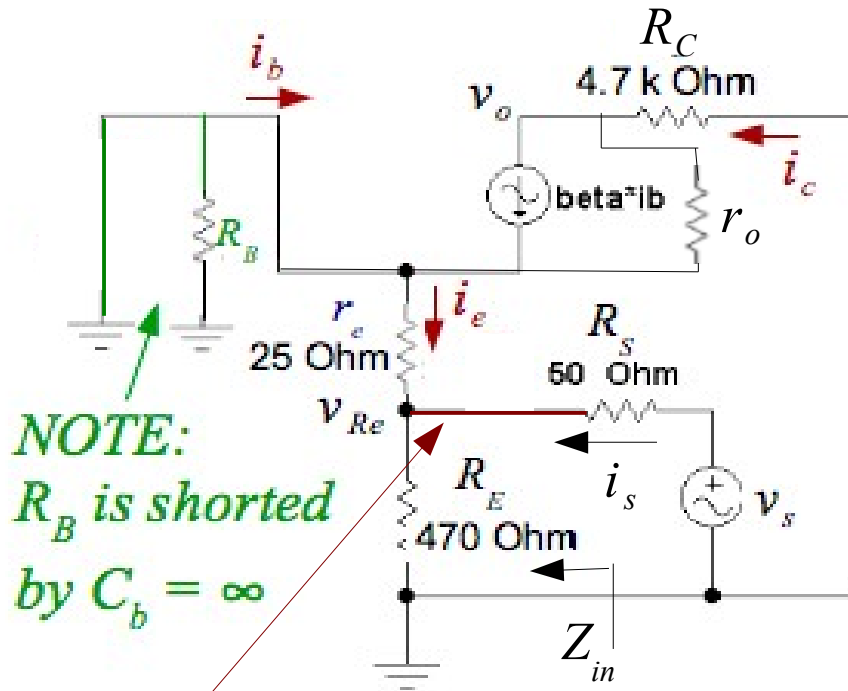
Current Gain

$$A_i = ?$$

Voltage Gain ($r_o \gg R_C$)

$$A_v = ?$$

Review - Mid-band Small Signal Analysis



NOTE:
 R_B is shorted
by $C_b = \infty$

$$C_{in} = \infty$$

Note: $i_s = -i_e$
 $R_E \gg r_e$

Input Impedance

$$v_{Re} = r_e \parallel R_E i_s$$

$$Z_{in} = \frac{v_{Re}}{i_s} = r_e \parallel R_E \approx r_e = \frac{V_T}{I_C}$$

Current Gain

$$A_i = \frac{i_e}{i_c} = \frac{1}{\alpha} \approx 1$$

Voltage Gain ($r_o \gg R_C$)

$$v_s = -i_e R_S - r_e \parallel R_E i_e$$

$$v_o = -R_C i_c = -\alpha R_C i_e = \frac{1}{\alpha} \frac{R_C}{R_S + r_e \parallel R_E} v_s$$

$$A_v = \frac{v_o}{v_s} \approx \frac{1}{\alpha} \frac{R_C}{R_S + r_e}$$

Common Base Small Signal Analysis - C_{in}

Determine C_{in} : (let $C_b = \infty$)

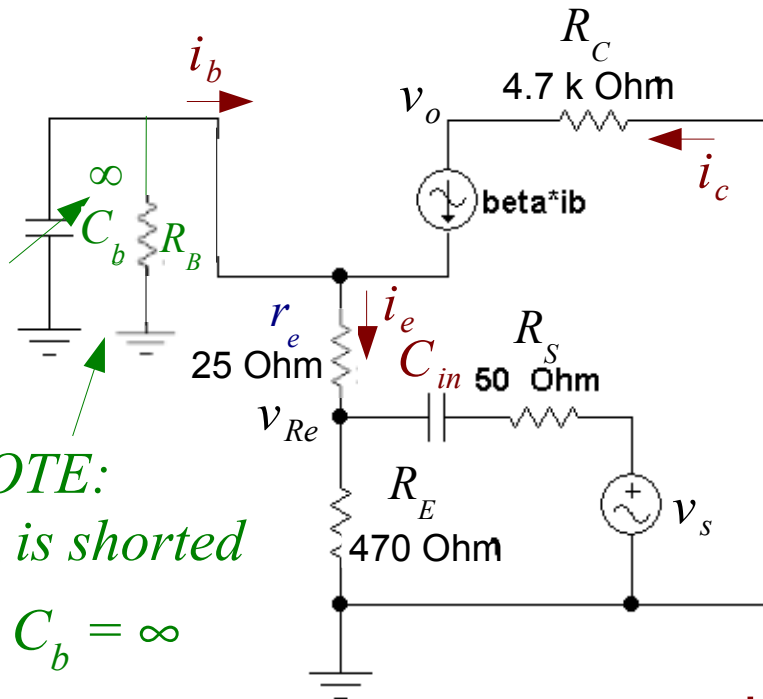
Find an equivalent impedance for the input circuit, R_S , C_{in} , and R_E :

$$v_{Re} = \frac{R_E \parallel r_e}{R_E \parallel r_e + R_S + \frac{1}{j2\pi f C_{in}}} v_s$$

$r_e = \frac{r_\pi}{1 + \beta}$

ideally $v_{Re} = \frac{R_E \parallel r_e}{R_E \parallel r_e + R_S} v_s$ for $f \geq f_{min}$

$$\frac{1}{2\pi f_{min} C_{in}} \ll R_S + R_E \parallel r_e \Rightarrow \frac{1}{2\pi f_{min} C_{in}} = \frac{R_S + r_e}{10} \Rightarrow C_{in} = \frac{10}{2\pi f_{min} (R_S + r_e)}$$



NOTE:
 R_B is shorted
by $C_b = \infty$

Determine C_{IN} cont.

A suitable value for C_{in} for a 20 Hz lower frequency:

$$2\pi f_{min} C_{in} (R_S + r_e) \gg 1 \Rightarrow C_{in} \geq \frac{10}{2\pi f_{min} (R_S + r_e)} = \frac{10}{2\pi \cdot 20 \cdot 75} F$$

$$C_{in} = \frac{10}{125.6 \cdot 75} \approx 1062 \mu F !$$

Not too Practical!

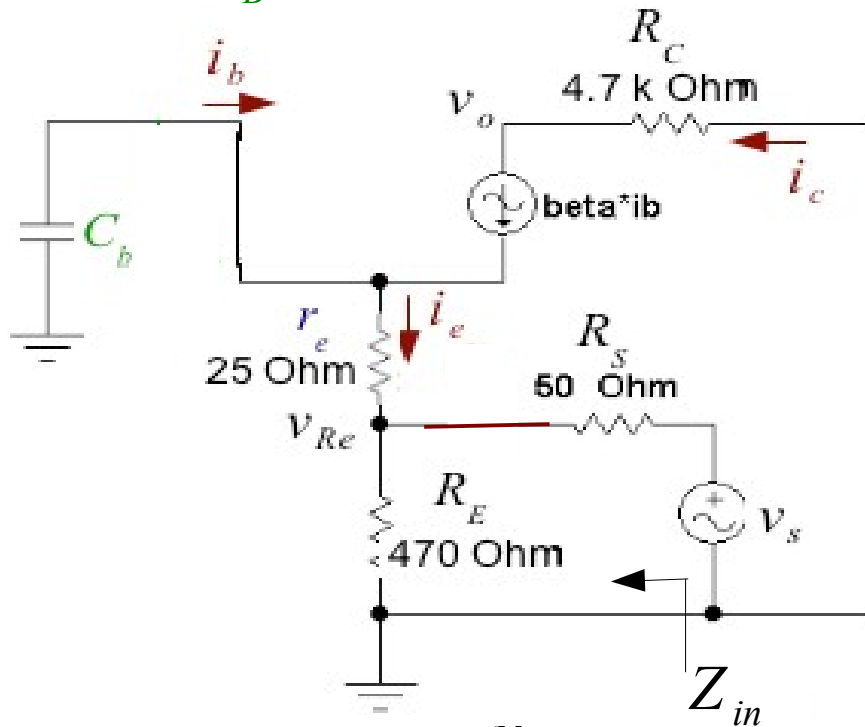
Must choose smaller value of C_{in} .

Choose: $2\pi f_{min} C_{in} (R_S + r_e) = 1$

$$C_{in} = \frac{1}{125.6 \cdot 75} \approx 106.2 \mu F$$

Small-signal Analysis - C_b

ignore R_B



Determine C_b : (let $C_{in} = \infty$)

Note the ac reference current reversals (due to v_s polarity)!

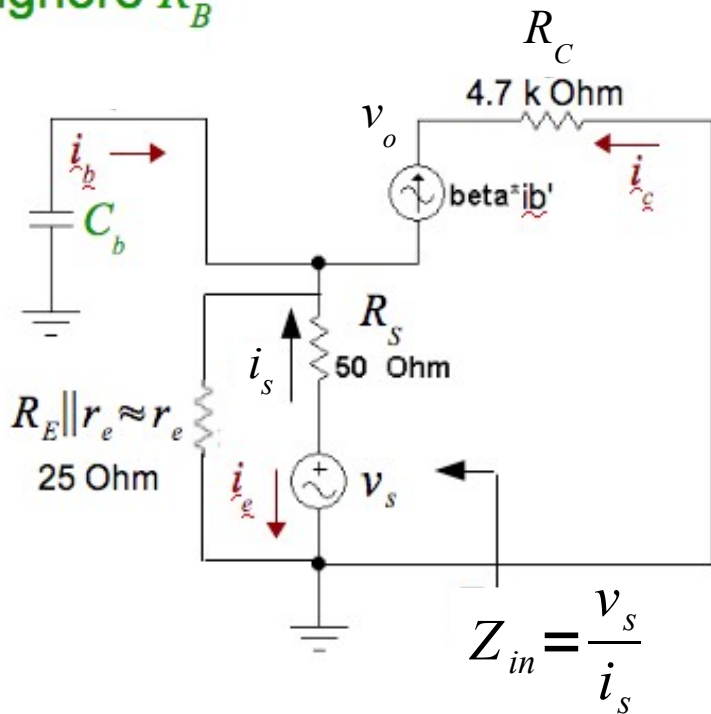
$$v_s = R_S i_s + \left(R_E \parallel \left(r_e + \frac{1}{j\omega C_b (\beta + 1)} \right) \right) i_s$$

$$Z_{in} = \frac{v_s}{i_s} = R_S + R_E \parallel \left(r_e + \frac{1}{j\omega C_b (\beta + 1)} \right)$$

Determine $Z_{in} = \frac{v_s}{i_s}$

Determine – C_B

ignore R_B



$$Z_{in} = \frac{v_s}{i_s} = R_S + R_E || \left(r_e + \frac{1}{j\omega C_b (\beta + 1)} \right)$$

ideally $Z_{in} \approx R_S + R_E || r_e \quad f \geq f_{min}$

or $\frac{1}{2\pi f C_b (\beta + 1)} \ll r_e \quad f \geq f_{min}$

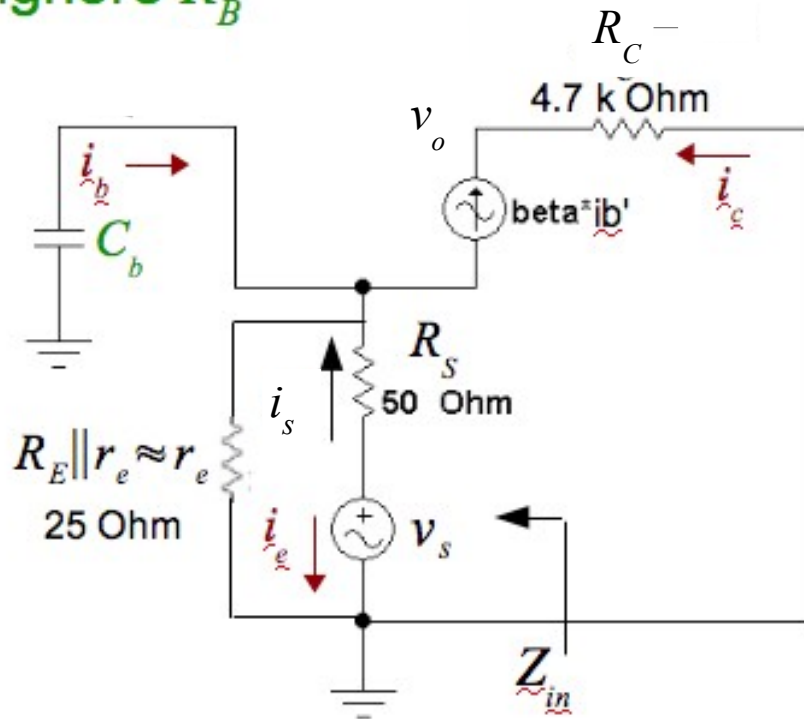
$$C_b \gg \frac{1}{2\pi f r_e (\beta + 1)}$$

Choose (conservatively):

$$C_b = \frac{10}{2\pi f_{min} ((\beta + 1) r_e)} F$$

Determine - C_B cont.

ignore R_B



Choosing (conservatively):

$$C_b = \frac{10}{2\pi f_{min}((\beta + 1)r_e)} F$$

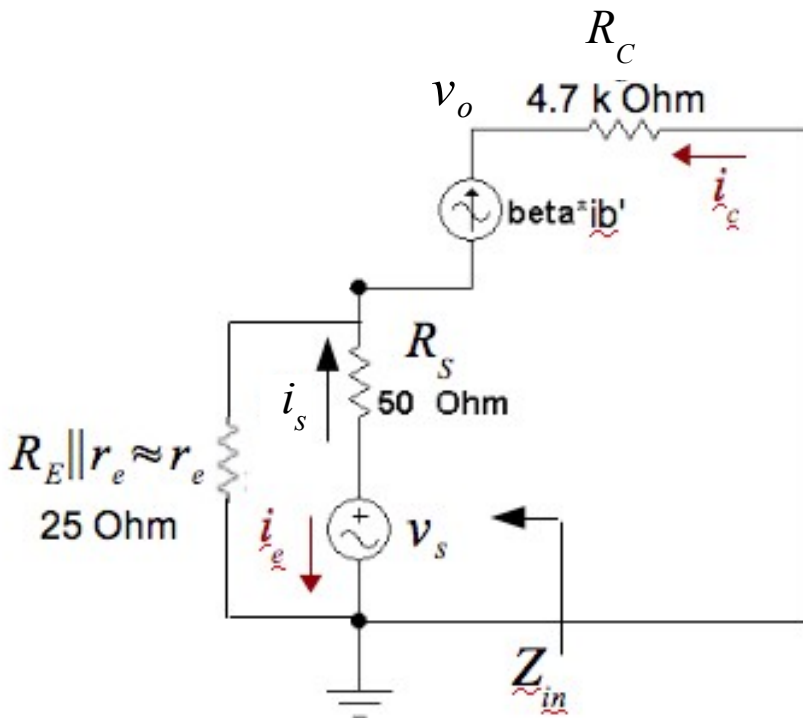
for $f_{min} = 20 \text{ Hz}$

i.e.

$$C_b = \frac{10}{2\pi 20((100)(25))} = 31.8 \mu F$$



Small-signal Analysis – Voltage Gain



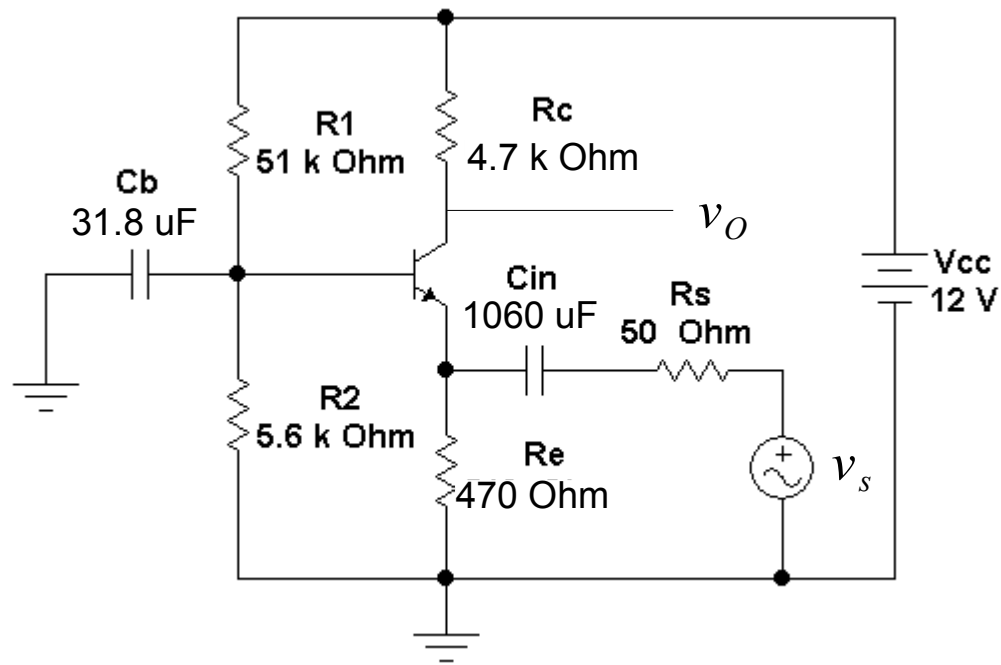
$$i_e = -i_s \approx \frac{-1}{R_S + r_e} v_s$$

$$v_o = -R_C i_c = -\alpha R_C i_e = \frac{\beta}{\beta + 1} \frac{R_C}{R_S + r_e} v_s$$

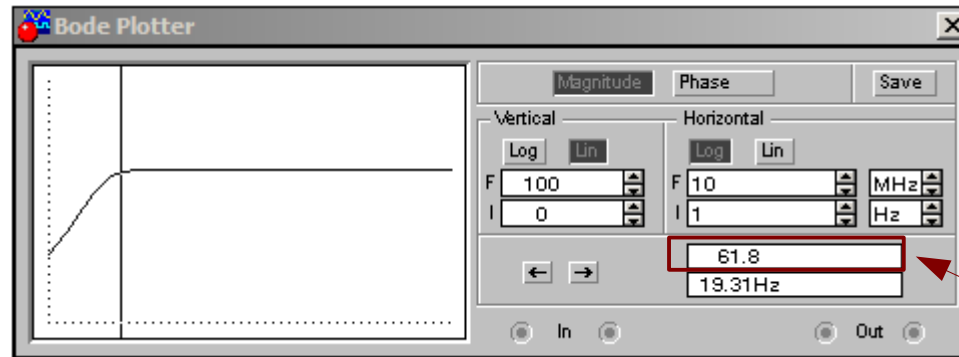
$$A_V = \frac{v_o}{v_s} = \frac{\beta}{\beta + 1} \frac{R_C}{R_S} = \frac{100}{101} \frac{4700}{50 + 25} = 62.1$$

Assume: $C_b = C_{in} = \infty$

Multisim Simulation

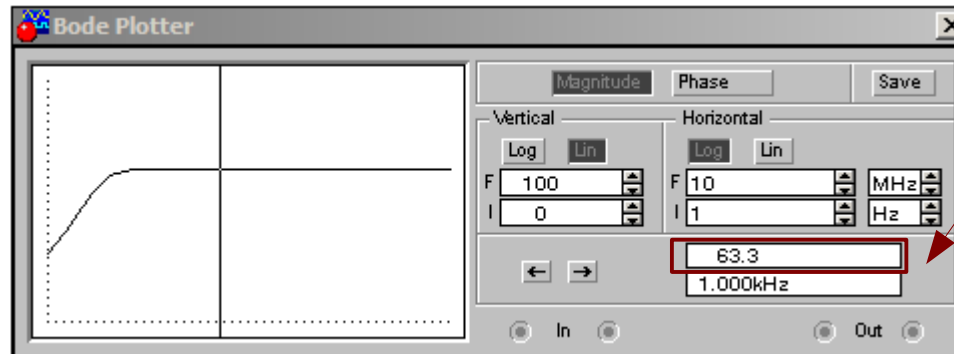


Multisim Frequency Response



20 Hz response

vertical axis is
a linear scale



1 kHz Response

$$A_{v(sim)} = 63.3 > A_{v(theory)} = 62.1$$