ESE 3400: Medical Devices Lab

Lec 12: October 24, 2022

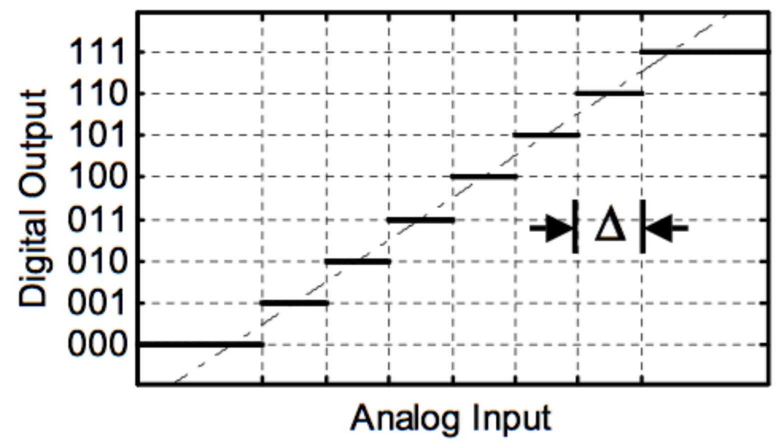
Data Converters Pt 2

Lecture Outline

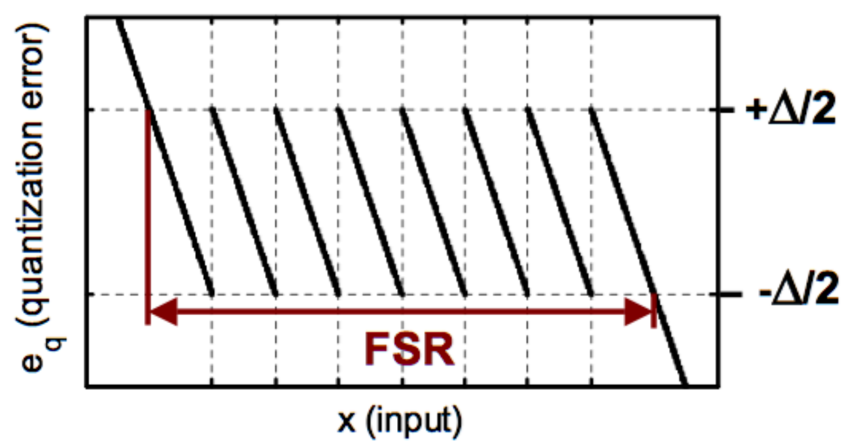
- SQNR
- Oversampling
- Nyquist ADCs
- Flash ADCs
- SAR ADCs

Ideal B-bit Quantizer

- Practical quantizers have a limited input range and a finite set of output codes
- E.g. a 3-bit quantizer can map onto $2^3 = 8$ distinct output codes



- Quantization error grows out of bounds beyond code boundaries
- We define the full scale range (FSR) as the maximum input range that satisfies $|e_q| \leq \Delta/2$
  - Implies that $FSR = 2^B \cdot \Delta$

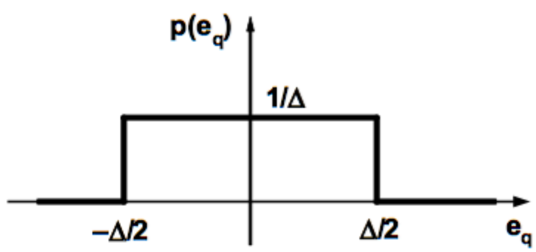


Effect of Quantization Error on Signal

- Quantization error is a deterministic function of the signal
  - Consequently, the effect of quantization strongly depends on the signal itself
- Unless, we consider fairly trivial signals, a deterministic analysis is usually impractical
  - More common to look at errors from a statistical perspective
  - "Quantization noise”

Quantization Error Statistics

- Crude assumption: $e_q(x)$ has uniform probability density
- This approximation holds reasonably well in practice when
  - Signal spans large number of quantization steps
  - Signal is "sufficiently active"
  - Quantizer does not overload

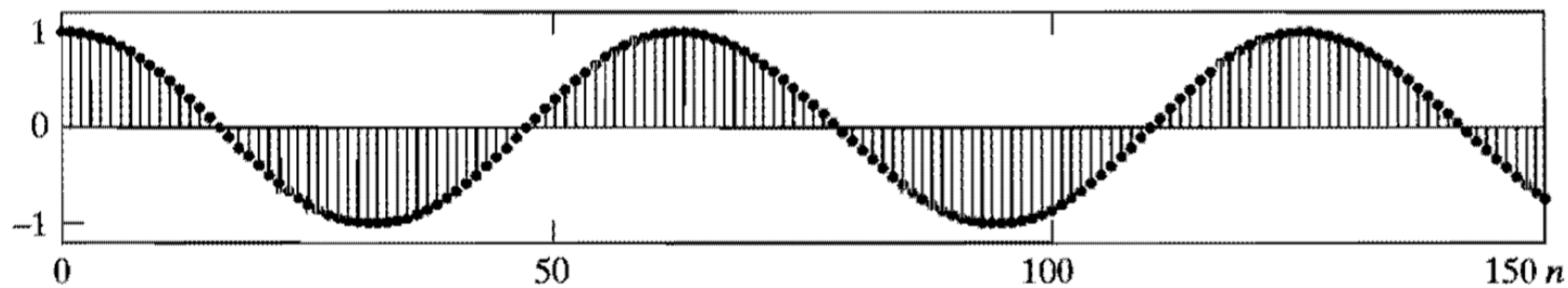


Mean $\bar{e} = \int_{-\Delta/2}^{+\Delta/2} \frac{e}{\Delta} de = 0$

Variance $\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12}$

Quantization Noise

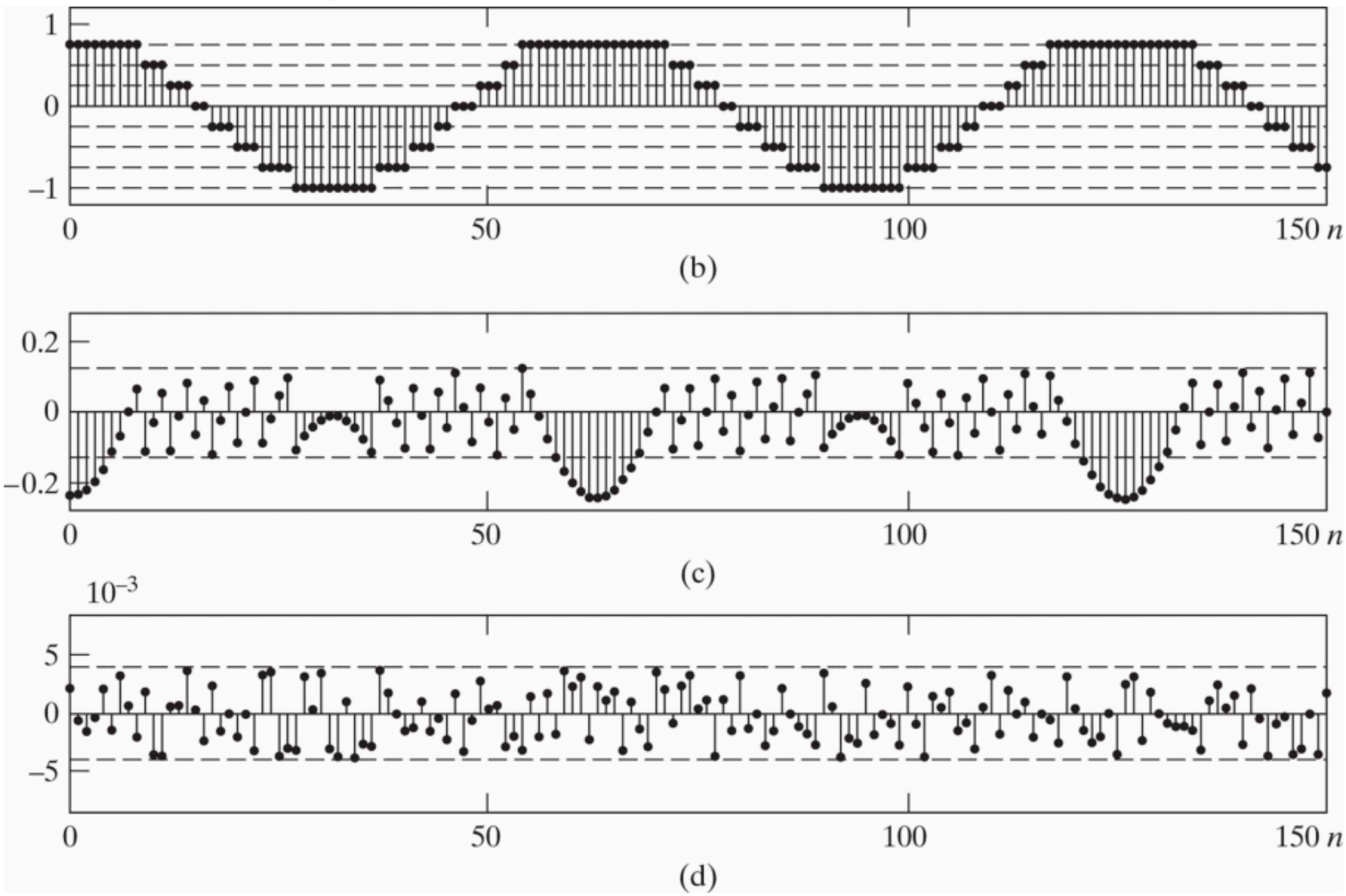
- **Figure 4.57** Example of quantization noise. (a) Unquantized samples of the signal x[n] = 0.99cos(n/10).



(a)

Quantization Noise

- **Figure 4.57**(continued) (b) Quantized samples of the cosine waveform in part (a) with a 3-bit quantizer. (c) Quantization error sequence for 3-bit quantization of the signal in (a). (d) Quantization error sequence for 8-bit quantization of the signal in (a).



Signal-to-Quantization-Noise Ratio

- Assuming full-scale sinusoidal input, we have

$$SNR_Q = 6.02B + 1.76\ dB$$

B (Number of Bits)	SQNR
8	50dB
12	74dB
16	98dB
20	122dB

Signal-to-Quantization-Noise Ratio

- For uniform B bits quantizer

$$SNR_Q = 10\log_{10}\left(\frac{\sigma_x^2}{\sigma_e^2}\right)$$

Signal-to-Quantization-Noise Ratio

- For uniform B bits quantizer

$$SNR_Q = 10\log_{10}\left(\frac{\sigma_x^2}{\sigma_e^2}\right) = 10\log_{10}\left(\frac{12\cdot 2^{2B}\sigma_x^2}{FSR^2}\right)$$

$$\mathrm{SNR}_Q = 6.02B + 10.8 - 20\log_{10}\left(\frac{FSR}{\sigma_x}\right)$$

Quantizer range

rms of amp

Signal-to-Quantization-Noise Ratio

$$\text{SNR}_Q = 6.02B + 10.8 - 20\log_{10}\left(\frac{FSR}{\sigma_x}\right)$$

Quantizer range

rms of amp

- Improvement of 6dB with every bit
- The range of the quantization must be adapted to the rms amplitude of the signal
  - Tradeoff between clipping and noise!
  - Often use pre-amp
  - Sometimes use analog auto gain controller (AGC)

Signal-to-Quantization-Noise Ratio

- Assuming full-scale sinusoidal input, we have

$$\mathrm{SNR}_Q = 6.02B + 10.8 - 20\log_{10}\left(\frac{FSR}{\sigma_x}\right)$$

Quantizer range

rms of amp

Signal-to-Quantization-Noise Ratio

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$$SNR_Q = 6.02B + 1.76 \text{ dB}$$

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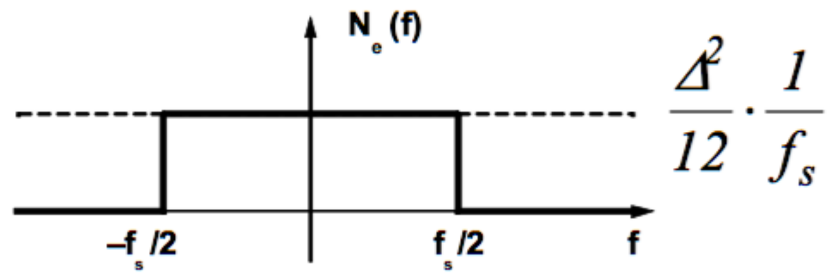
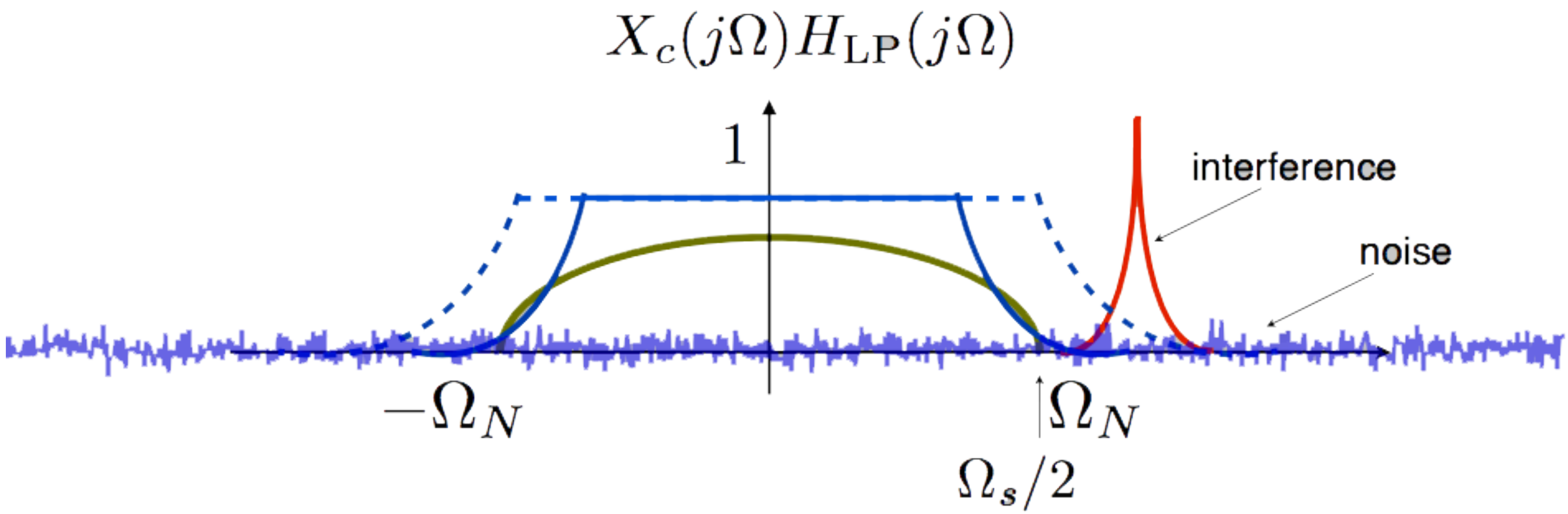
Quantization Noise Spectrum

- If the quantization error is "sufficiently random", it also follows that the noise power is uniformly distributed in frequency



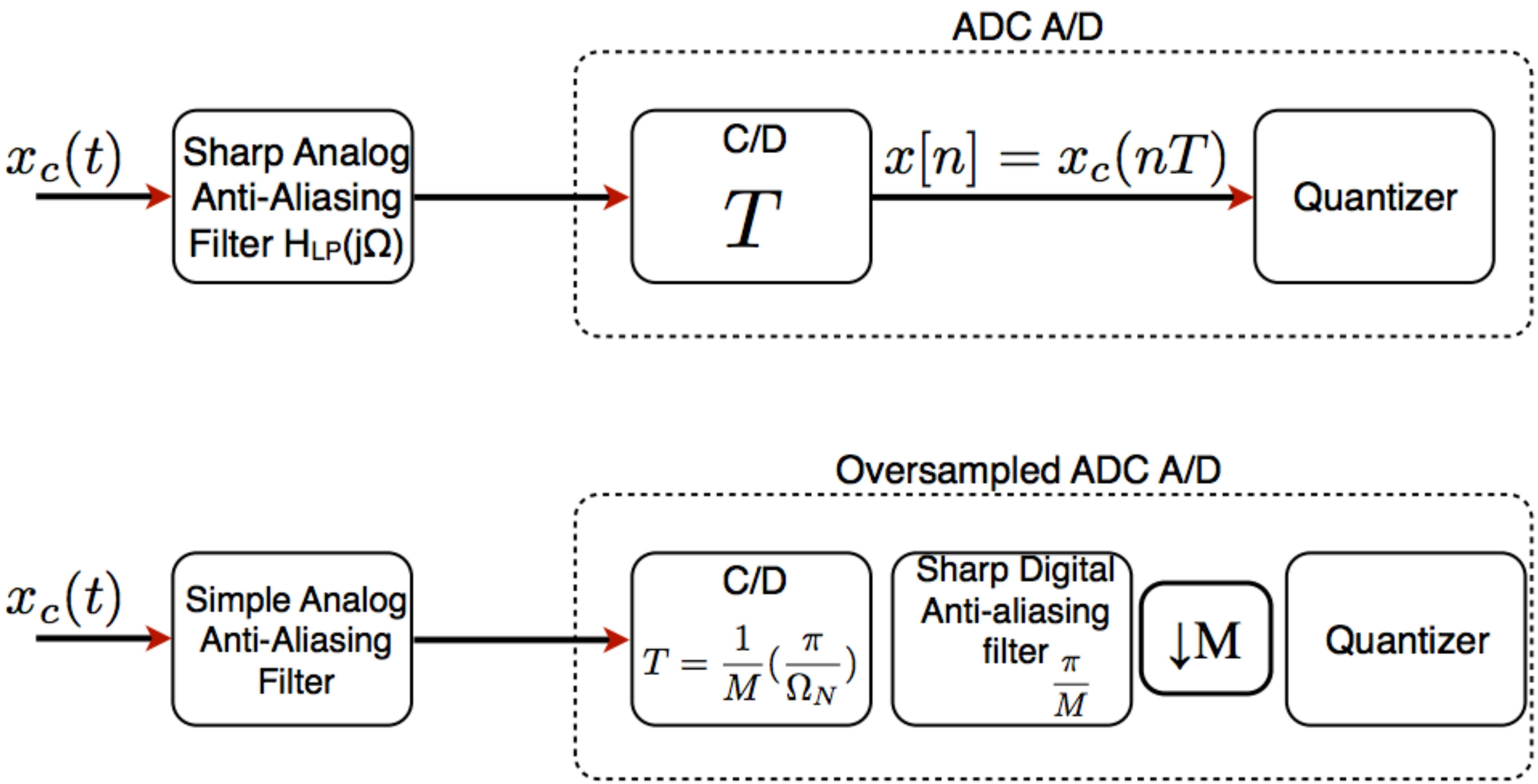
- References
  - W. R. Bennett, "Spectra of quantized signals," Bell Syst. Tech. J., pp. 446-72, July 1988.
  - B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," IRE Trans. Circuit Theory, vol. CT-3, pp. 266-76, 1956.

Non-Ideal Anti-Aliasing Filter

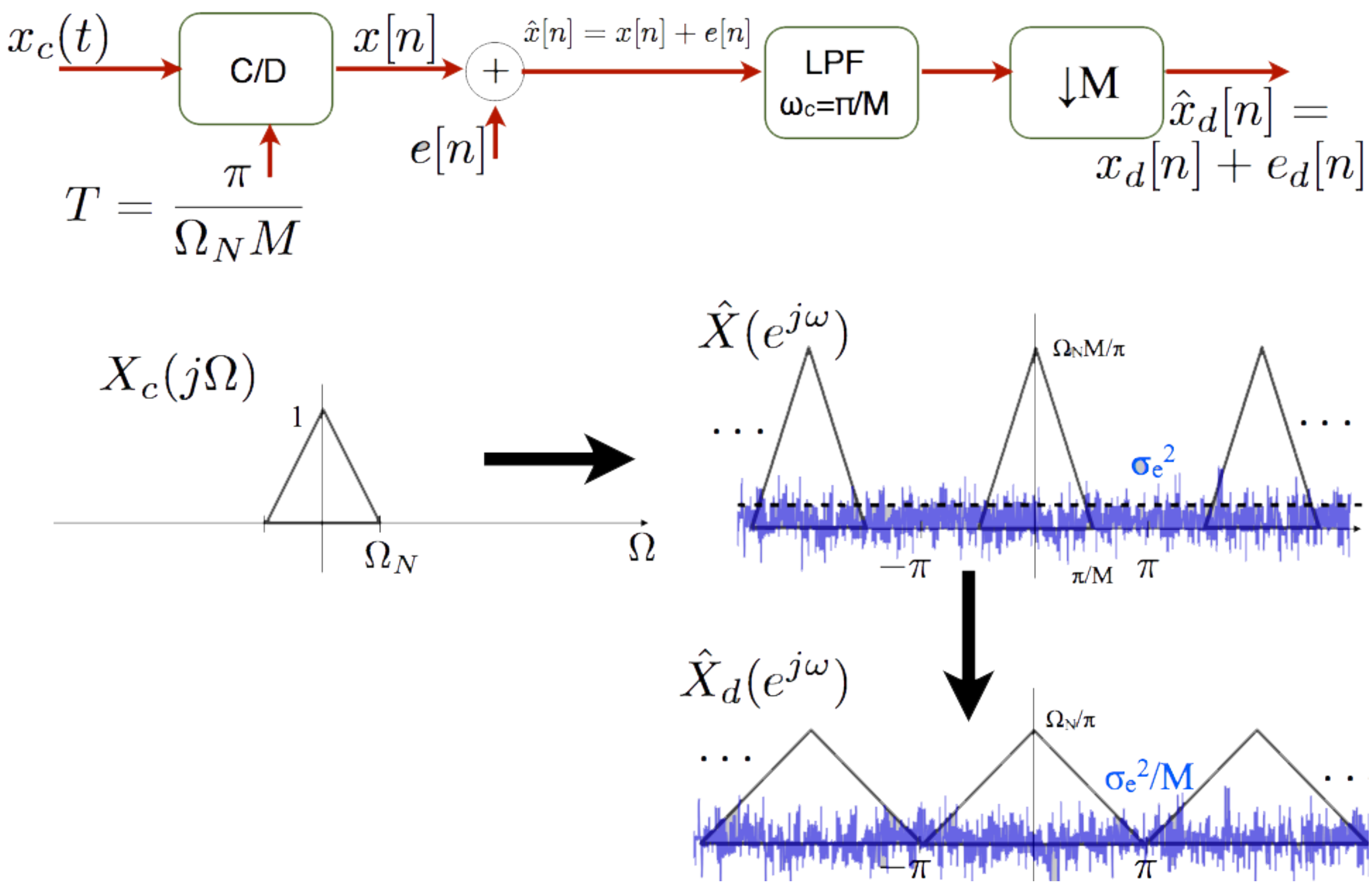


- Problem: Hard to implement sharp analog filter
- Consequence: Crop part of the signal and suffer from noise and interference

Oversampled ADC



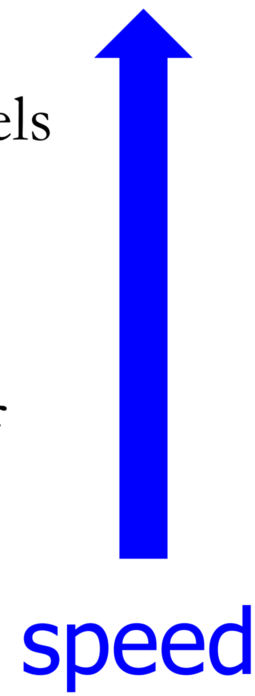
Quantization Noise with Oversampling



ADC Architectures

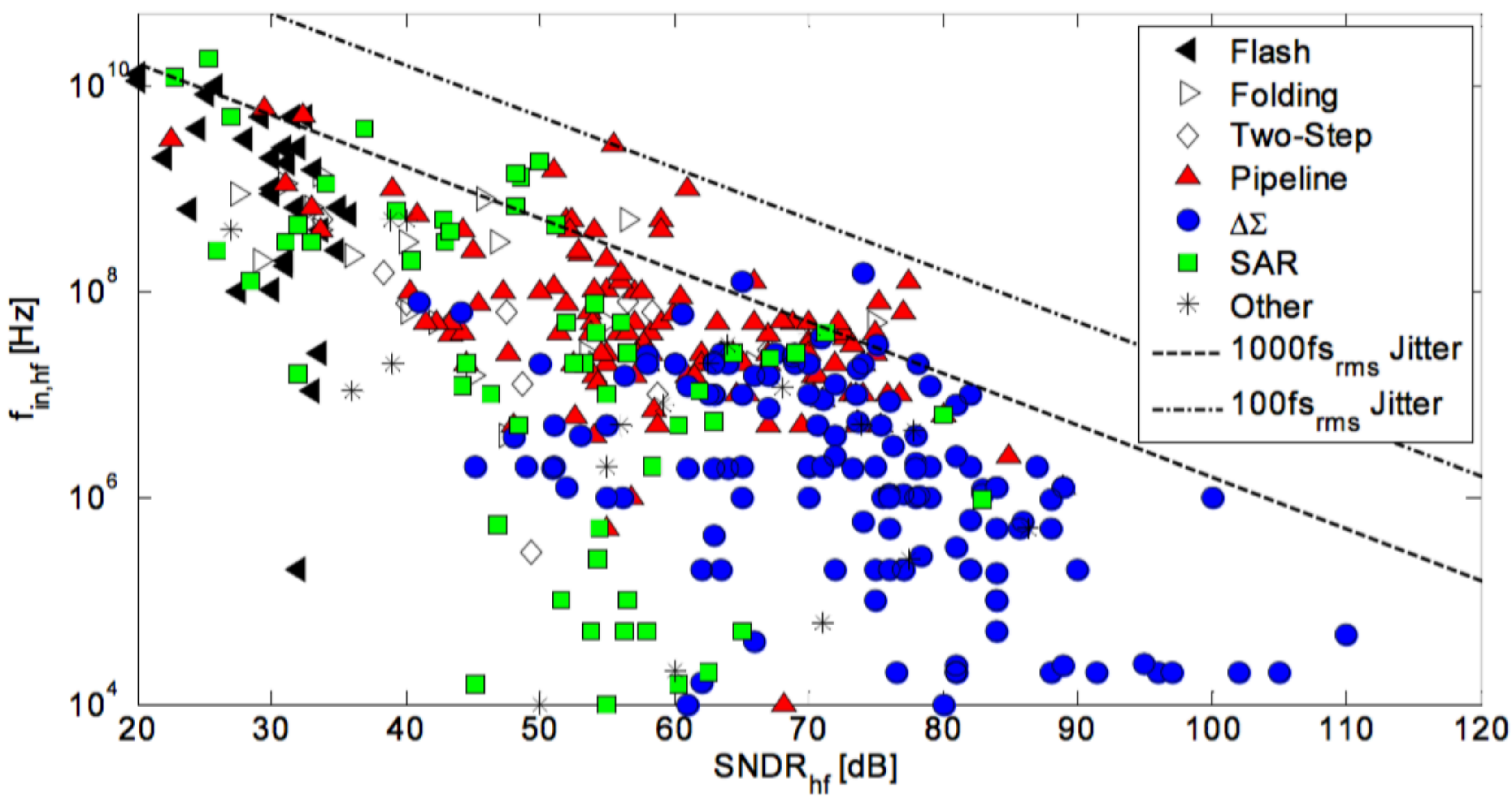
Nyquist ADC Architectures

- Word-at-a-time
  - E.g. flash ADC
  - Instantaneous comparison with 2^B-1 reference levels
- Multi-step
  - E.g. pipeline ADCs
  - Coarse conversion, followed by fine conversion of residuals
- Bit-at-a-time
  - E.g. successive approximation ADCs
  - Conversion via a binary search algorithm



ADC Survey (ISSCC & VLSI 1997-2013)

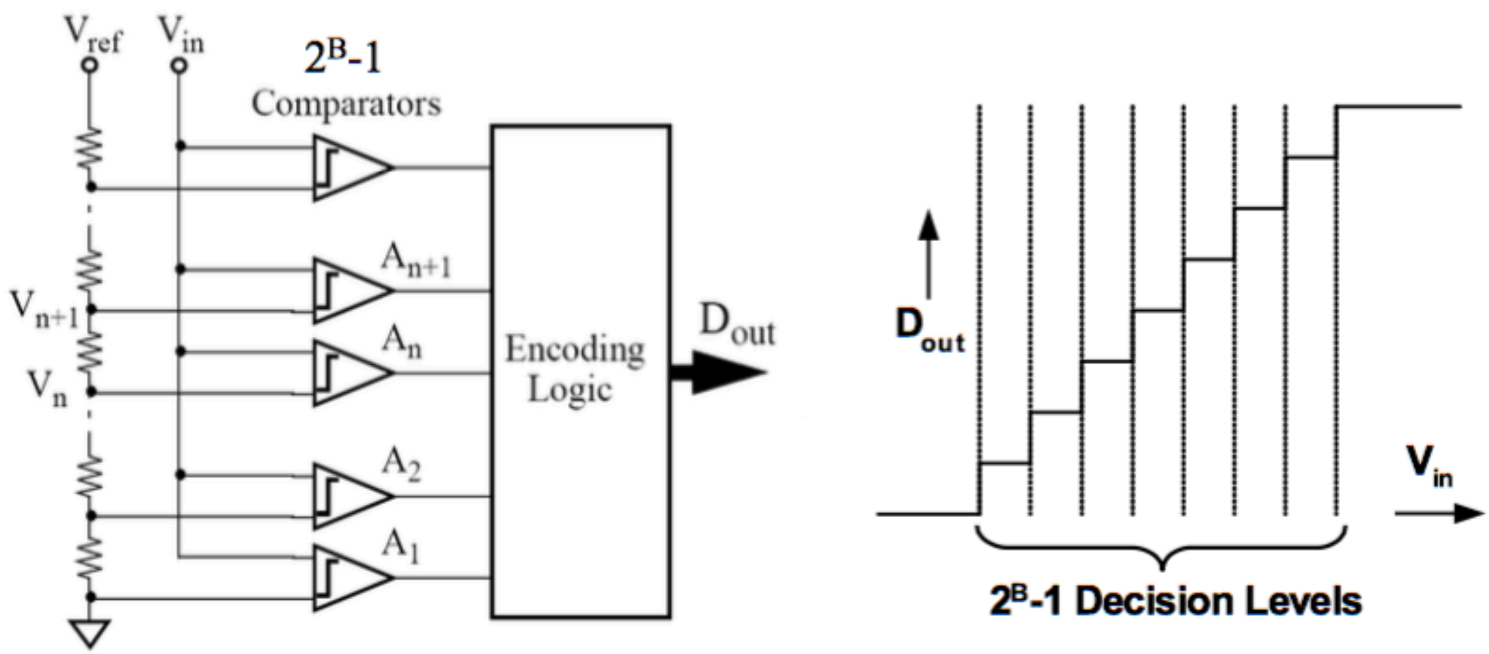
Data: http://www.stanford.edu/~murmann/adcsurvey.html



Flash ADCs

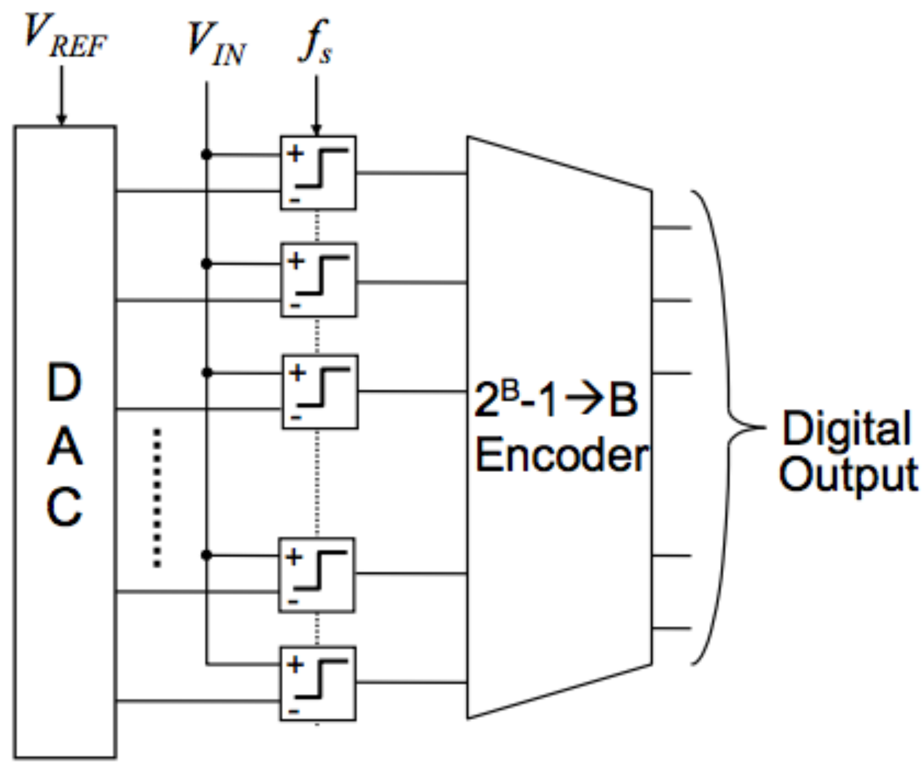
Flash ADC

- Fast
  - Speed limited by single comparator plus encoding logic
- High circuit complexity (2^B-1 comparators), high input capacitance
  - Typically only use for resolution up to 6…8 bits

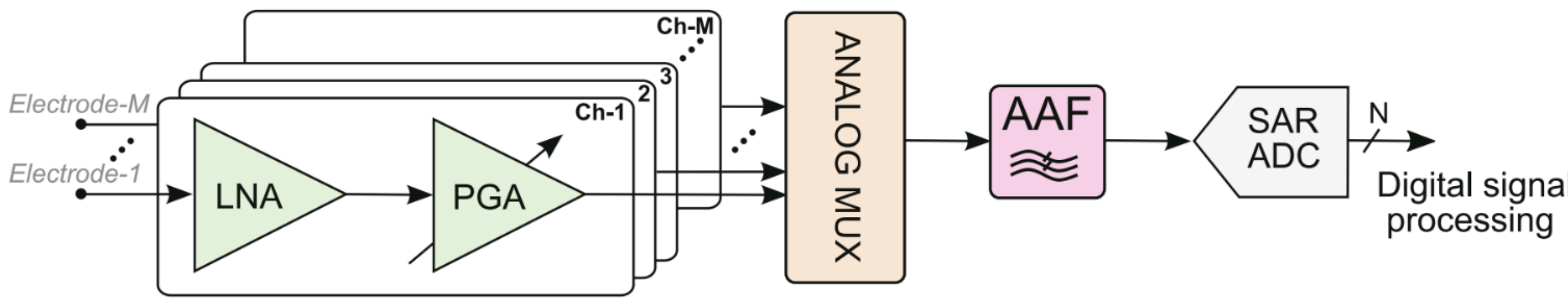


Flash ADC

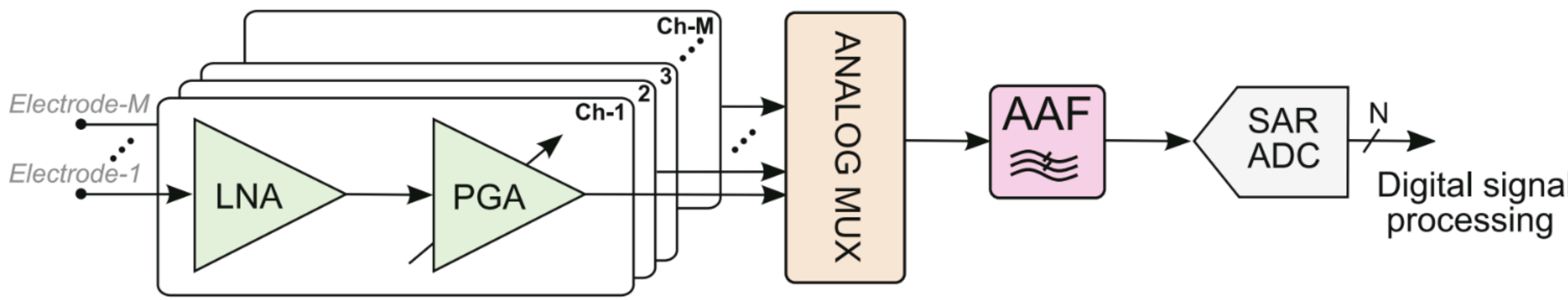
- B-bit flash ADC:
  - DAC generates all possible 2^B-1 levels
  - 2^B-1 comparators compare V_{IN} to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code

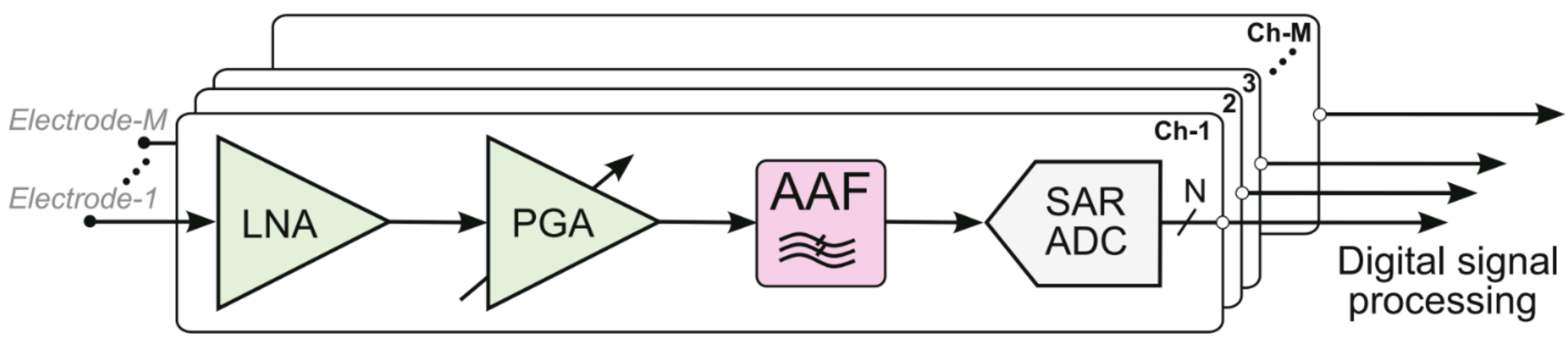


Multi-channel Bio-potential Recording

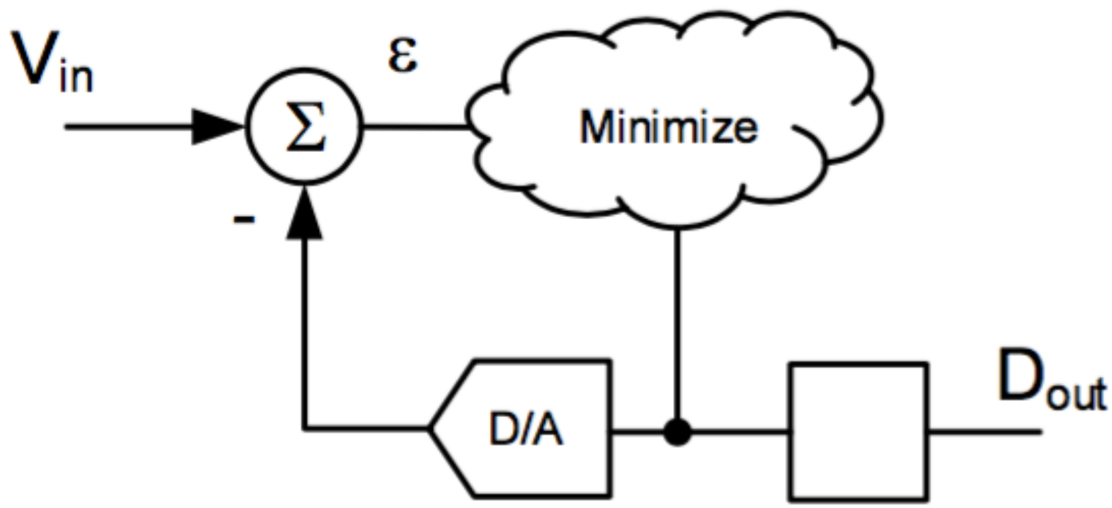


Multi-channel Bio-potential Recording



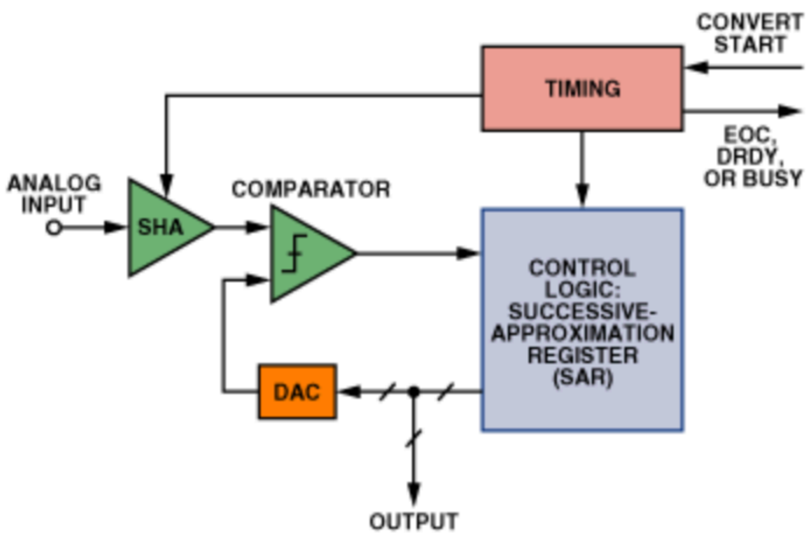


SAR ADC Architectures



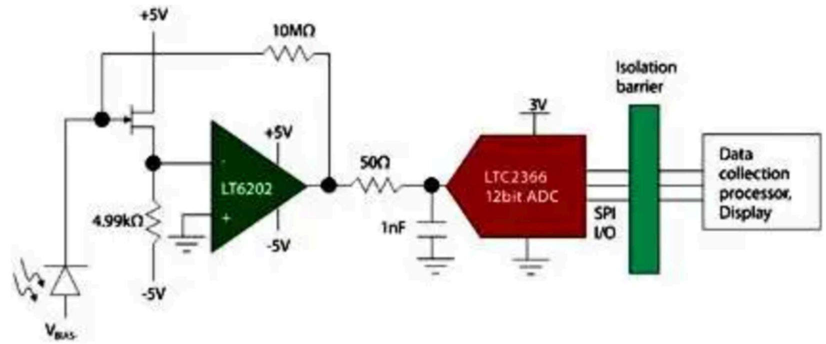
- Most ADC architectures (other than flash) are based on minimizing (reducing) the error between input and a D/A signal approximation
  - Pipeline uses distributed DAC
  - SAR ADC uses comparator to sense error
  - Sigma-delta ADC minimizes error via integration and feedback

SAR ADC



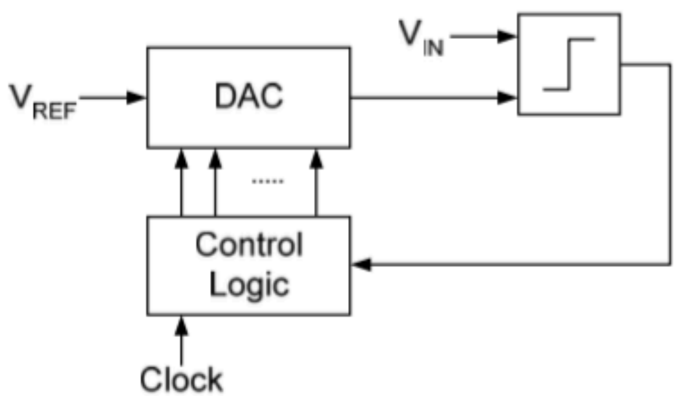
- Key features:
- High resolution
- Fast response and low latency
- Power varies with sample rate

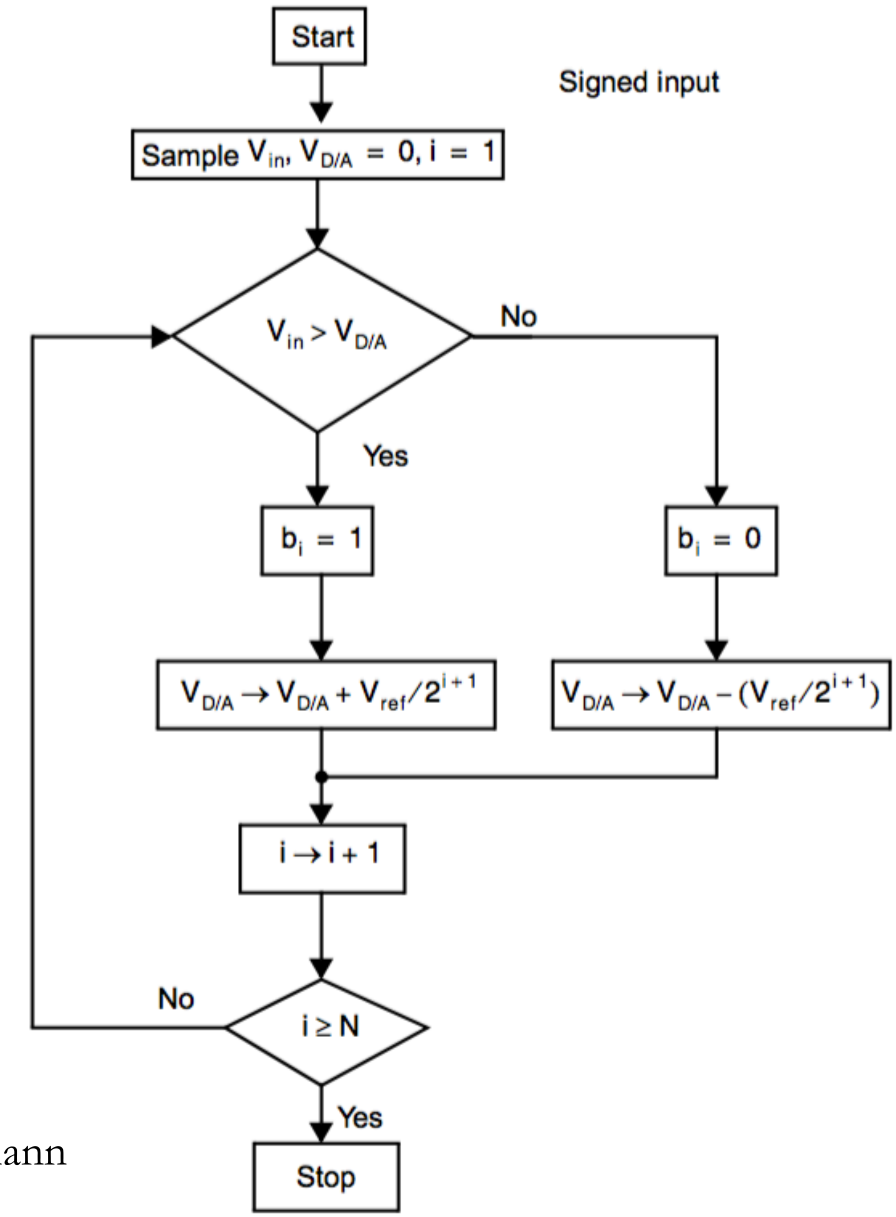
Pulse Oximetry Example



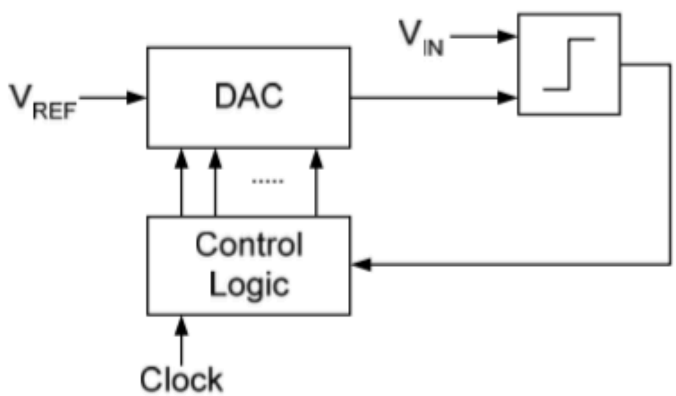
- LTC2366 is part of a family of tiny ADCs sampling from 100KSps to 3MSps
- ADCs dissipate only 7.8mW at 3MSps, 1.5mW at 100KSps and 0.3 microwatts in sleep mode
- LTC2366 features no data latency through the ADC

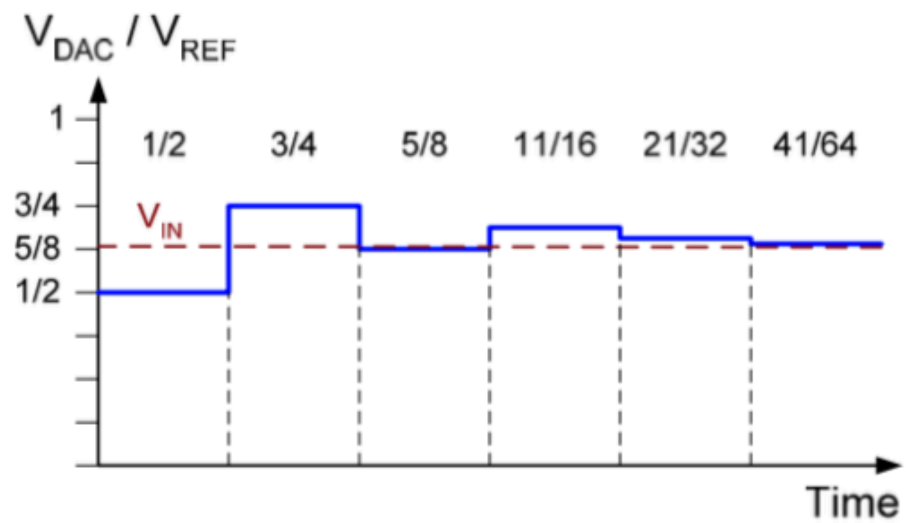
Successive Approximation Algorithm





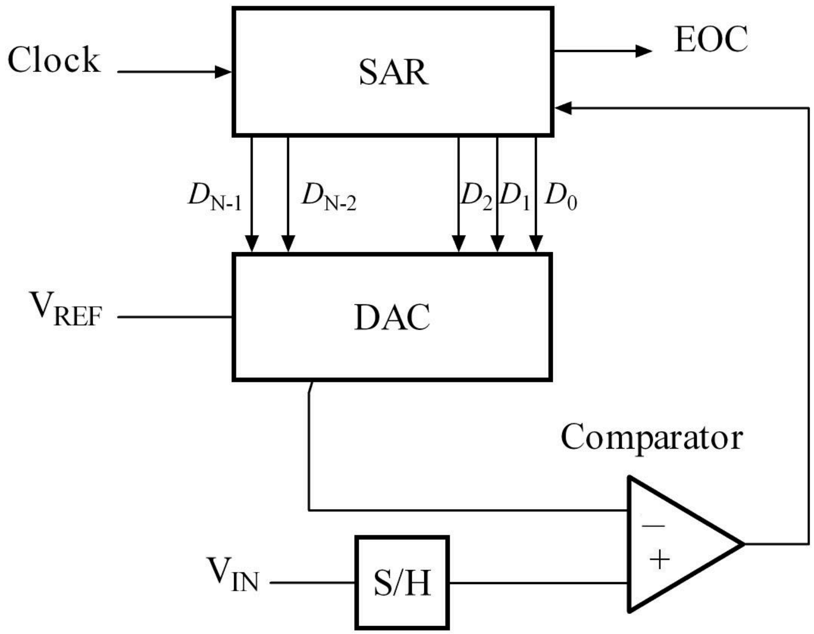
Successive Approximation Register ADC

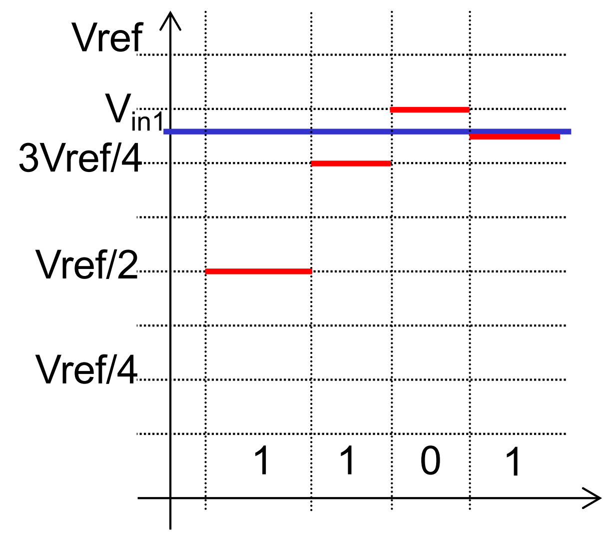




- Binary search over DAC output
- High accuracy achievable (16+ bits)
  - Relies on highly accurate comparator
- Moderate speed (1+ Mhz)

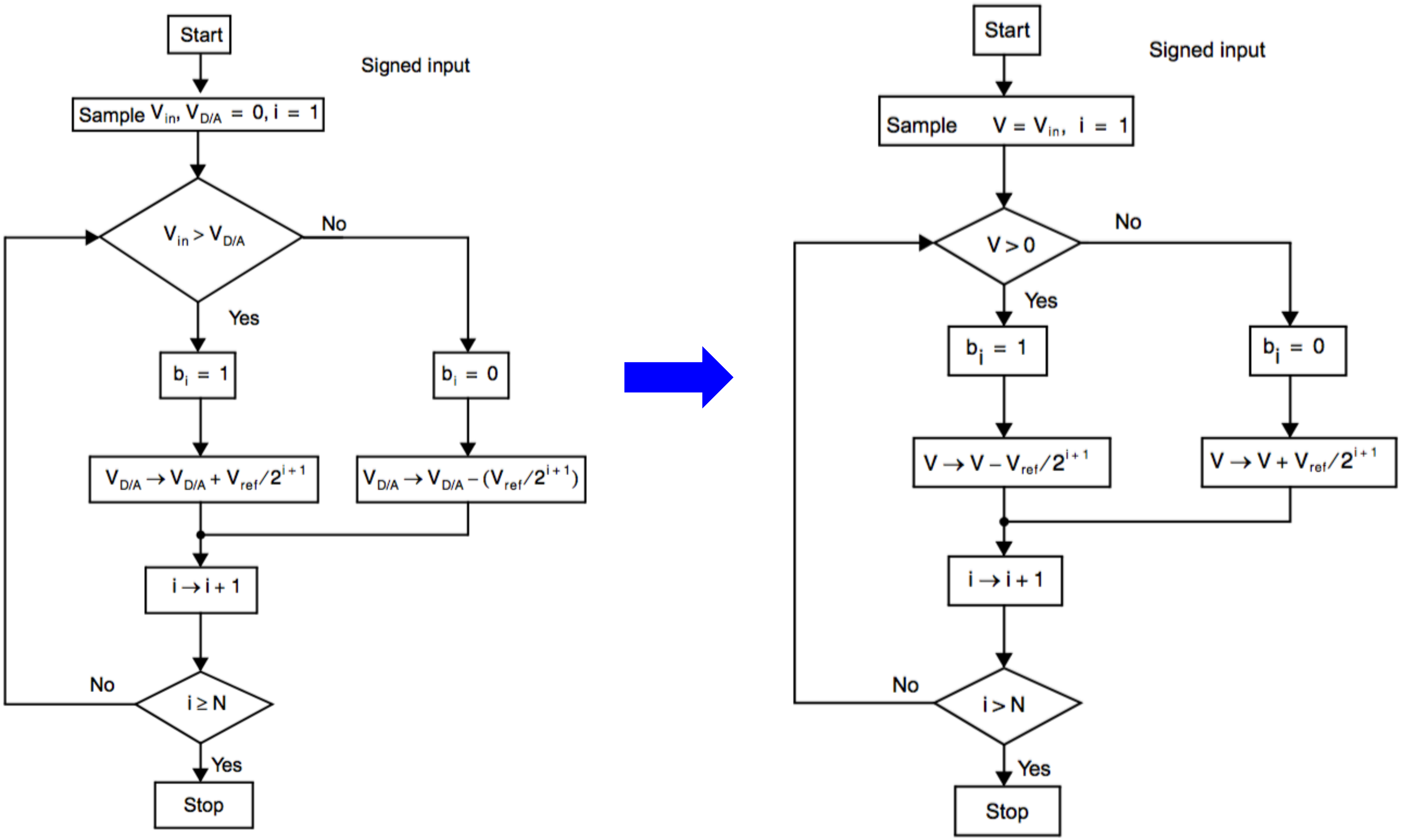
SAR ADC Block Diagram





- Sampling phase: Sample input with Sample-and-Hold
- Bit-cycling: Compare with DAC output, adjusting the SAR with each clock cycle as bits are determined

Charge Redistribution ADC



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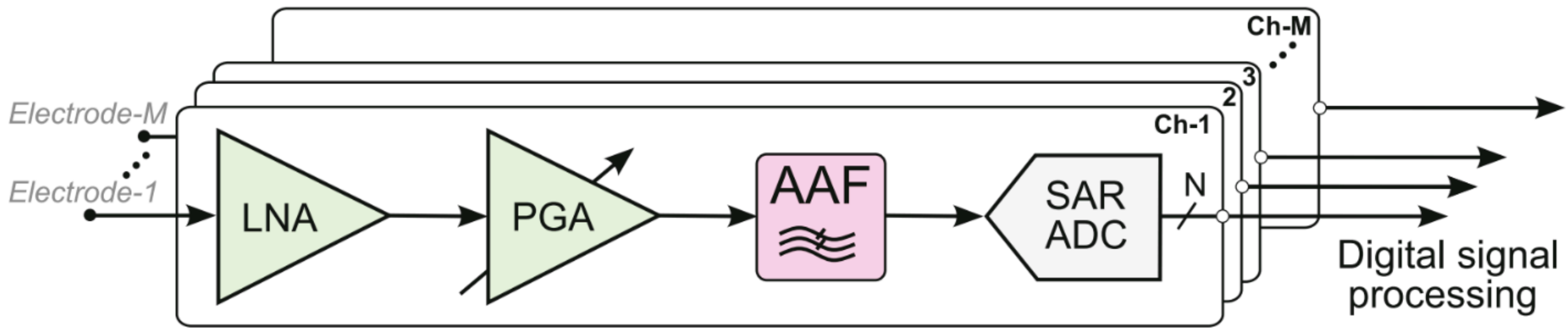

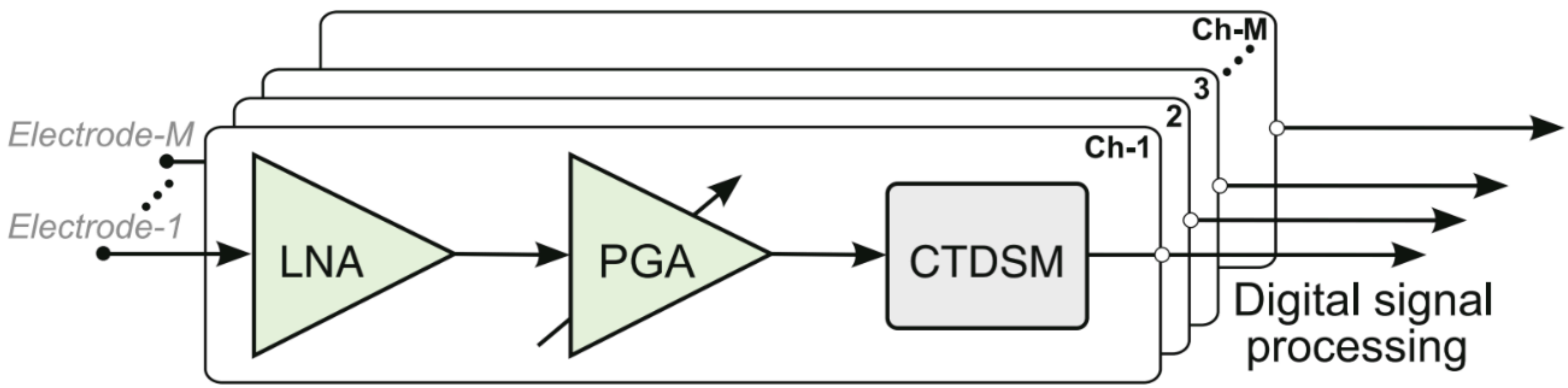

Big Ideas

- SQNR
  - SQNR determined by bit resolution, B
  - ENOB determined by SNR
- Oversampling
  - Enables reduction in quantization noise and reduces stress on AAF. More next lecture…
- Nyquist ADCs
  - Speed vs. SNR tradeoff favors certain architectures for given application
  - Flash ADCs
    - Word-at-a-time for high speed, low resolution applications
  - SAR ADCs
    - Bit-at-a-time for low speed, low power applications
    - Highly suited for medical devices

Admin

- Lab tomorrow
  - More PCB population and testing