# ESE 3400: Medical Devices Lab

Lec 6: October 11, 2023

Data Converters

# Lecture Outline

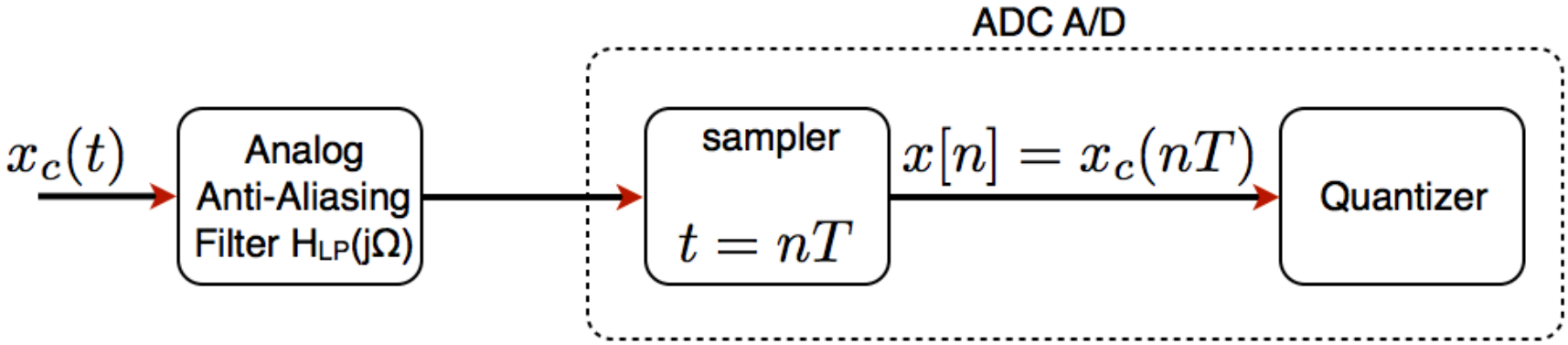
- DTFT vs DFT
- Sampling Examples
- SQNR
- Oversampling
- ADC Architectures
  - Flash ADCs
  - SAR ADCs
  - Delta-Sigma ADCs

# ADC

Analog to Digital Converter

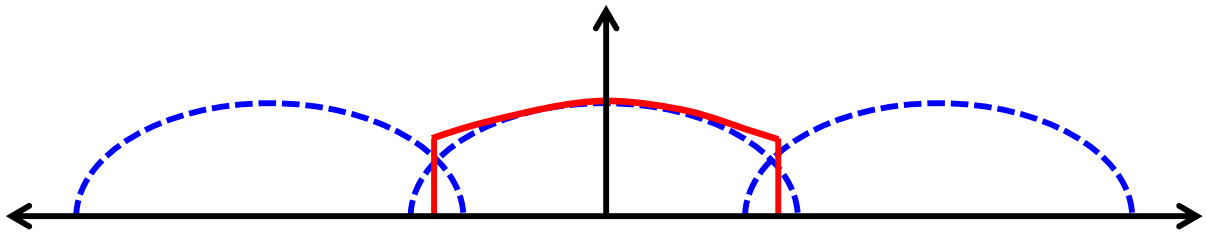
Penn

# Anti-Aliasing Filter with ADC



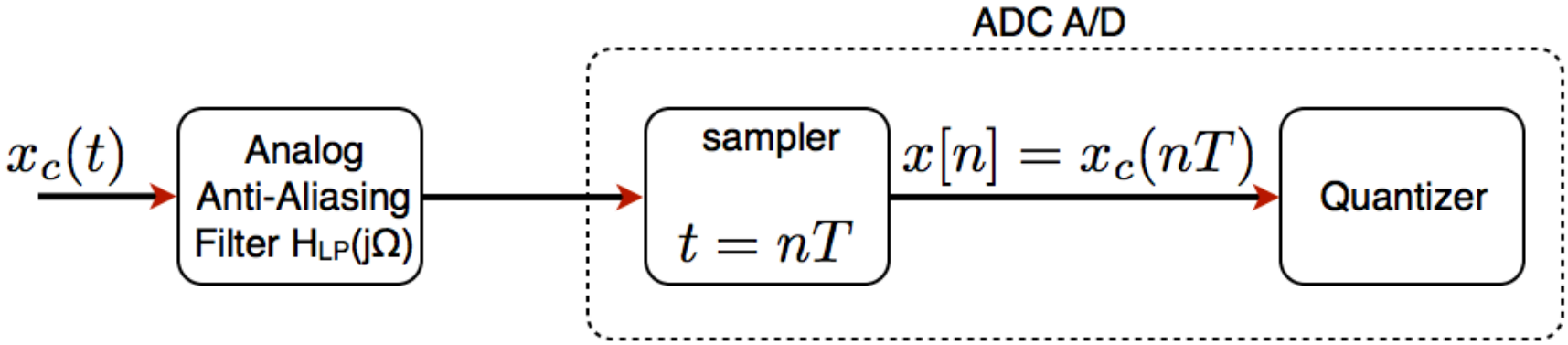
# Aliasing

- If $\Omega_N > \Omega_s/2$, $x_r(t)$ an aliased version of $x_c(t)$

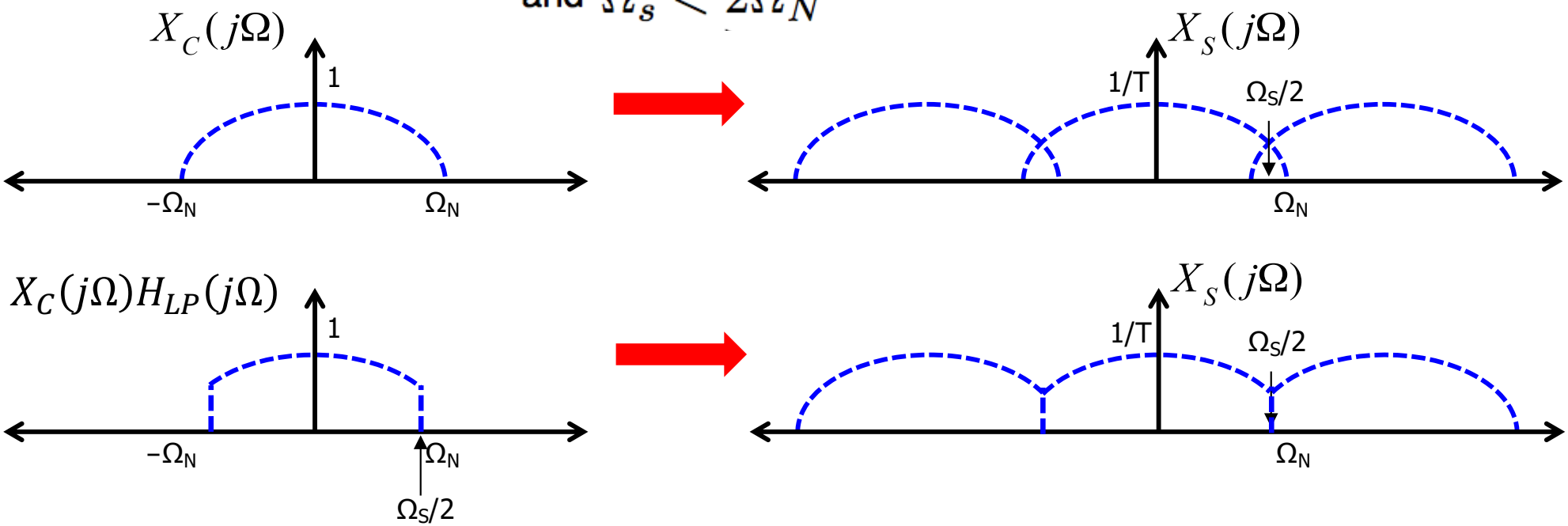


$$X_r(j\Omega) = \begin{cases} TX_s(j\Omega) & \text{if} \quad |\Omega| \leq \Omega_s/2 \\ 0 & \text{otherwise} \end{cases}$$

# Anti-Aliasing Filter with ADC




and $\Omega_s < 2\Omega_N$



# DTFT Vs. DFT

DTFT:

$$X(e^{j\omega}) = \sum_{k=-\infty}^{\infty} x[k]e^{-j\omega k}$$

$$x[n] = \frac{1}{2\pi}\int_{-\pi}^{\pi} X(e^{j\omega})e^{j\omega n}d\omega$$

DFT:

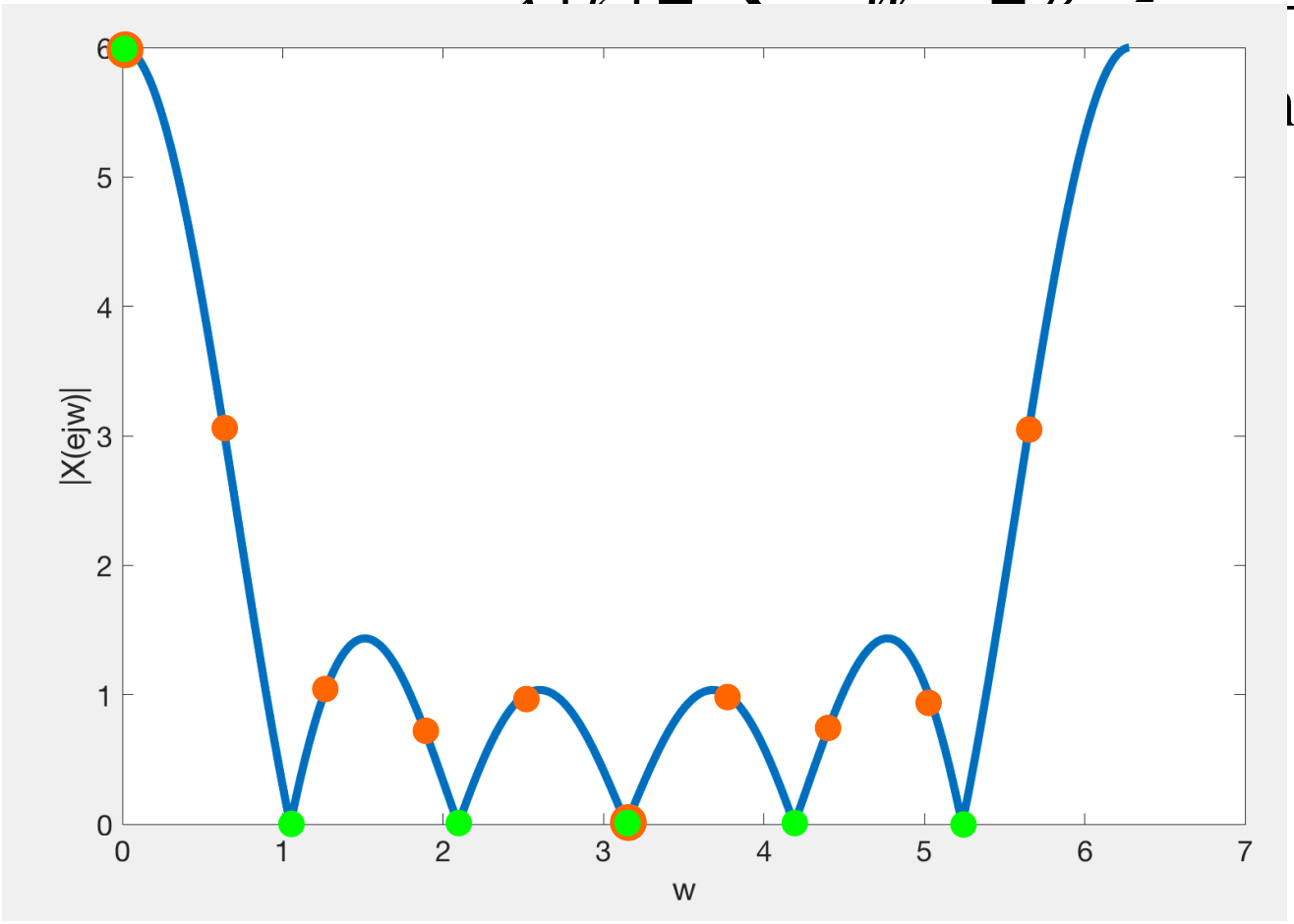
$$x[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k]W_N^{-kn}$$

$$X[k] = \sum_{n=0}^{N-1} x[n]W_N^{kn}$$

# DFT vs DTFT

- Back to example

$$X[k] = \sum^{5} W^{nk} = e^{-j\frac{\pi}{2}k} \frac{\sin\left(\frac{3\pi}{5}k\right)}{\sin\left(\frac{\pi}{10}k\right)}$$

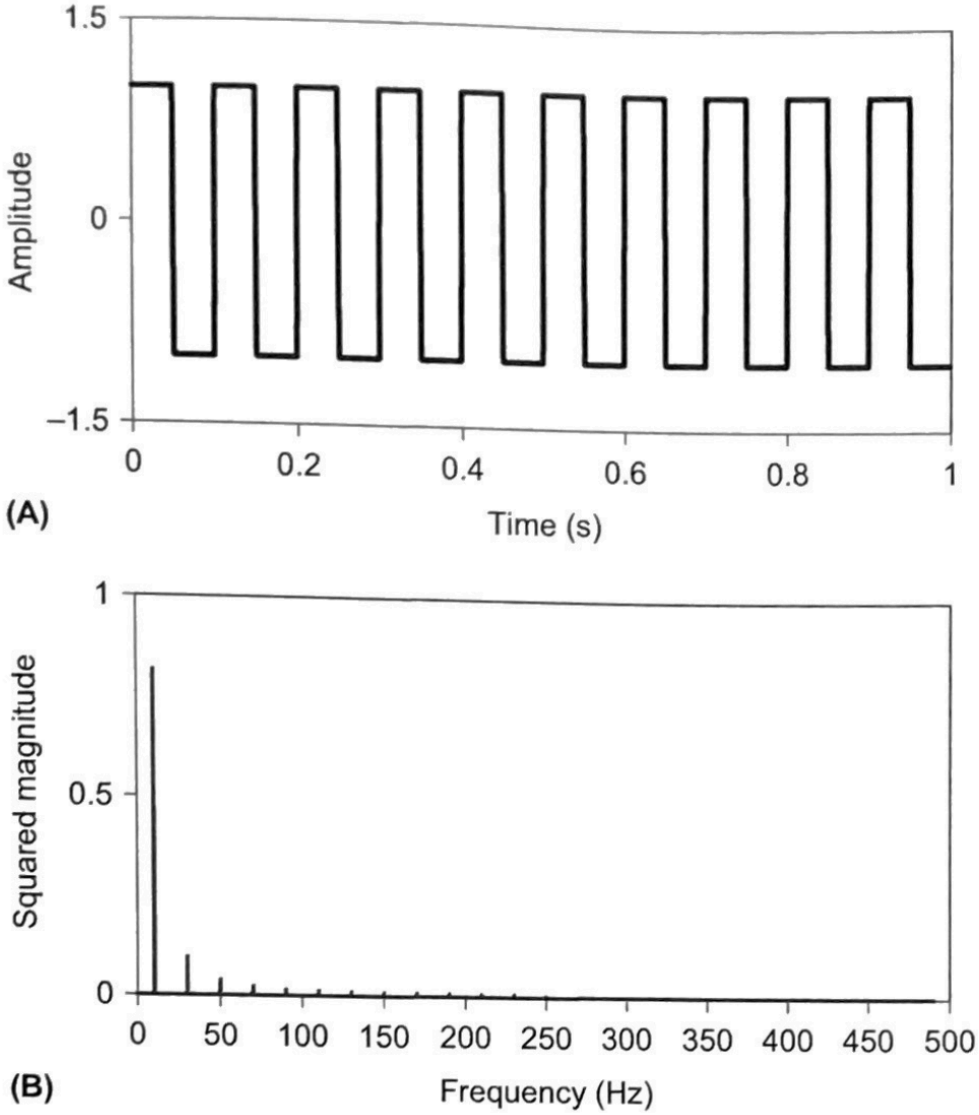



"6-point" DFT

"10-point" DFT

Use `fftshift` to center around dc

# Sampling/Reconstruction Example



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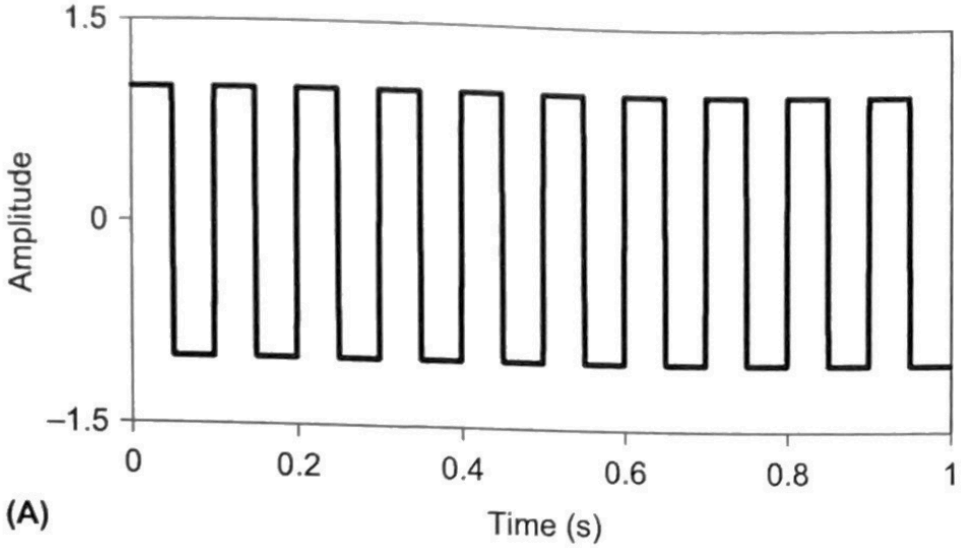


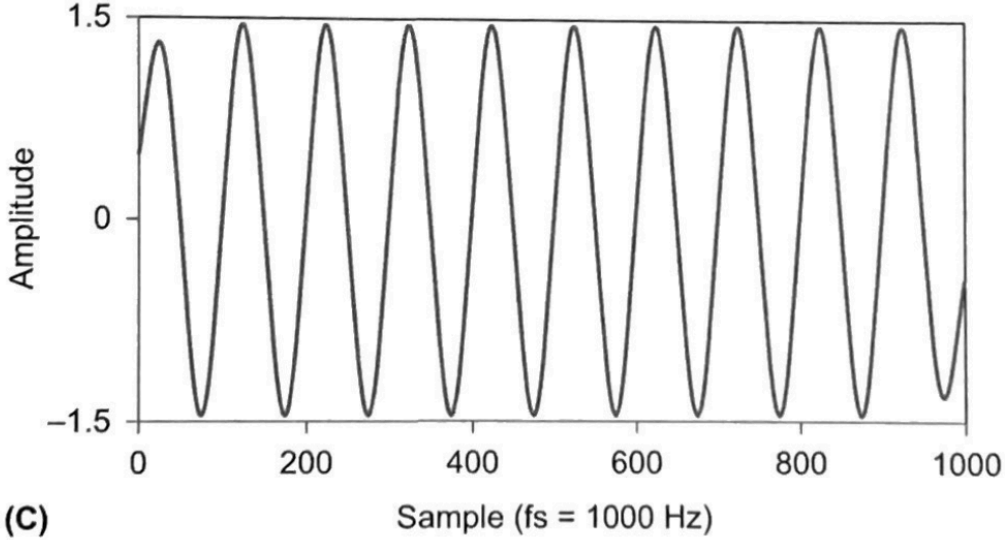


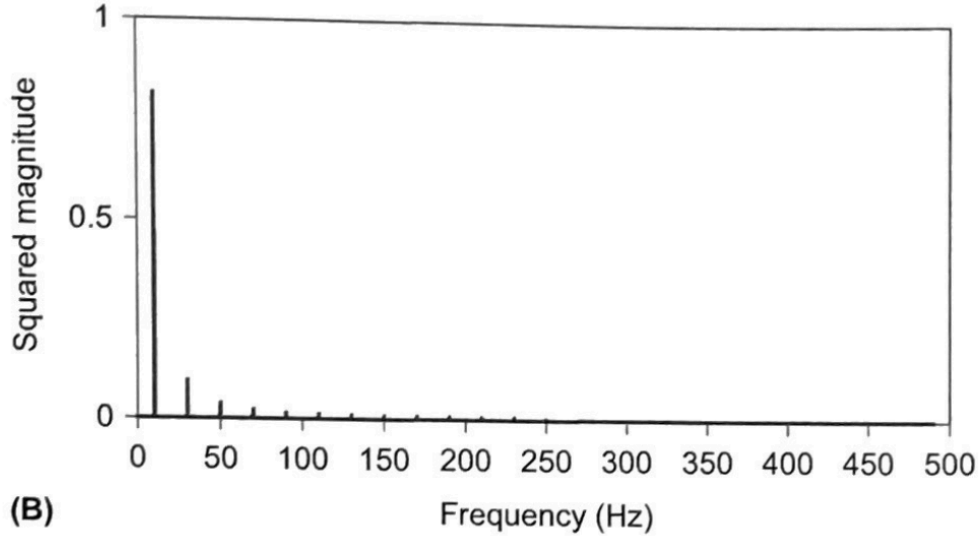

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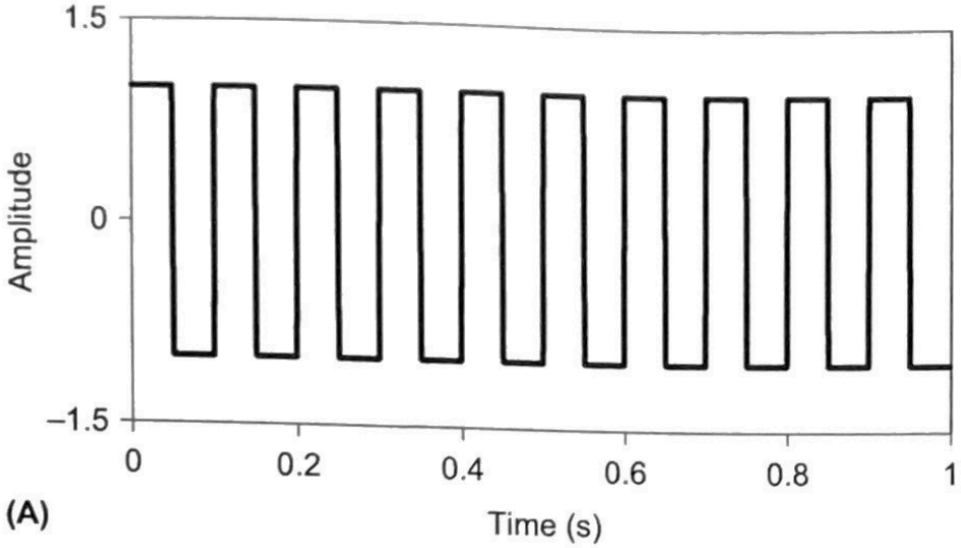
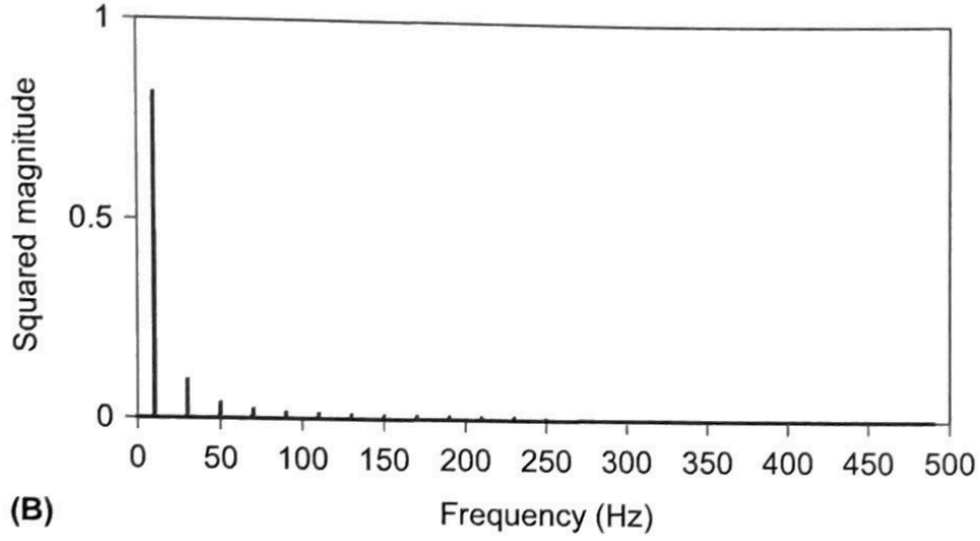
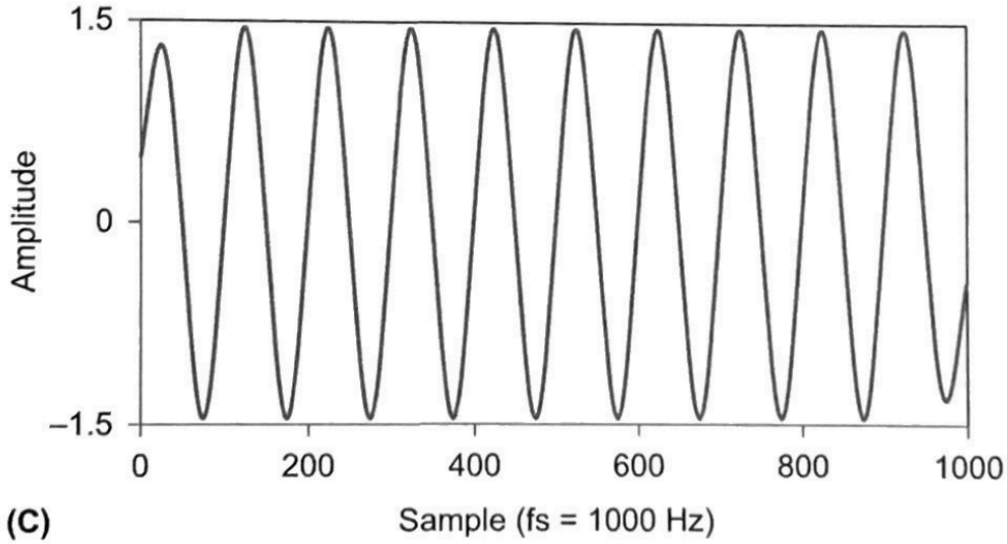
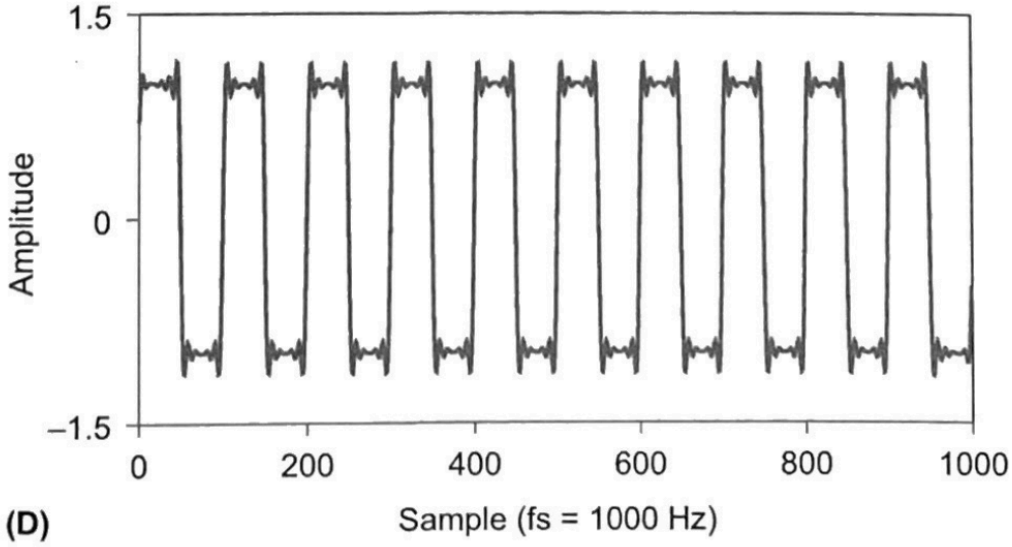
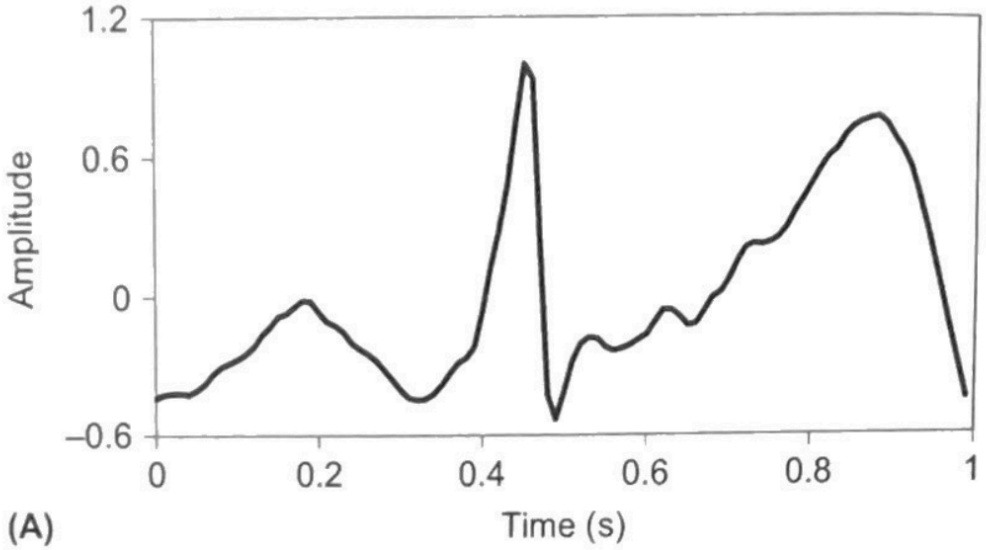


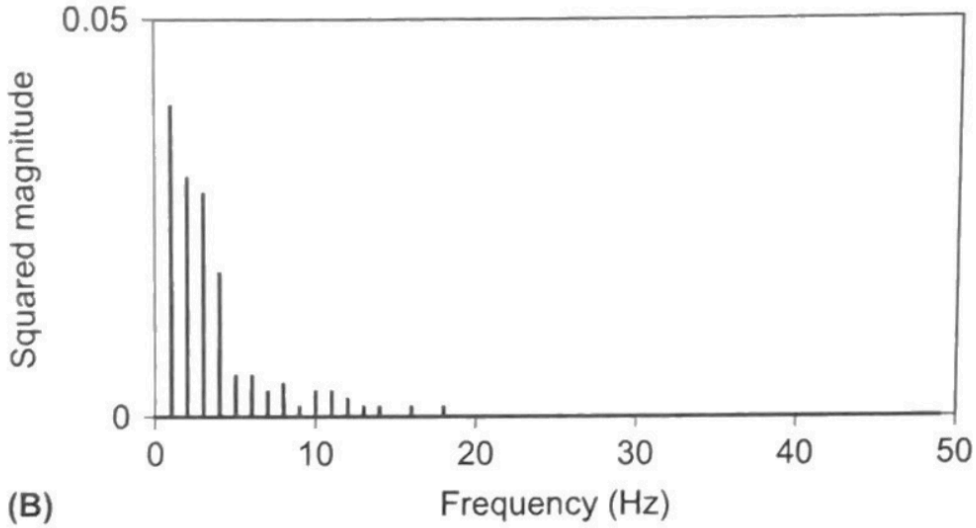



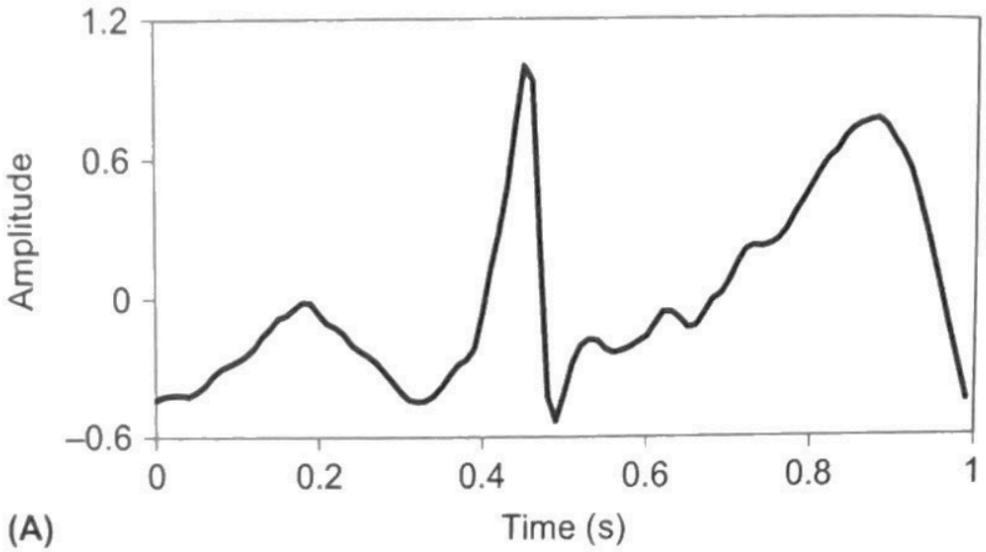



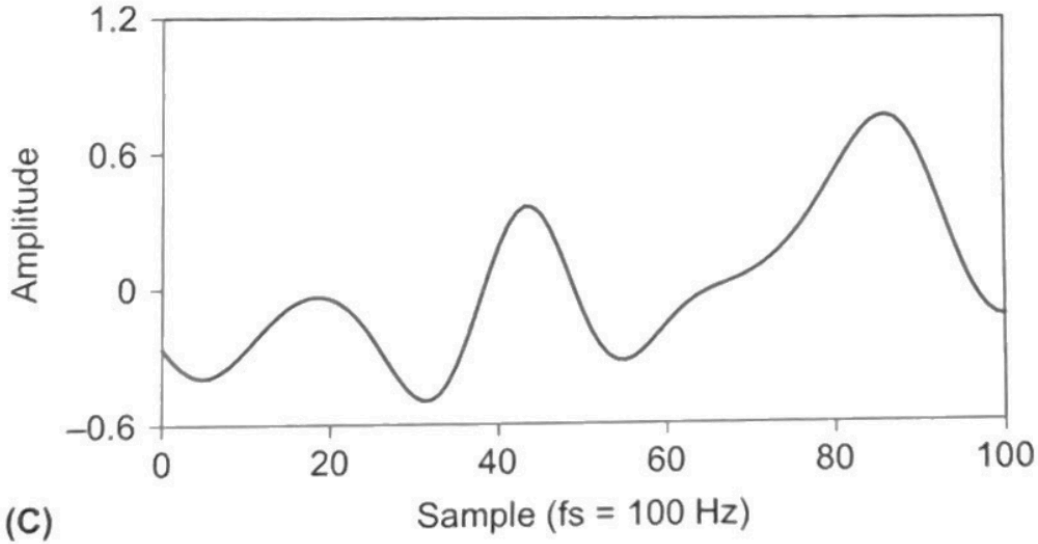
# ECG Example

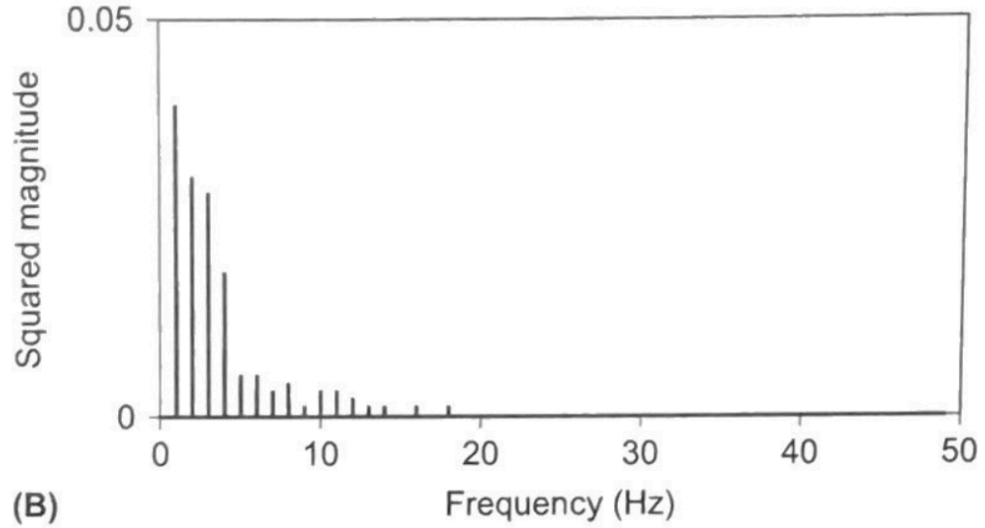

1.2
0.6
0
–0.6
Amplitude
0
0.2
0.4
0.6
0.8
1
Time (s)
(A)


0.05
0
Squared magnitude
0
10
20
30
40
50
Frequency (Hz)
(B)

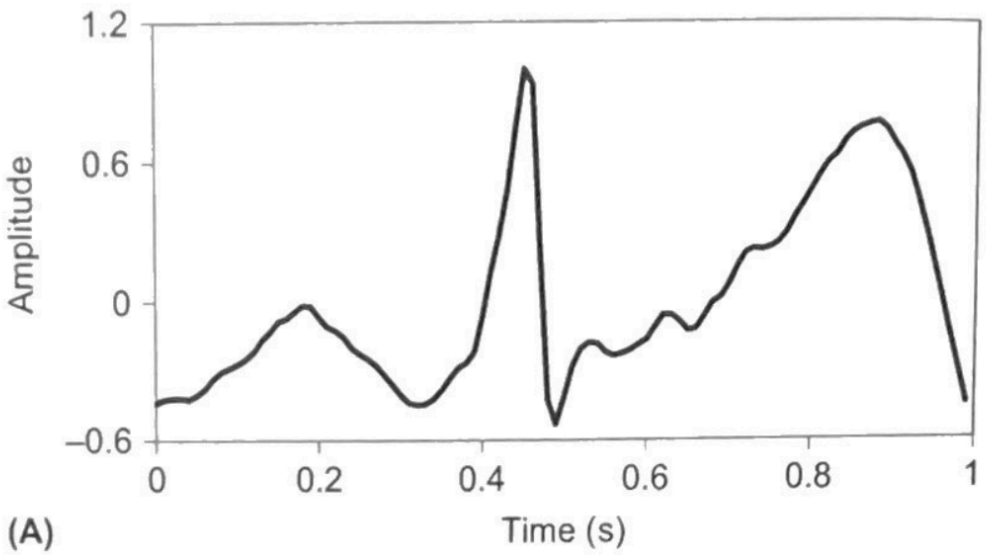
# ECG Example

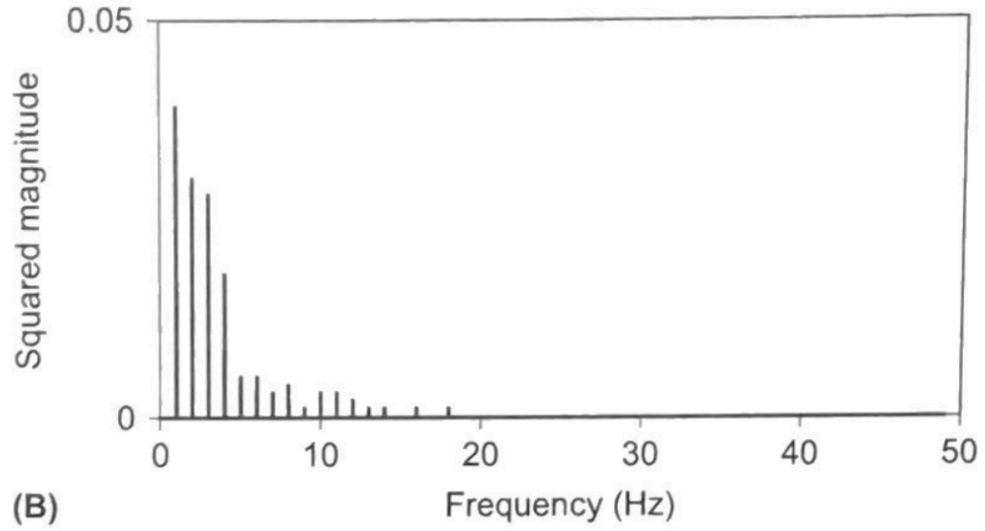

1.2
0.6
0
−0.6
Amplitude
0
0.2
0.4
0.6
0.8
1
Time (s)
(A)

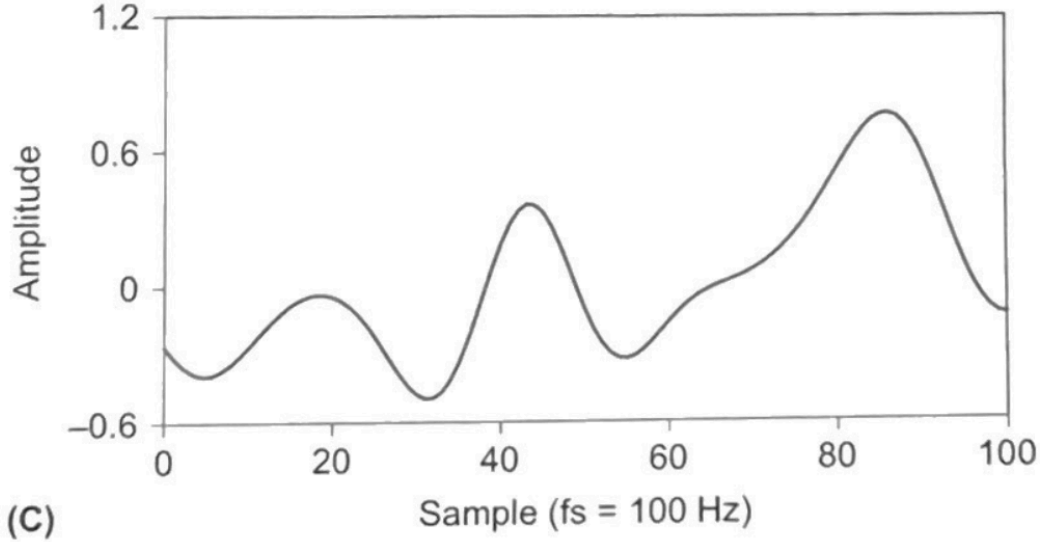

1.2
0.6
0
−0.6
Amplitude
0
20
40
60
80
100
Sample (fs = 100 Hz)
(C)

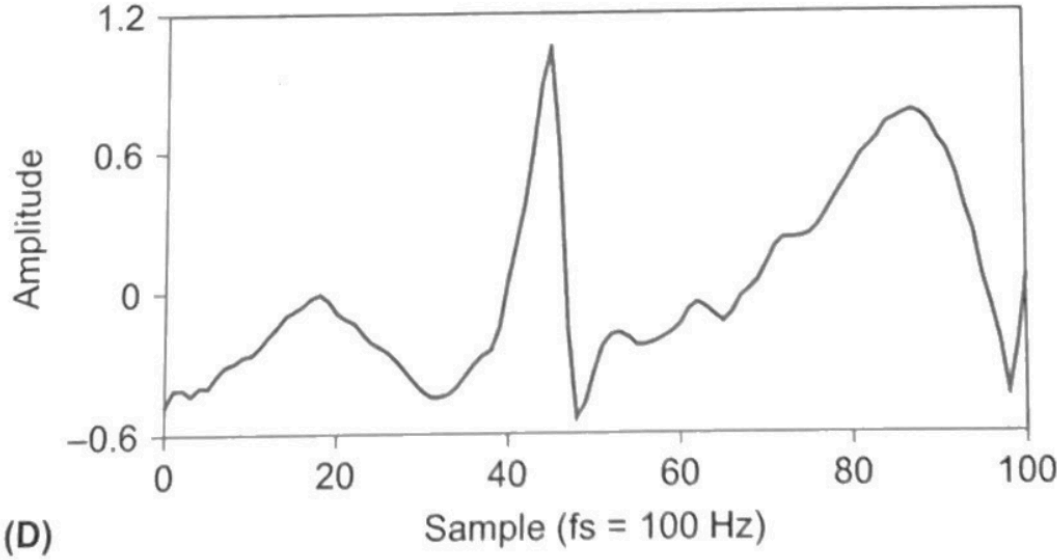

0.05
0
Squared magnitude
0
10
20
30
40
50
Frequency (Hz)
(B)

# ECG Example

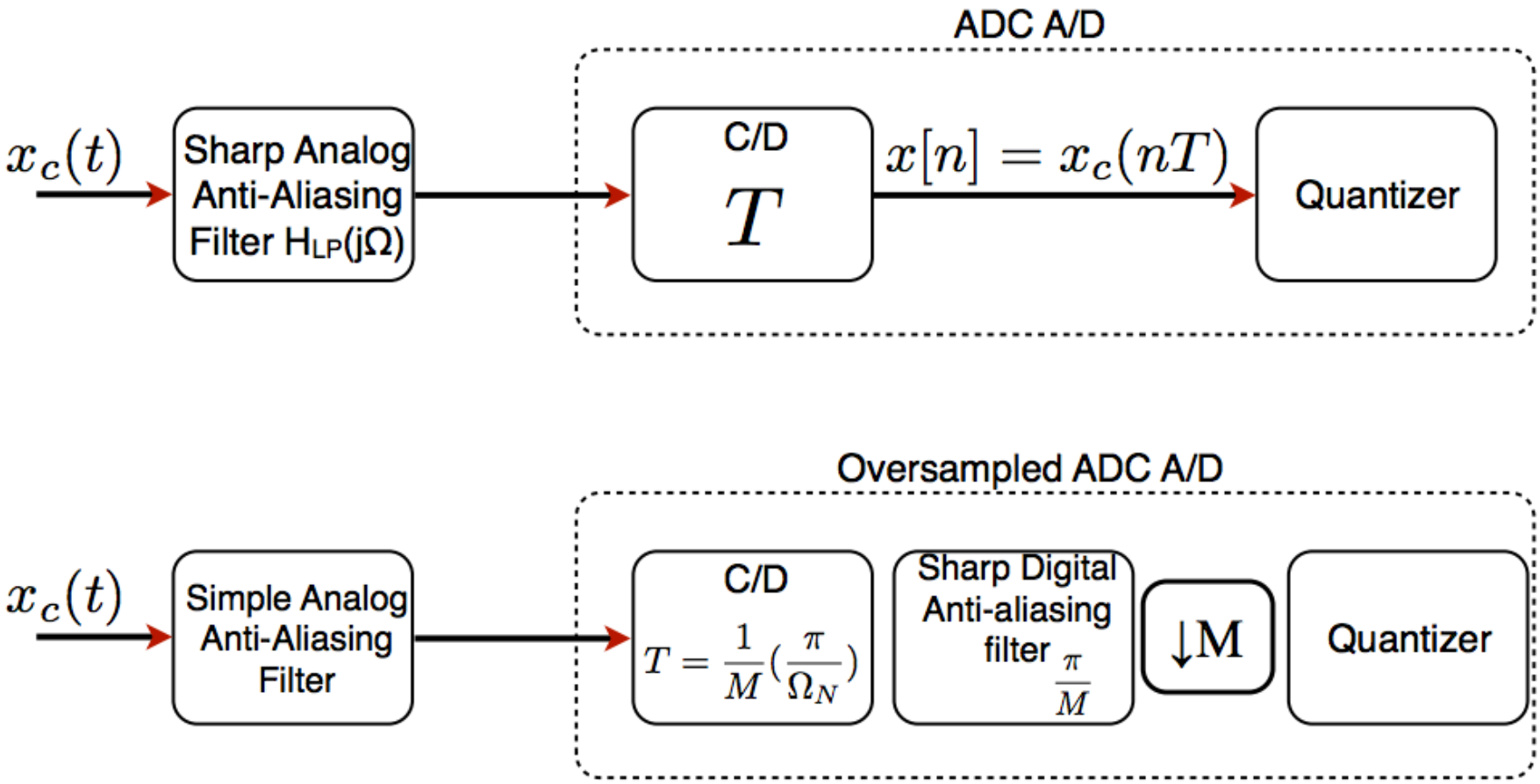

1.2
0.6
0
−0.6
Amplitude
0
0.2
0.4
0.6
0.8
1
Time (s)
(A)


0.05
0
Squared magnitude
0
10
20
30
40
50
Frequency (Hz)
(B)

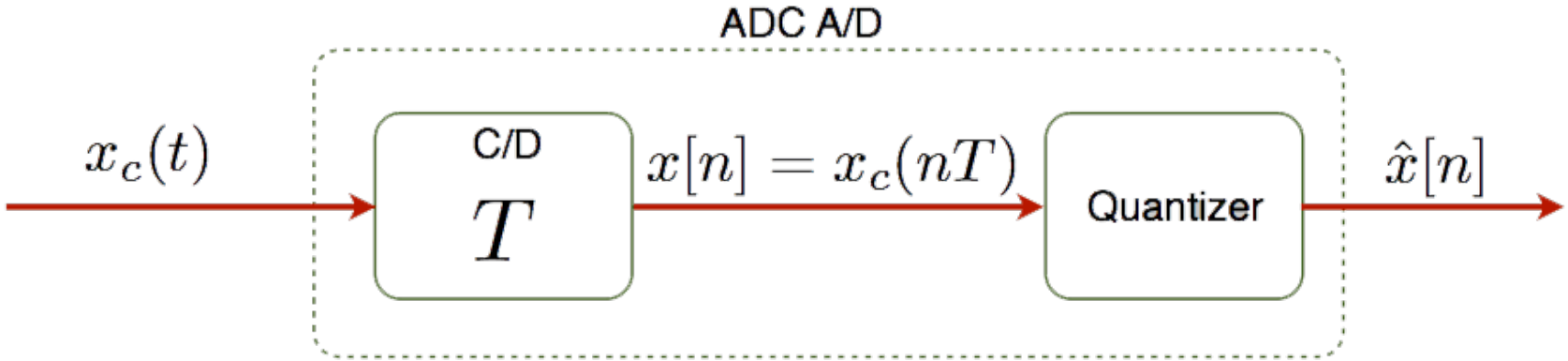

1.2
0.6
0
−0.6
Amplitude
0
20
40
60
80
100
Sample (fs = 100 Hz)
(C)

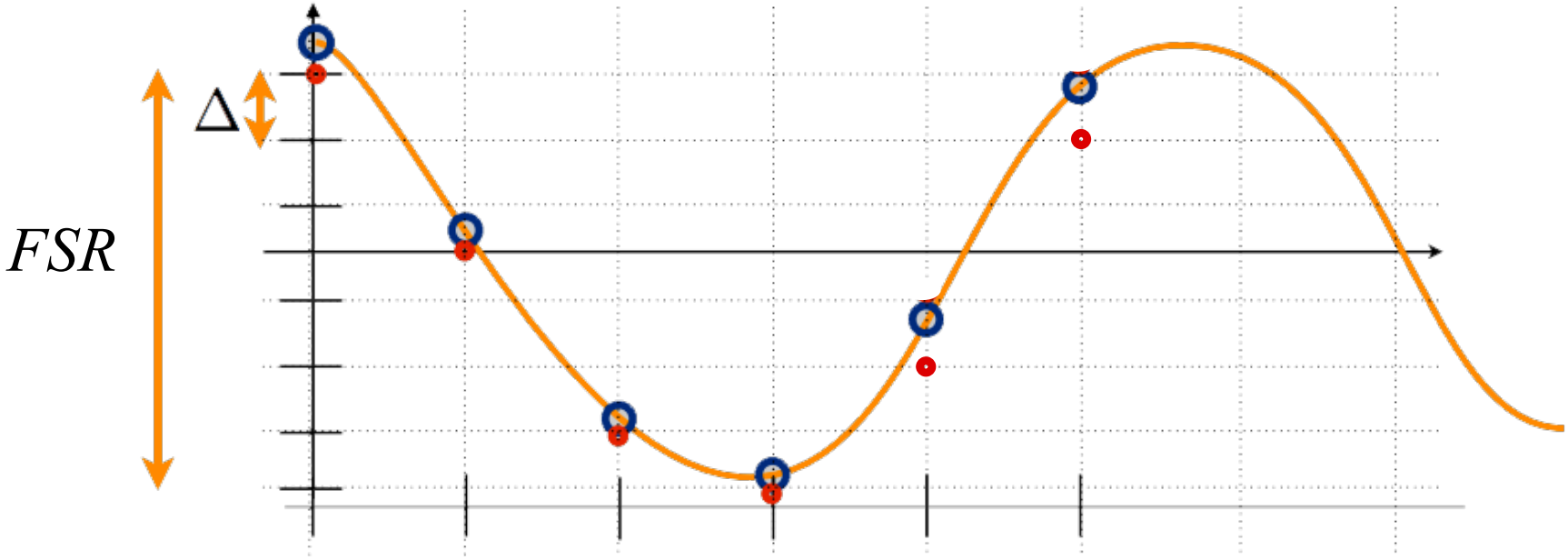

1.2
0.6
0
−0.6
Amplitude
0
20
40
60
80
100
Sample (fs = 100 Hz)
(D)

# Oversampled ADC



# Sampling and Quantization

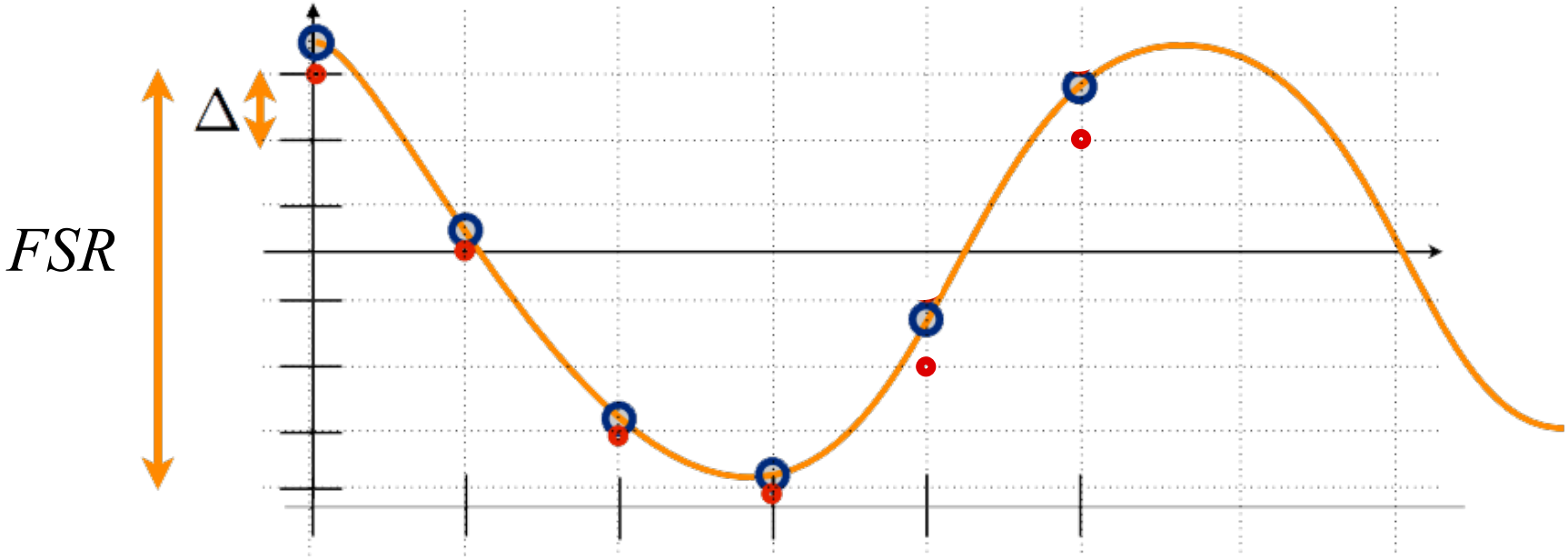


# Sampling and Quantization

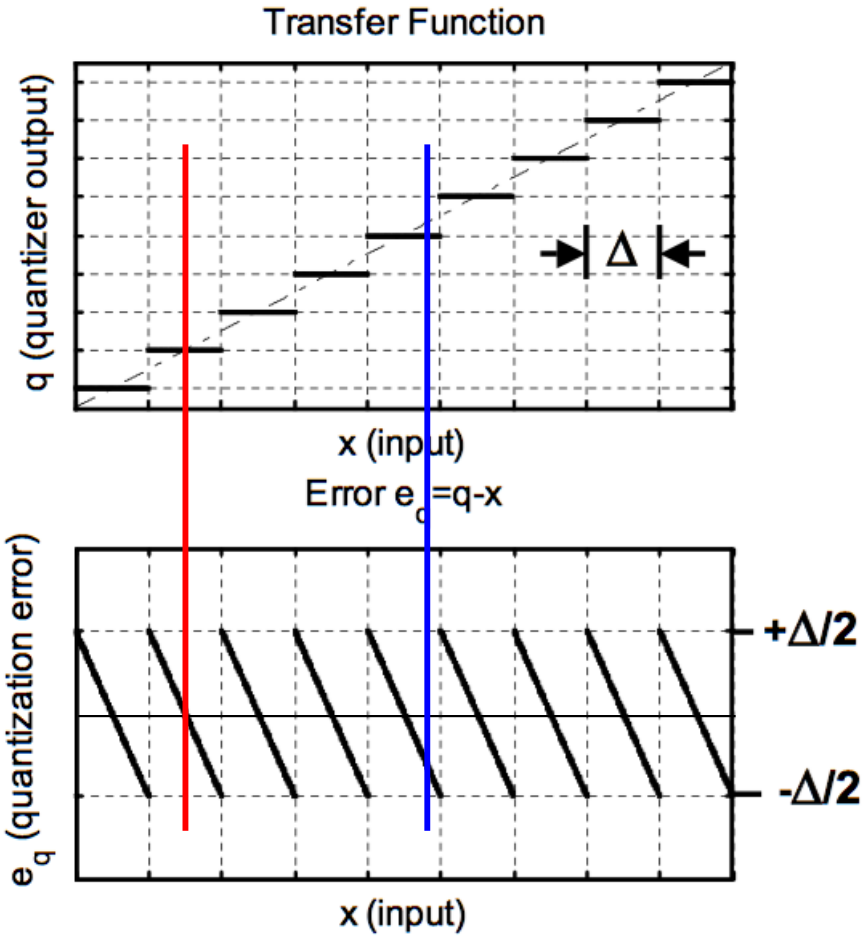
- For an input signal with $V_{pp}$=FSR with B bits

$$\Delta = \frac{FSR}{2^B}$$



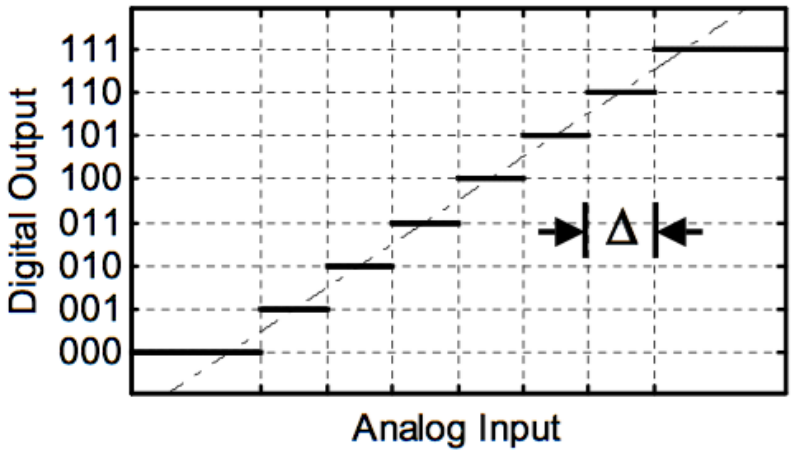
# Ideal Quantizer

- Quantization step Δ
- Quantization error has sawtooth shape
  - Bounded by –Δ/2, +Δ/2
- Ideally infinite input range and infinite number of quantization levels

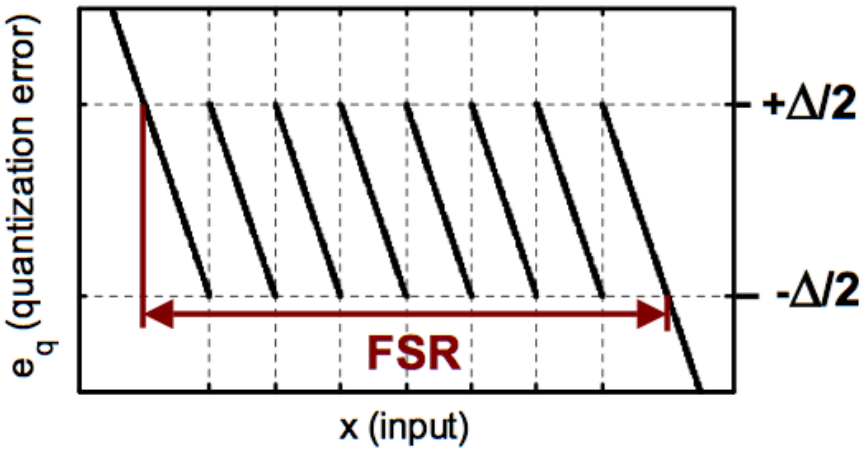


# Ideal B-bit Quantizer

- Practical quantizers have a limited input range and a finite set of output codes
- E.g. a 3-bit quantizer can map onto $2^3$=8 distinct output codes




- Quantization error grows out of bounds beyond code boundaries
- We define the full scale range (FSR) as the maximum input range that satisfies $|e_q| \leq \Delta/2$
  - Implies that FSR = $2^B \cdot \Delta$

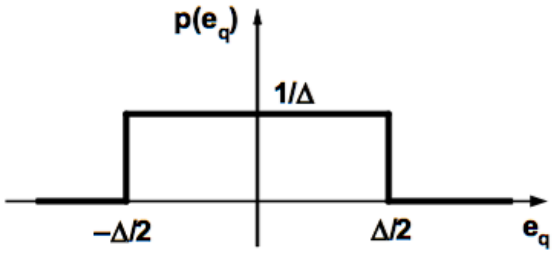


# Effect of Quantization Error on Signal

- Quantization error is a deterministic function of the signal
  - Consequently, the effect of quantization strongly depends on the signal itself
- Unless, we consider fairly trivial signals, a deterministic analysis is usually impractical
  - More common to look at errors from a statistical perspective
  - "Quantization noise"

# Quantization Error Statistics

- Crude assumption: $e_q(x)$ has uniform probability density
- This approximation holds reasonably well in practice when
  - Signal spans large number of quantization steps
  - Signal is "sufficiently active"
  - Quantizer does not overload

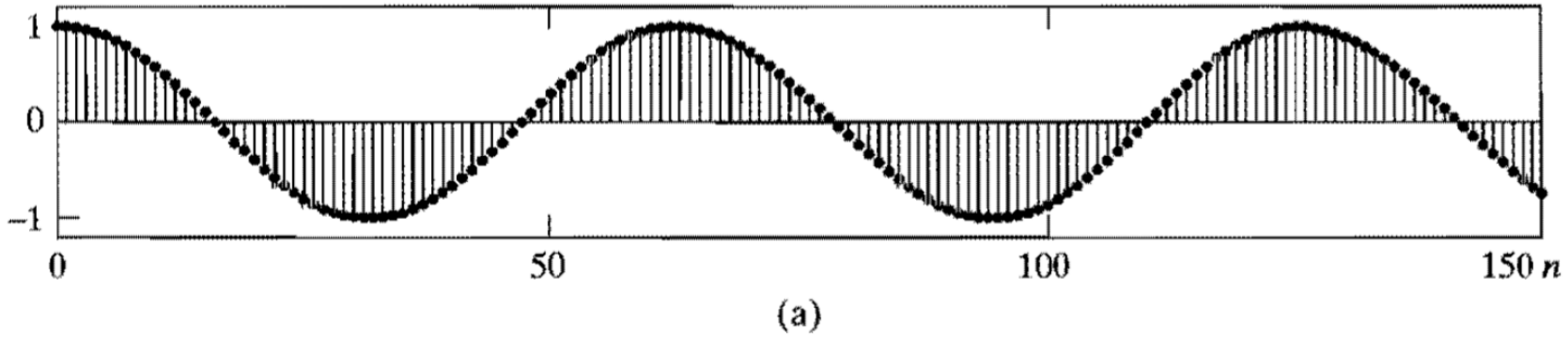



**Mean** $\bar{e} = \int_{-\Delta/2}^{+\Delta/2} \frac{e}{\Delta} de = 0$

**Variance** $\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12}$

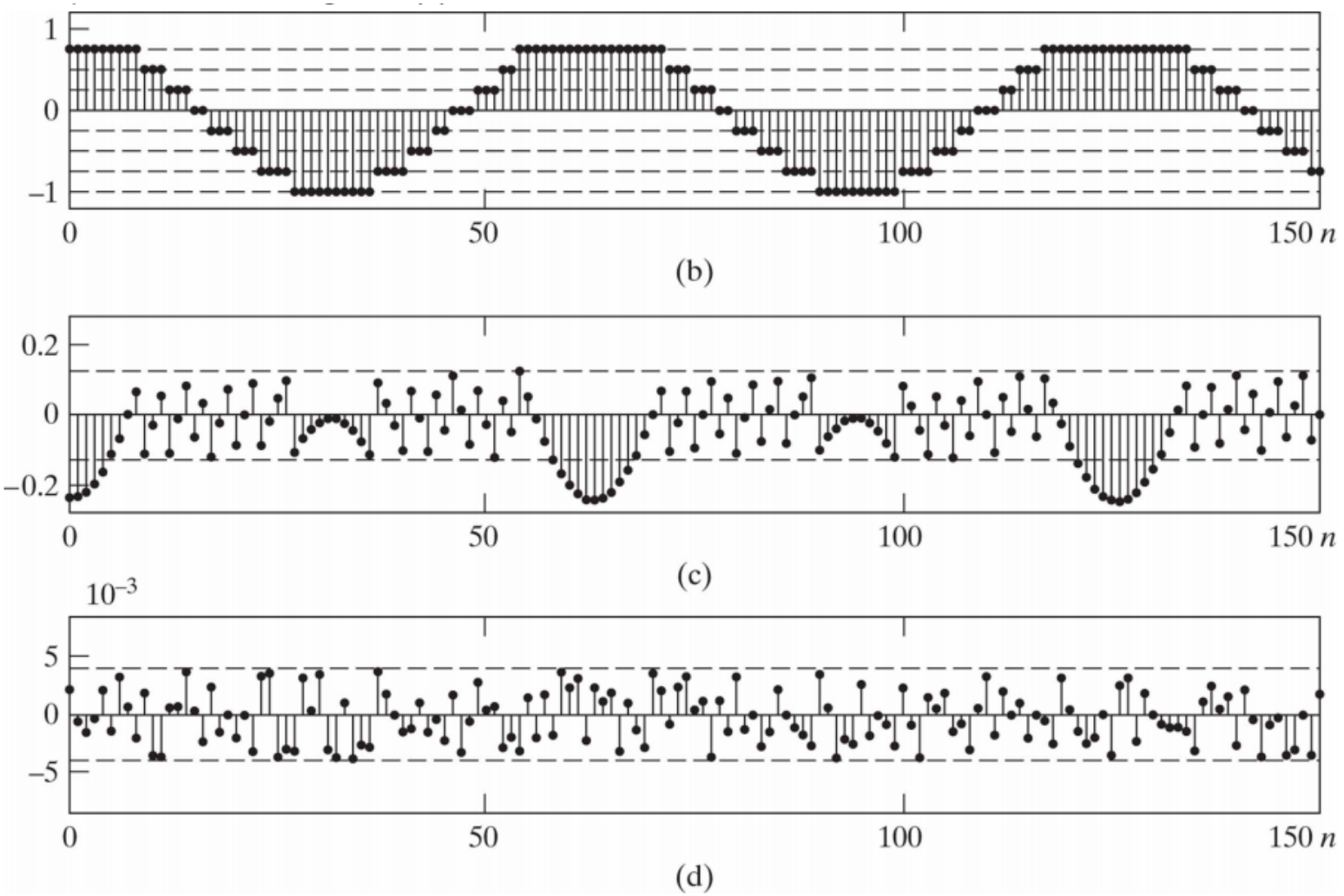
# Quantization Noise

- **Figure 4.57** Example of quantization noise. (a) Unquantized samples of the signal x[n] = 0.99cos(n/10).



# Quantization Noise

- **Figure 4.57**(continued) (b) Quantized samples of the cosine waveform in part (a) with a 3-bit quantizer. (c) Quantization error sequence for 3-bit quantization of the signal in (a). (d) Quantization error sequence for 8-bit quantization of the signal in (a).



# Signal-to-Quantization-Noise Ratio

- Assuming full-scale sinusoidal input, we have

$$SNR_Q = 6.02B + 1.76 \text{ dB}$$

| B (Number of Bits) | SQNR |
|---|---|
| 8 | 50dB |
| 12 | 74dB |
| 16 | 98dB |
| 20 | 122dB |

# Signal-to-Quantization-Noise Ratio

- For uniform B bits quantizer

$$SNR_Q = 10 \log_{10} \left( \frac{\sigma_x^2}{\sigma_e^2} \right)$$

# Signal-to-Quantization-Noise Ratio

- For uniform B bits quantizer

$$SNR_Q = 10\log_{10}\left(\frac{\sigma_x^2}{\sigma_e^2}\right)$$

$$= 10\log_{10}\left(\frac{12\cdot 2^{2B}\sigma_x^2}{FSR^2}\right)$$

$$\mathrm{SNR}_Q = 6.02B + 10.8 - 20\log_{10}\left(\frac{FSR}{\sigma_x}\right)$$

Quantizer range

rms of amp

# Signal-to-Quantization-Noise Ratio

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$$\mathrm{SNR}_Q = 6.02B + 10.8 - 20\log_{10}\left(\frac{FSR}{\sigma_x}\right)$$

Quantizer range

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# Signal-to-Quantization-Noise Ratio

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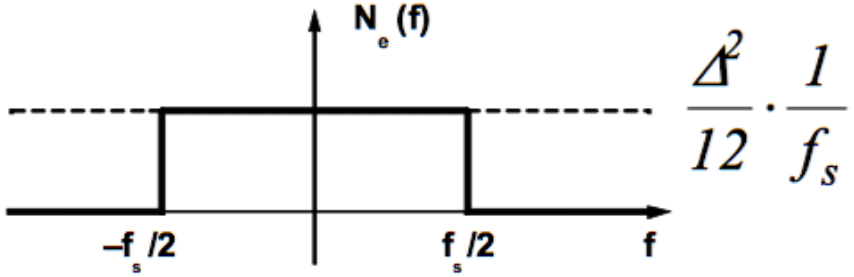
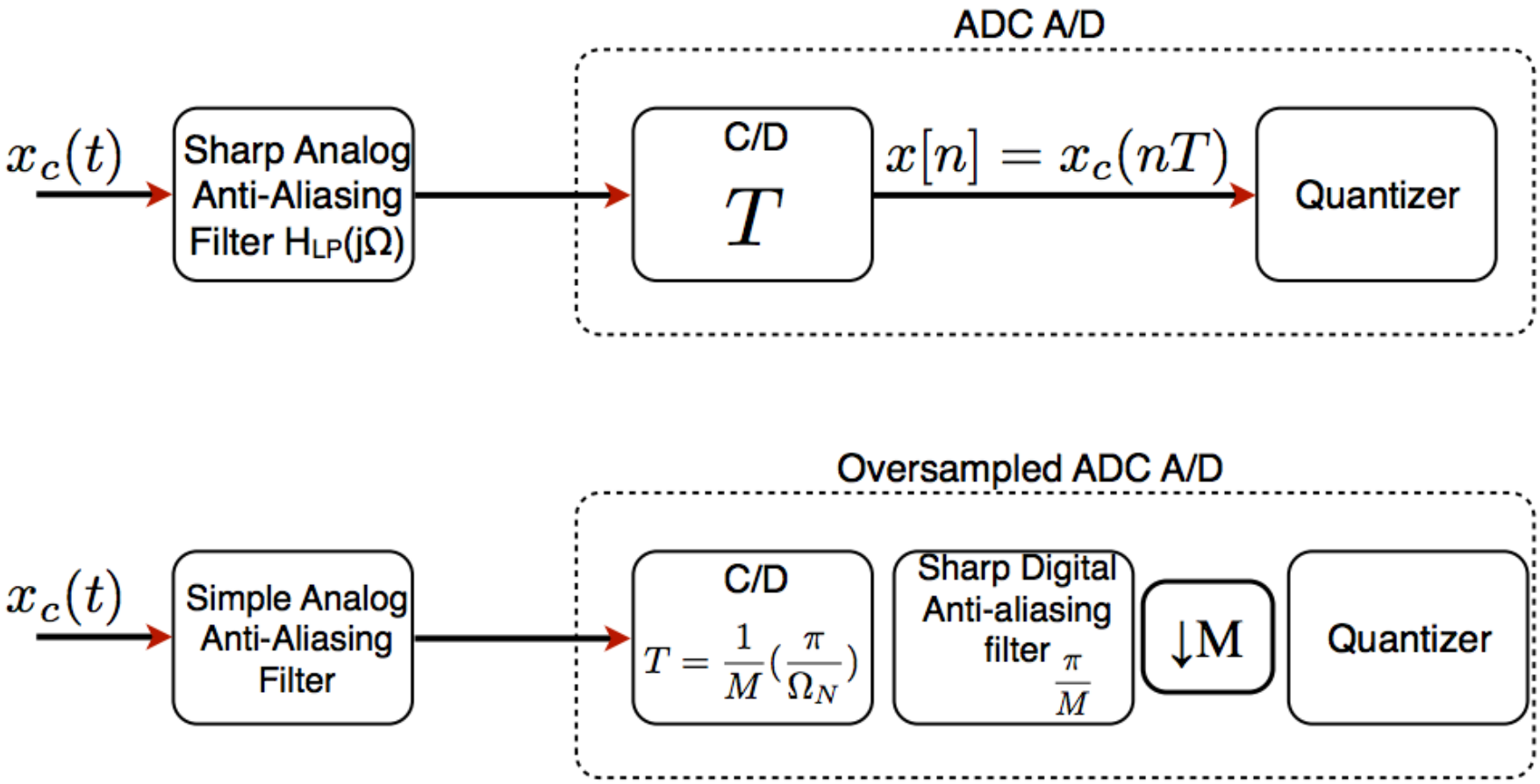
# Quantization Noise Spectrum

- If the quantization error is "sufficiently random", it also follows that the noise power is uniformly distributed in frequency

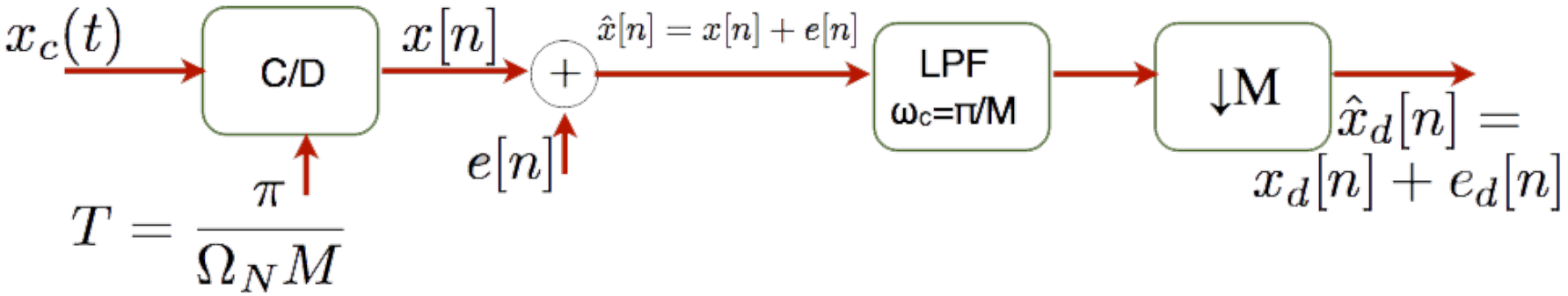


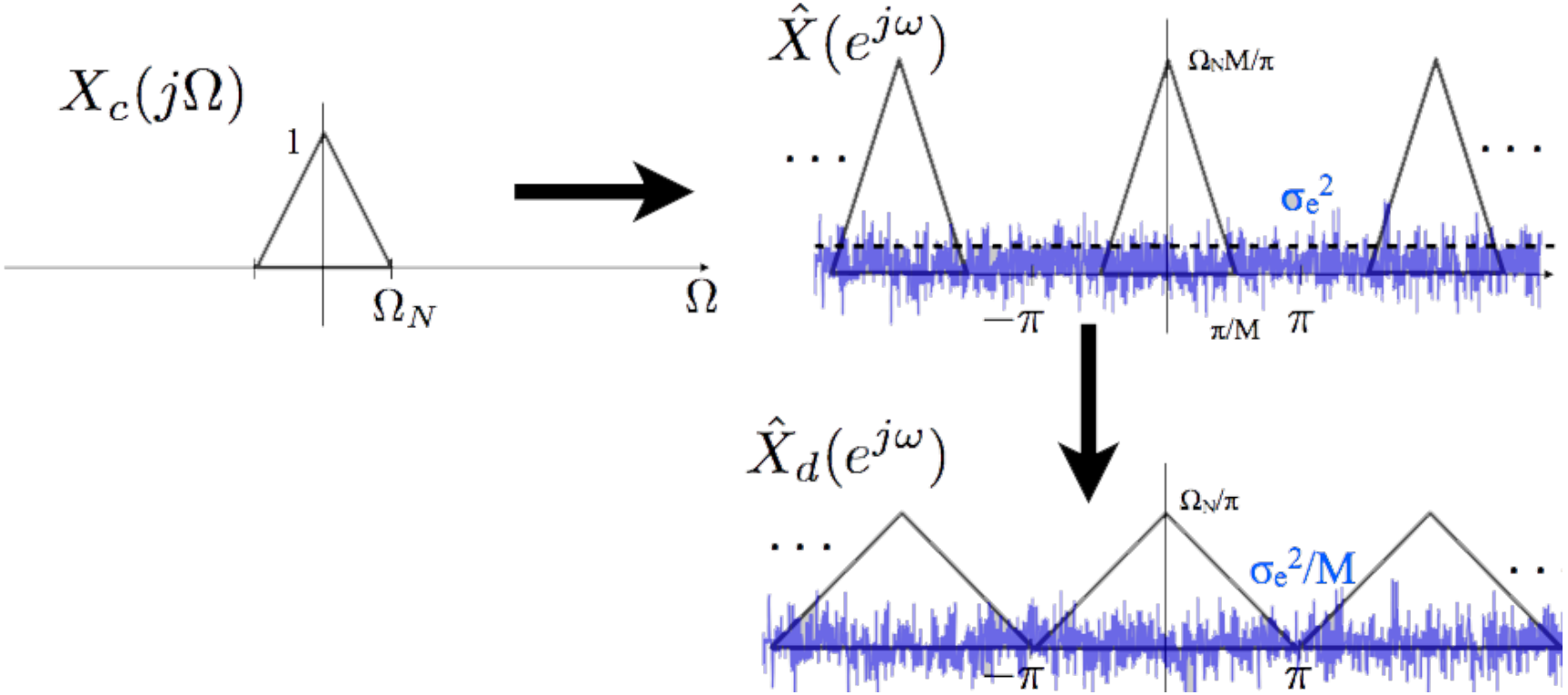

- References
  - W. R. Bennett, "Spectra of quantized signals," Bell Syst. Tech. J., pp. 446-72, July 1988.
  - B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," IRE Trans. Circuit Theory, vol. CT-3, pp. 266-76, 1956.

# Oversampled ADC



# Quantization Noise with Oversampling



# ADC Architectures

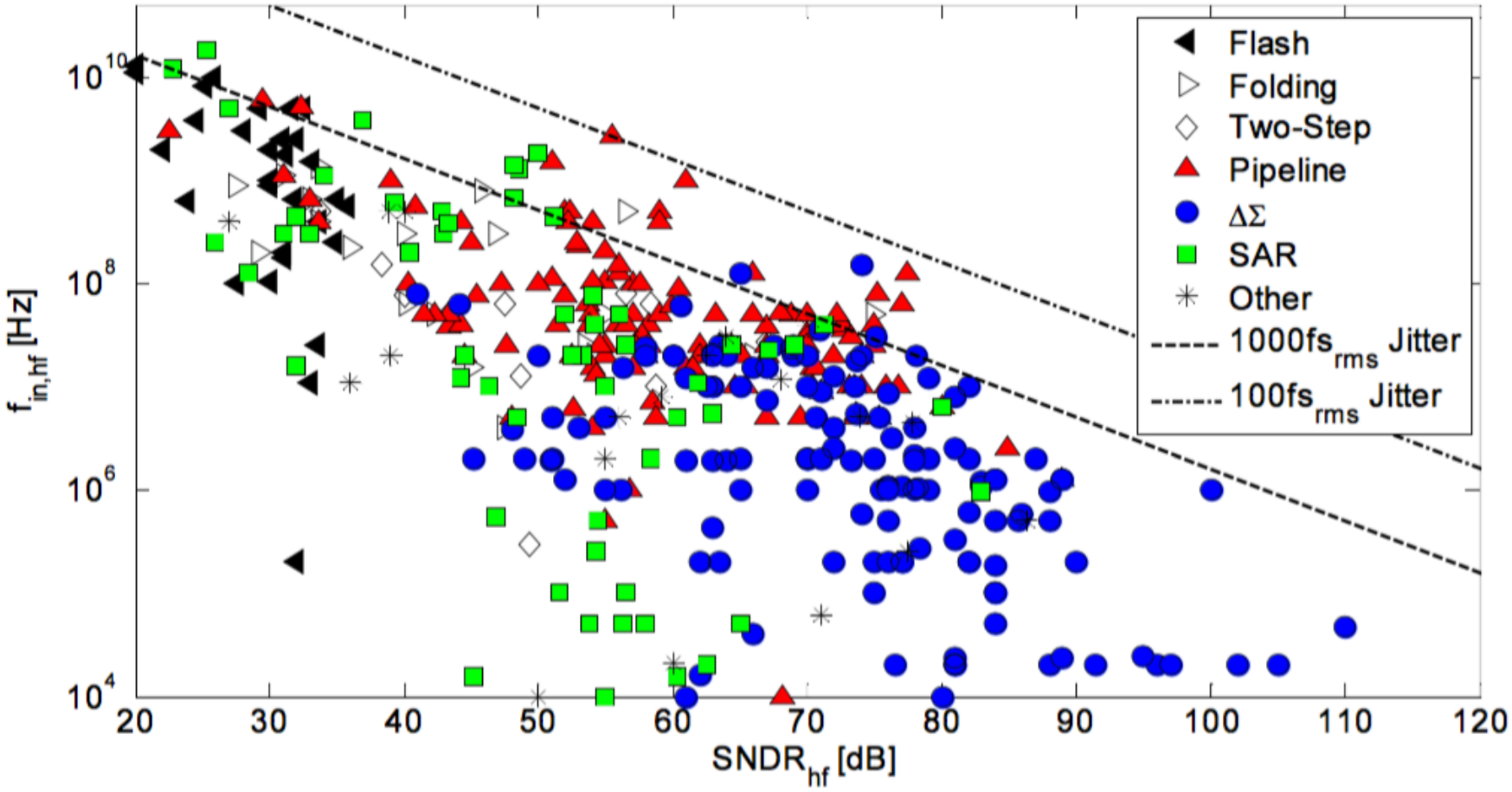
# Nyquist ADC Architectures

- Word-at-a-time
  - E.g. flash ADC
  - Instantaneous comparison with $2^B$-1 reference levels
- Multi-step
  - E.g. pipeline ADCs
  - Coarse conversion, followed by fine conversion of residuals
- Bit-at-a-time
  - E.g. successive approximation ADCs
  - Conversion via a binary search algorithm

speed

# ADC Survey (ISSCC & VLSI 1997-2013)

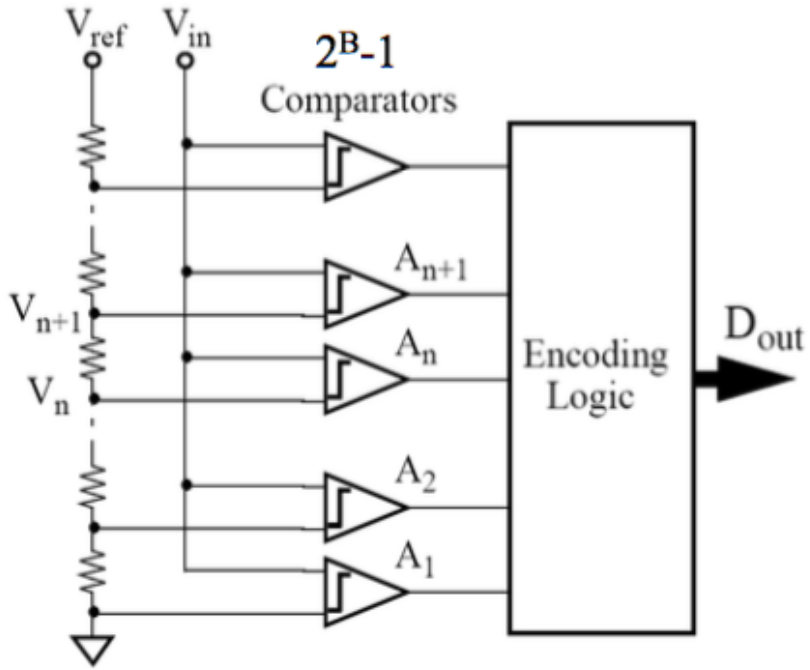
Data: http://www.stanford.edu/~murmann/adcsurvey.html

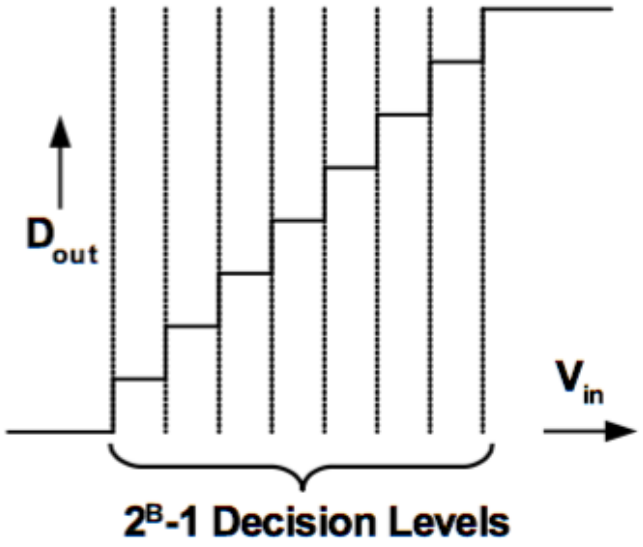


# Flash ADCs

# Flash ADC

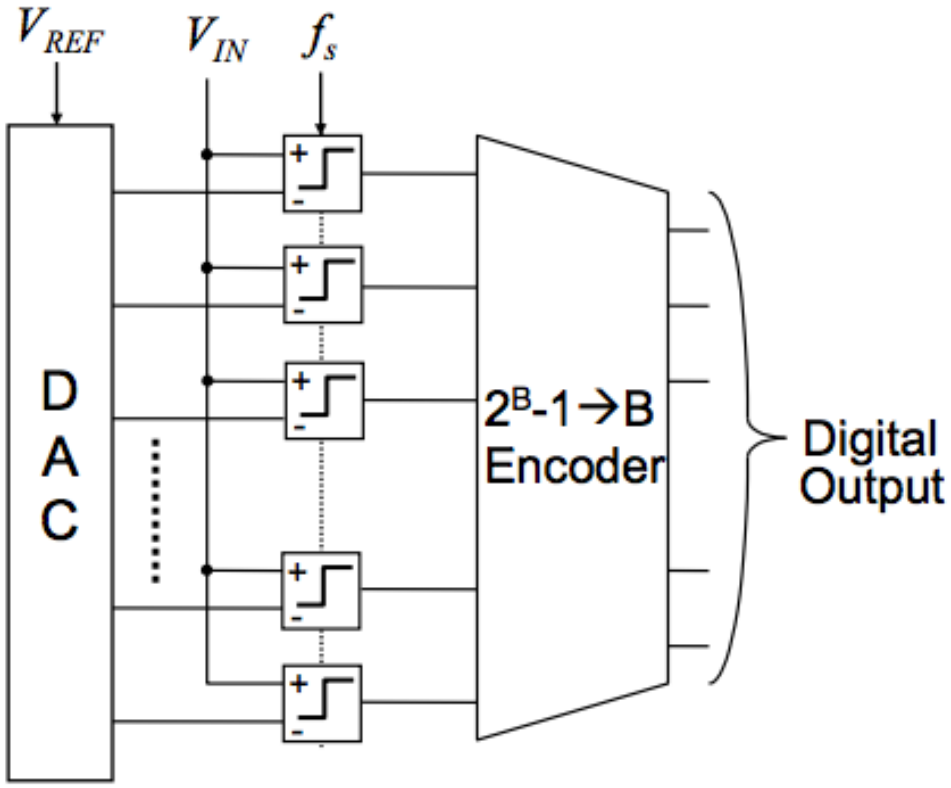
- Fast
  - Speed limited by single comparator plus encoding logic
- High circuit complexity ($2^B$-1 comparators), high input capacitance
  - Typically only use for resolution up to 6...8 bits



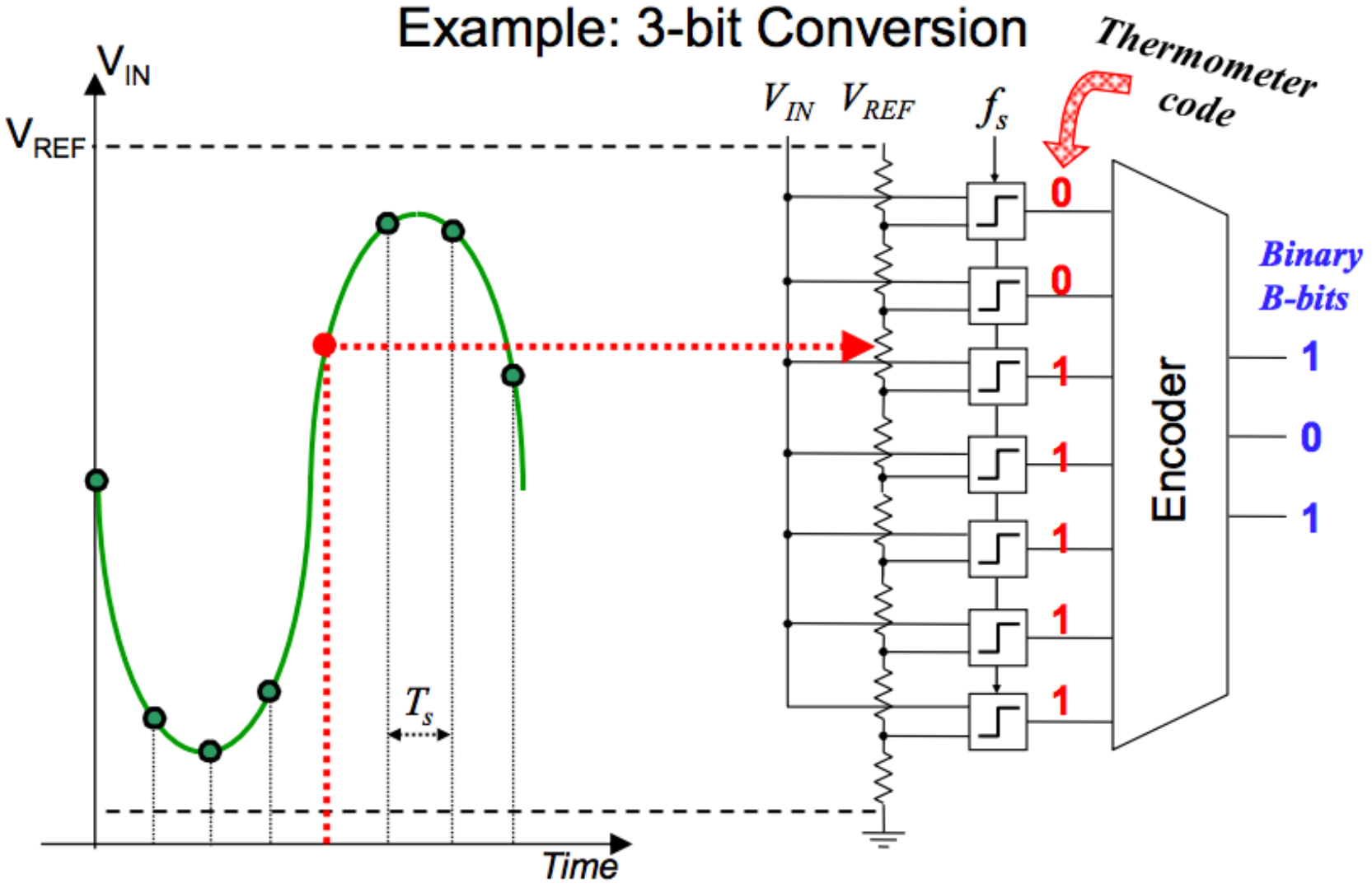



# Flash ADC

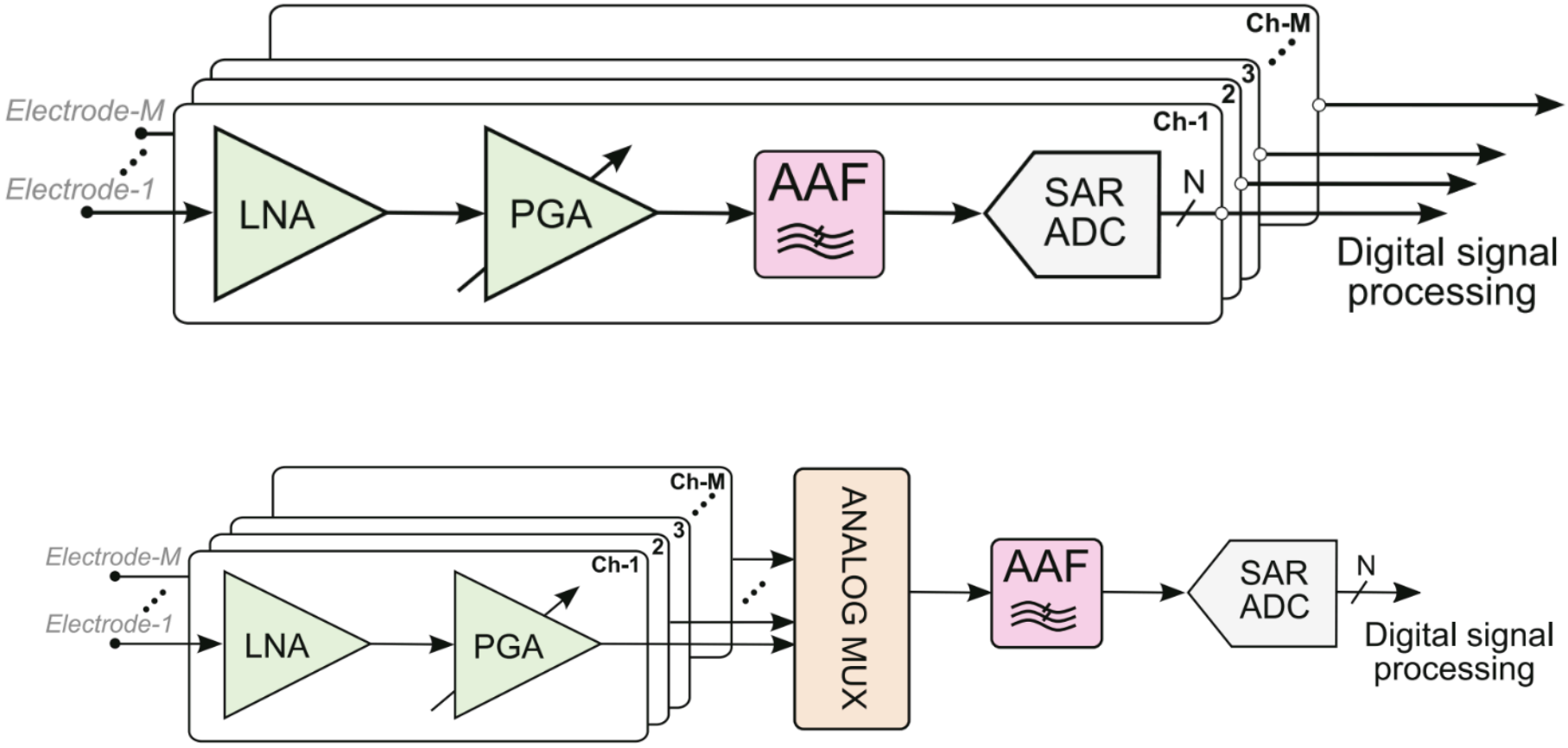
- B-bit flash ADC:
  - DAC generates all possible $2^B$-1 levels
  - $2^B$-1 comparators compare $V_{IN}$ to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code



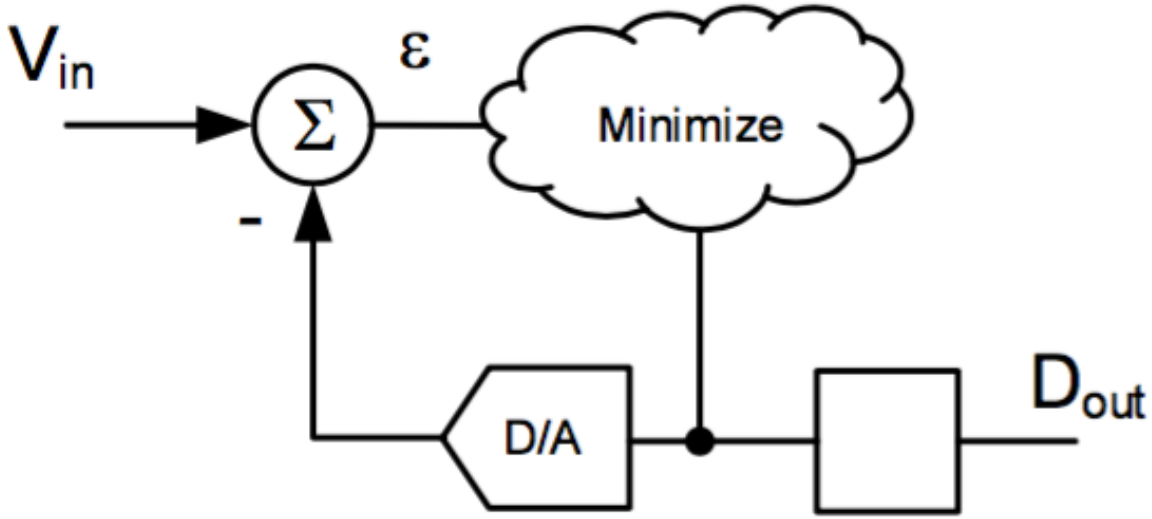
# Flash ADC


Example: 3-bit Conversion
$V_{IN}$
$V_{REF}$
$V_{IN}$ $V_{REF}$
$f_s$
Thermometer code
0
0
1
1
1
1
1
Encoder
Binary B-bits
1
0
1
$T_s$
Time

# Multi-channel Bio-potential Recording

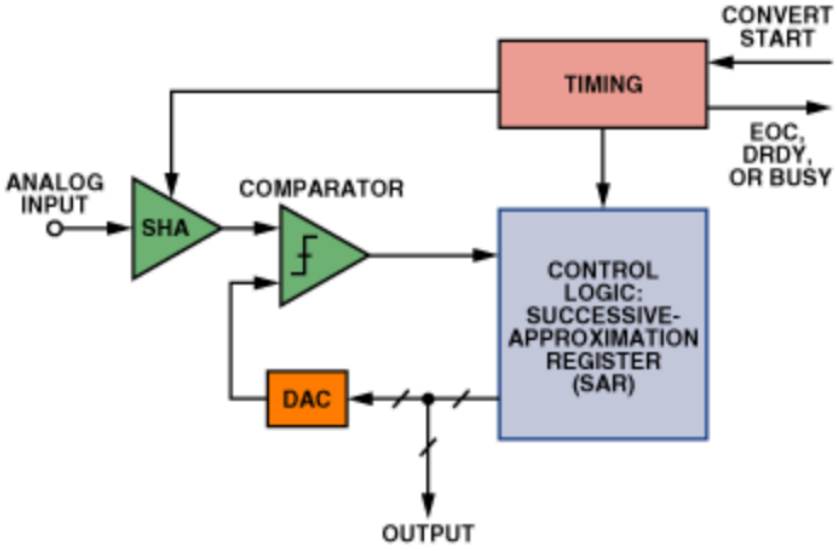


# SAR ADC Architectures



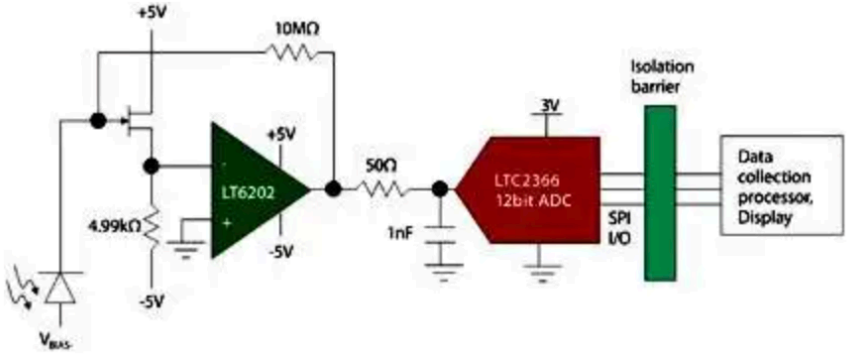

- Most ADC architectures (other than flash) are based on minimizing (reducing) the error between input and a D/A signal approximation
  - Pipeline uses distributed DAC
  - SAR ADC uses comparator to sense error
  - Sigma-delta ADC minimizes error via integration and feedback

# SAR ADC



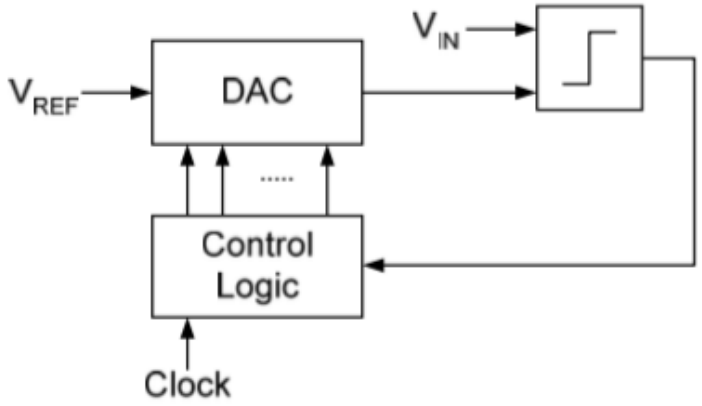

- Key features:
- High resolution
- Fast response and low latency
- Power varies with sample rate

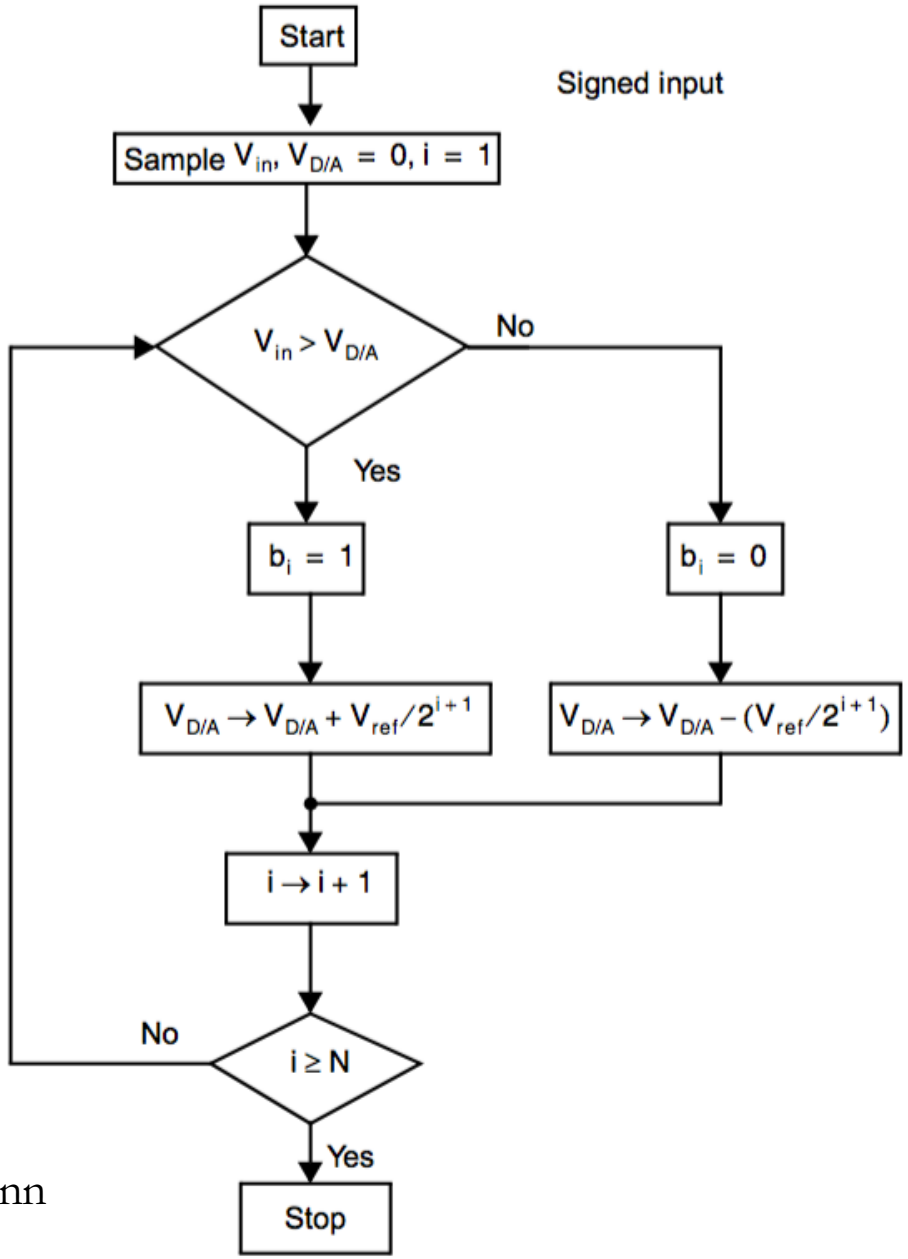
# Pulse Oximetry Example



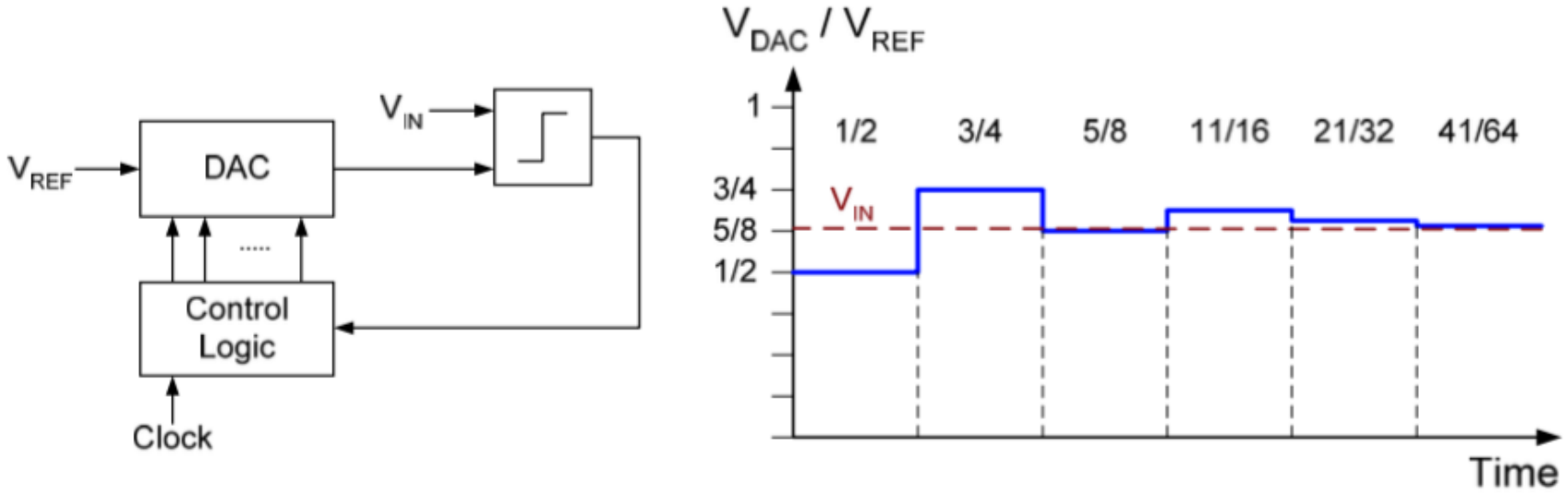

- LTC2366 is part of a family of tiny ADCs sampling from 100KSps to 3MSps
- ADCs dissipate only 7.8mW at 3MSps, 1.5mW at 100KSps and 0.3 microwatts in sleep mode
- LTC2366 features no data latency through the ADC

# Successive Approximation Algorithm



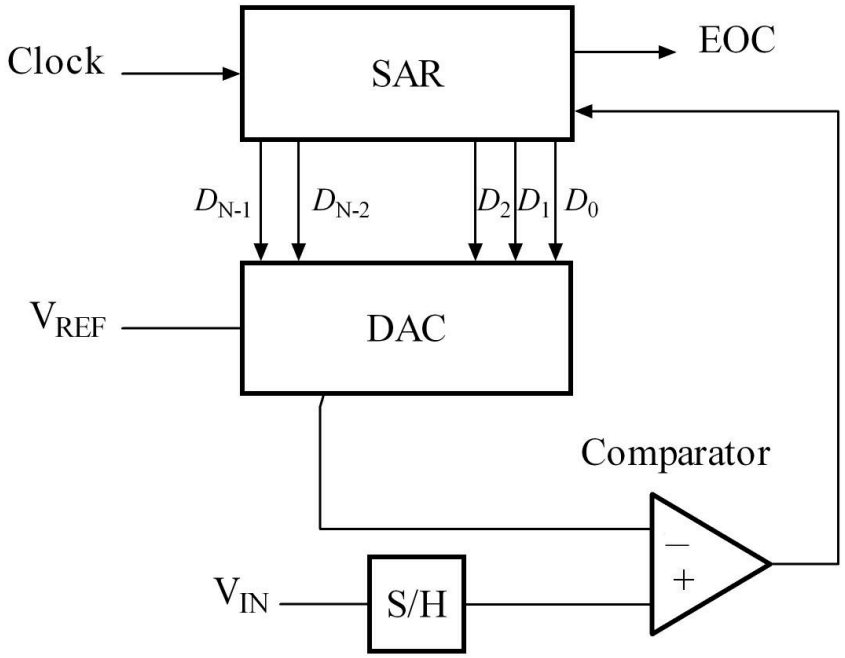



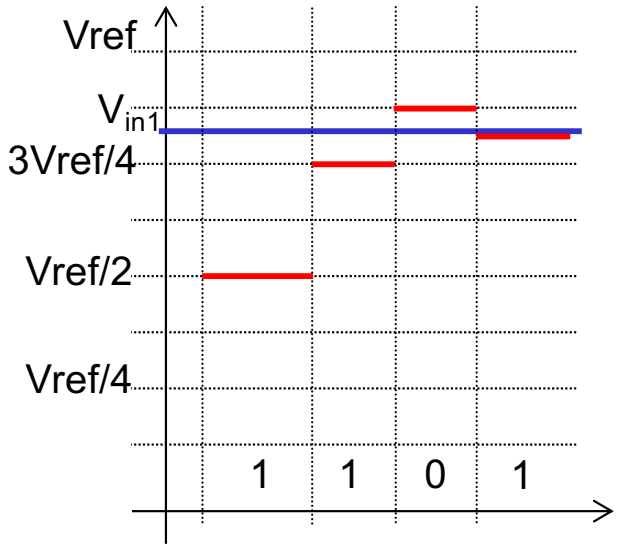
# Successive Approximation Register ADC




- Binary search over DAC output
- High accuracy achievable (16+ bits)
  - Relies on highly accurate comparator
- Moderate speed (1+ Mhz)

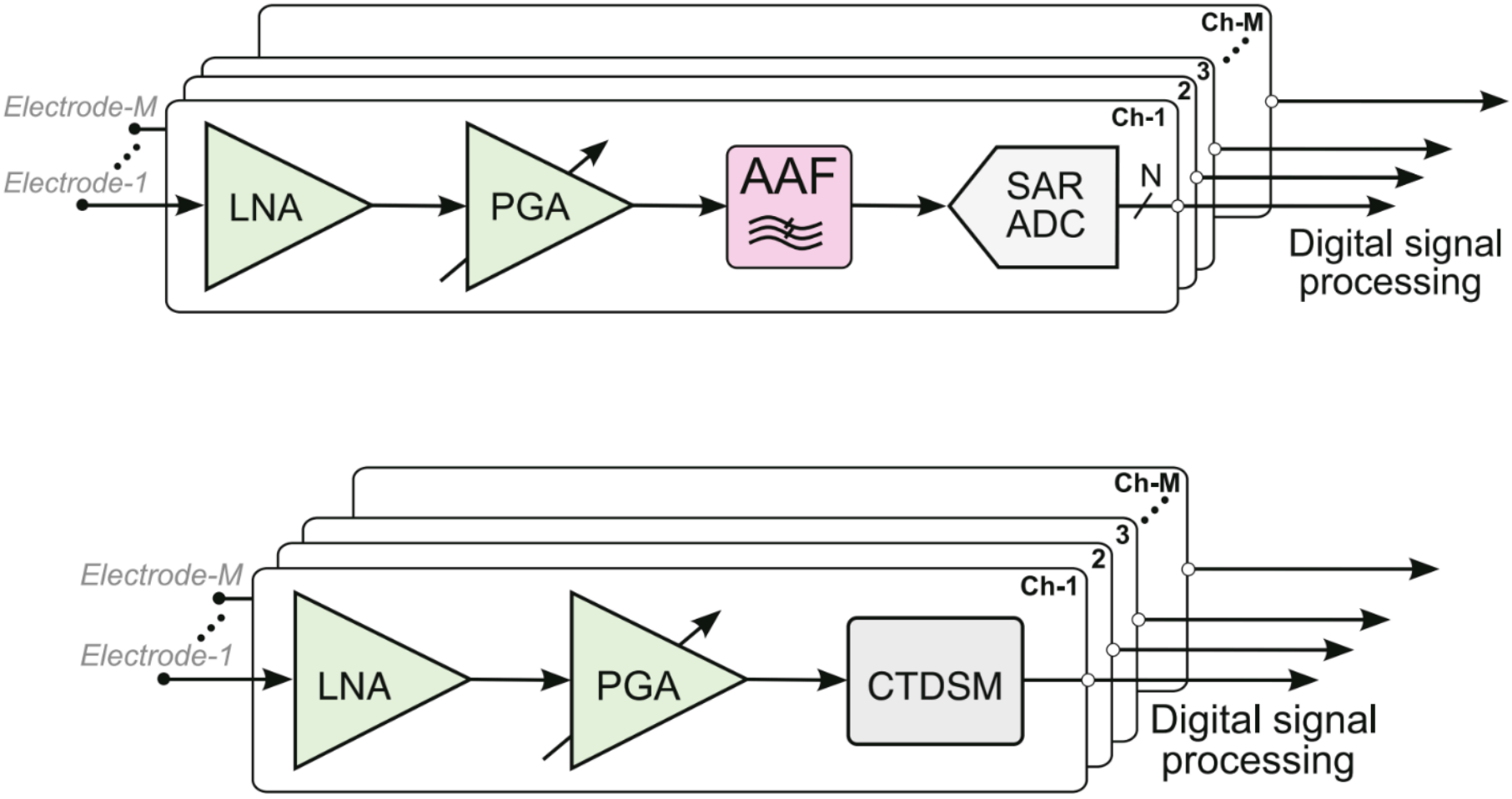
# SAR ADC Block Diagram



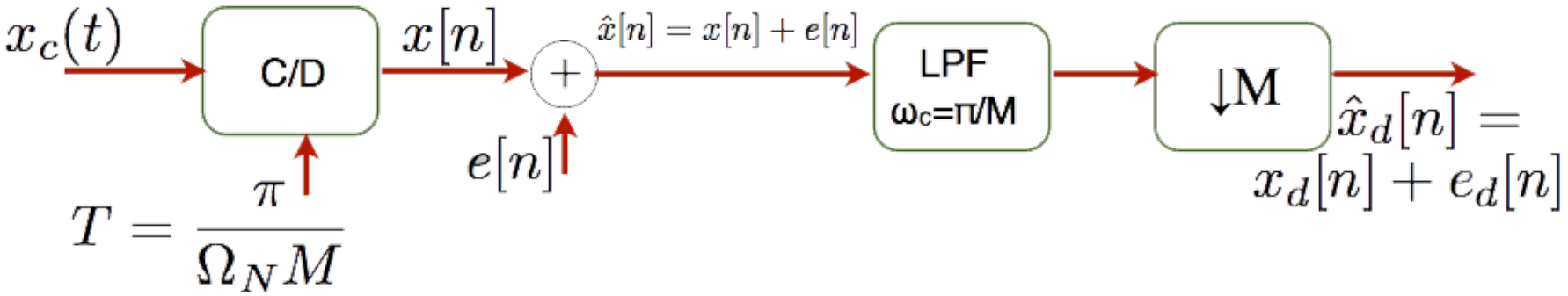



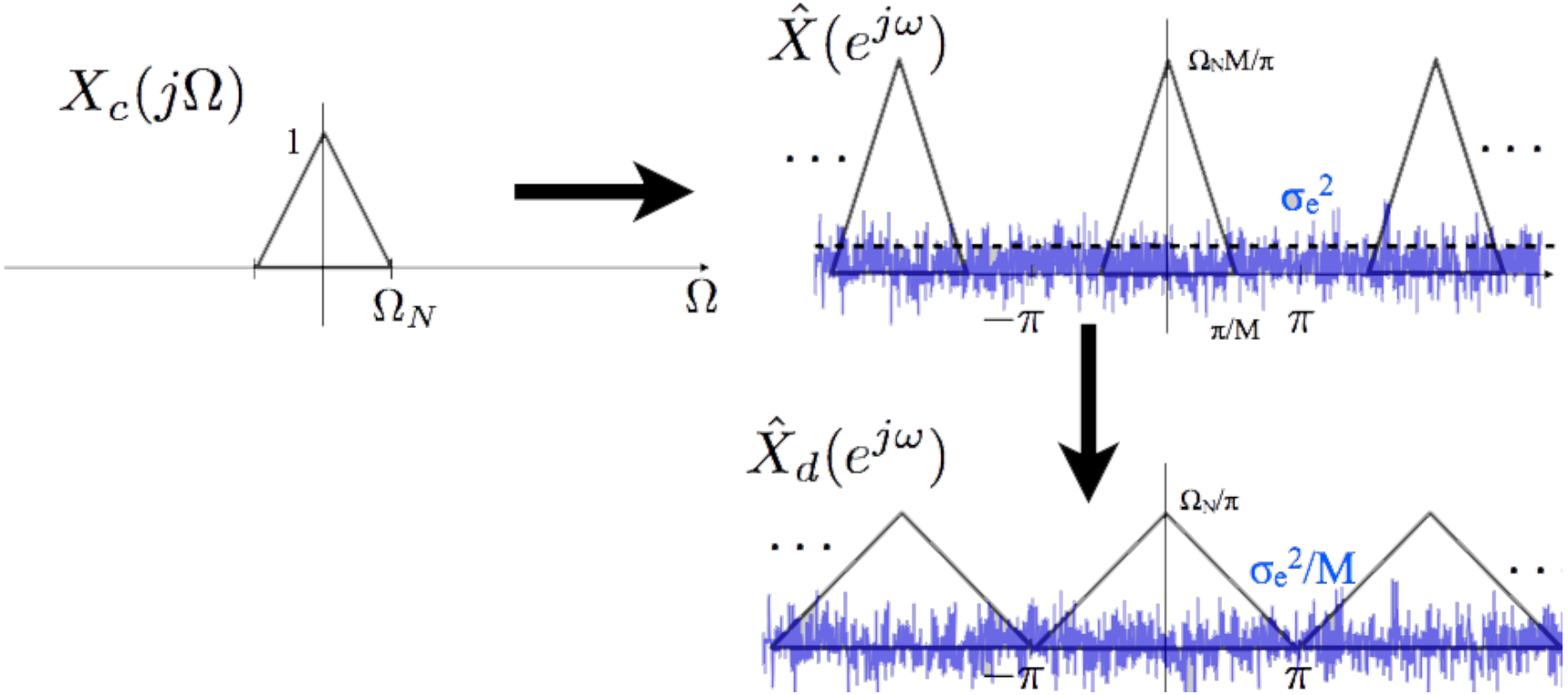

- Sampling phase: Sample input with Sample-and-Hold
- Bit-cycling: Compare with DAC output, adjusting the SAR with each clock cycle as bits are determined

# Multi-channel Bio-potential Recording



# Quantization Noise with Oversampling



# Oversampled Converters Baseband Noise

$$S_B = S_{B0}\left(\frac{2f_B}{f_s}\right) = \frac{S_{B0}}{M}$$

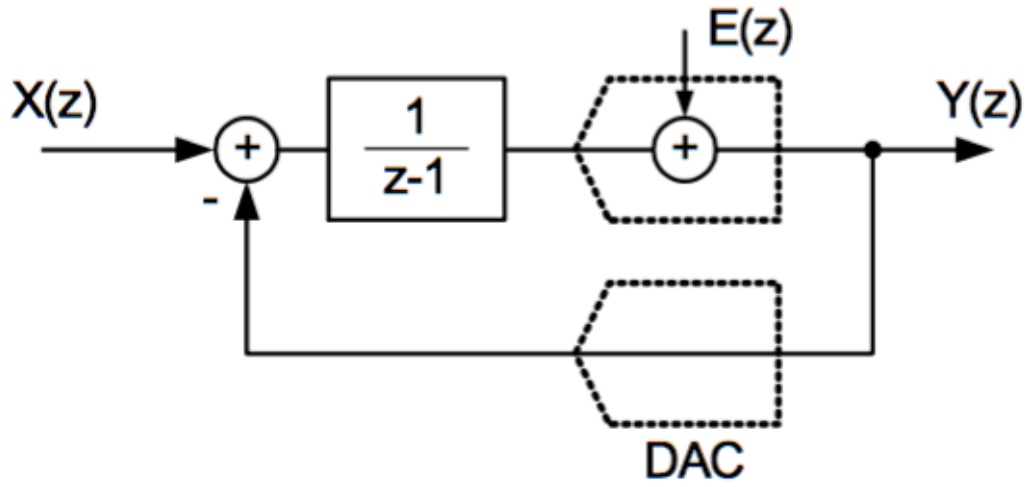
$$where\ M = \frac{f_s}{2f_B} = oversampling\ ratio$$

2X increase in M

→ 3dB reduction in $S_B$

→ ½ bit increase in resolution/octave oversampling

# First Order Sigma-Delta Modulator




$$Y(z) = E(z)\frac{1}{1+\frac{1}{z-1}} + X(z)\frac{\frac{1}{z-1}}{1+\frac{1}{z-1}}$$

$$= E(z)\left(1-z^{-1}\right) + X(z)z^{-1}$$

- Output is equal to delayed input plus filtered quantization noise

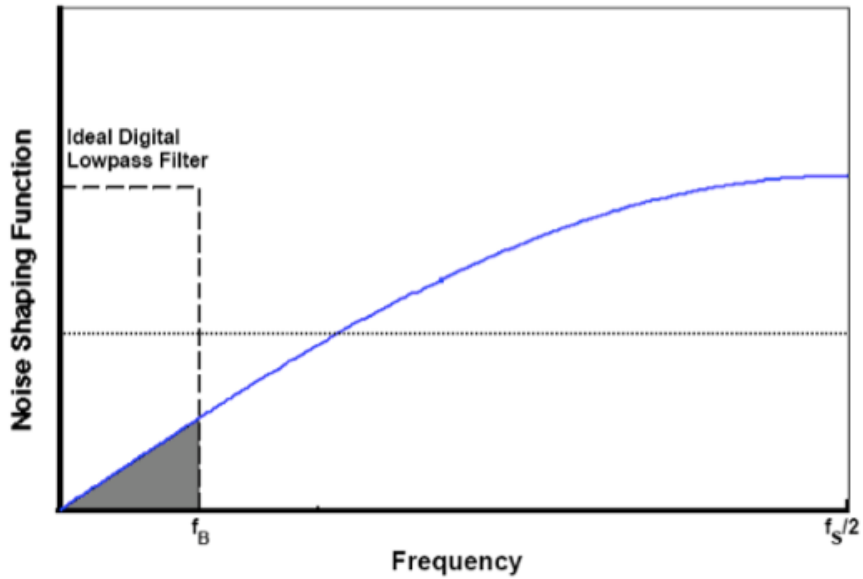
# NTF Frequency Domain Analysis

$$H_e(z) = 1 - z^{-1}$$

$$H_e(j\omega) = \left(1 - e^{-j\omega T}\right) = 2e^{-j\omega T/2}\left(\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2}\right)$$

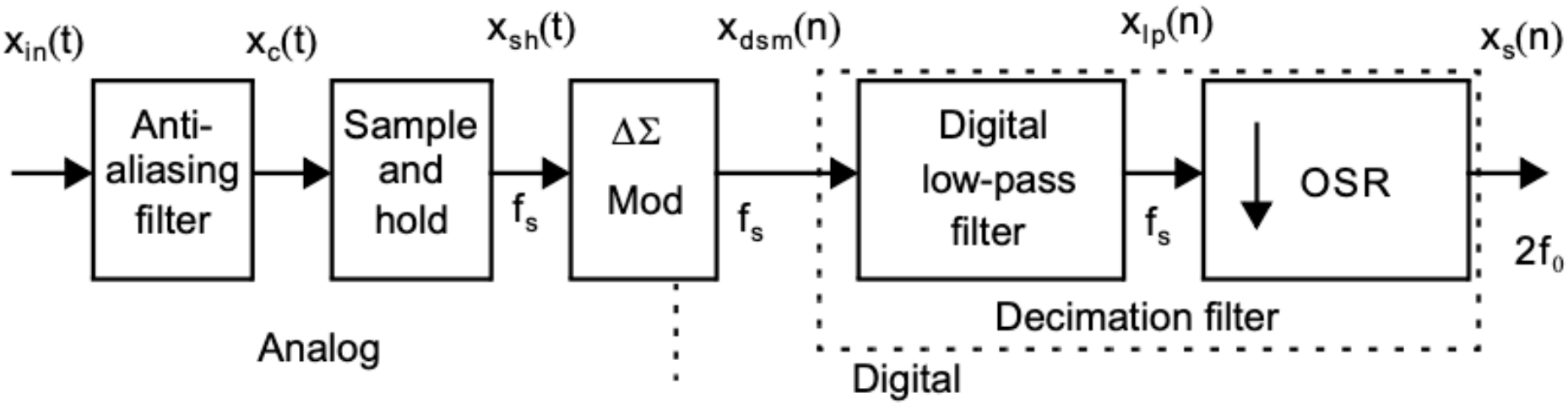
$$= 2e^{-j\frac{\omega T}{2}}\left(j\sin\left(\frac{\omega T}{2}\right)\right) = 2\sin\left(\frac{\omega T}{2}\right)e^{-j\frac{\omega T - \pi}{2}}$$

$$|H_e(f)| = 2|\sin(\pi f T)| = 2\left|\sin\left(\pi\frac{f}{f_s}\right)\right|$$

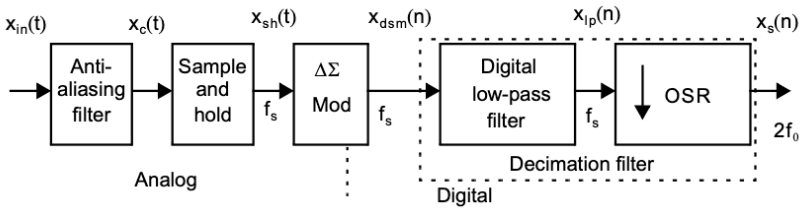


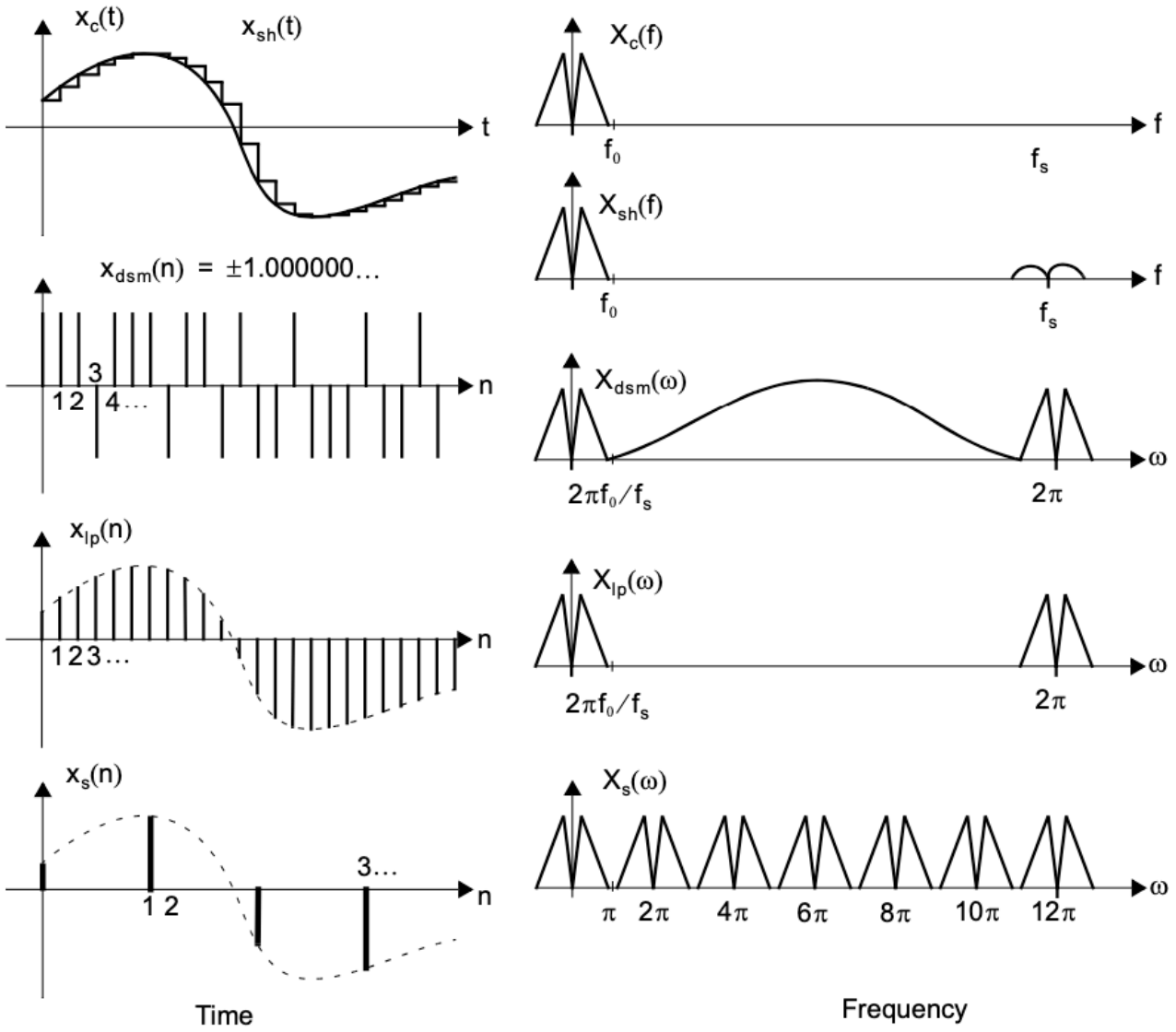

- "First order noise Shaping"
  - Quantization noise is attenuated at low frequencies, amplified at high frequencies

# Decimation Filter

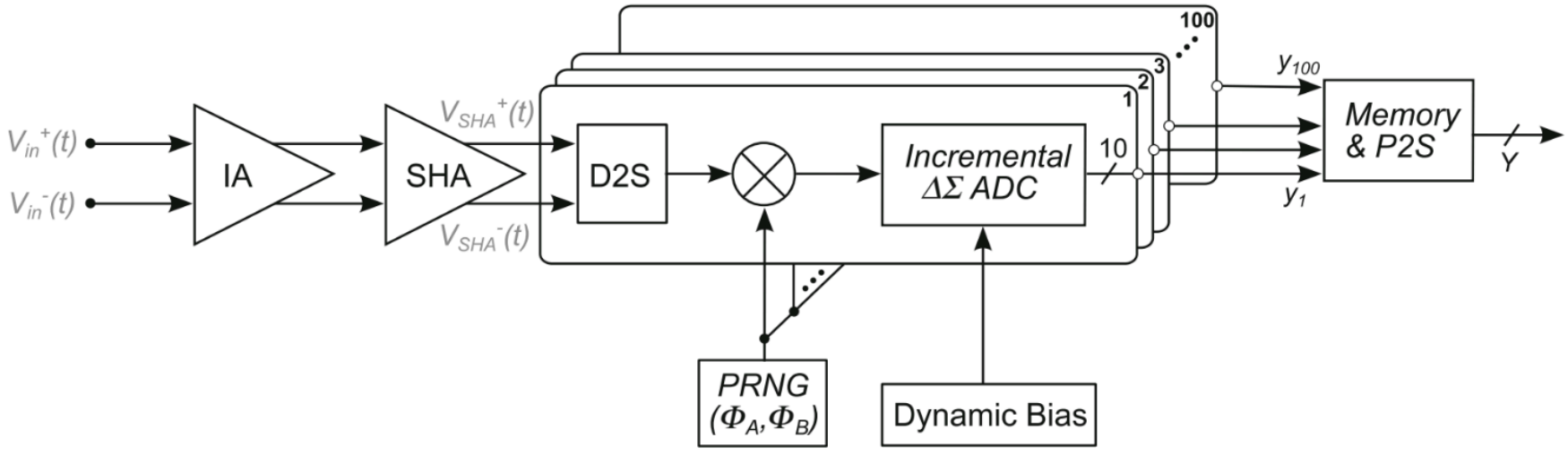


# Decimation Filter



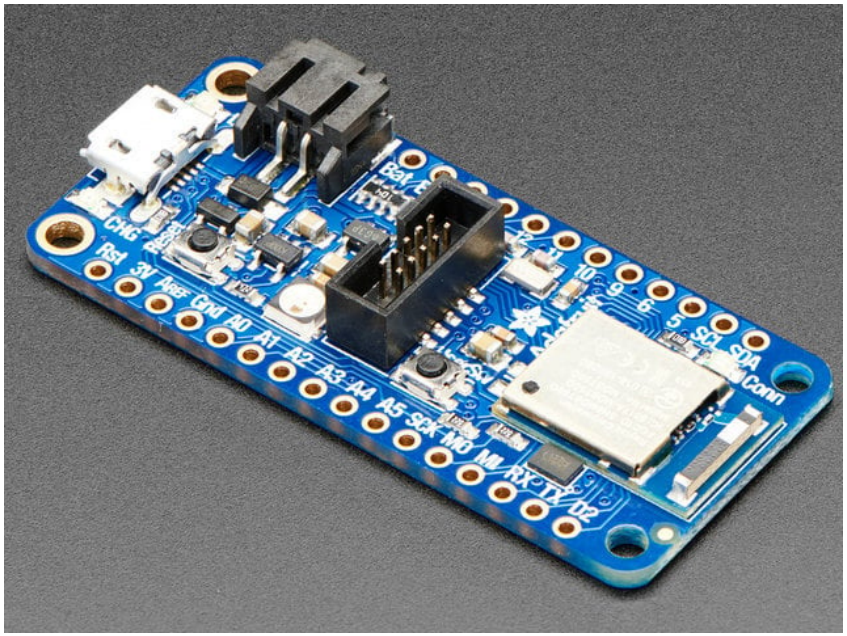
# Compressed Sensing Front End for ECG Monitoring




- Compressive sensing allows fewer samples to recover signals exactly if signal is sparse.

# Lab 6 – Data Converters

- The nRF52 family includes an adjustable 'successive-approximation ADC' which can be configured to convert data with up to 14-bit resolution (0..16383), and the reference voltage can be adjusted up to 3.6V internally.



# Big Ideas

- DTFT vs DFT
  - The DFT characterizes the spectral content of the desired signals
- SQNR
  - SQNR determined by bit resolution, B
  - ENOB determined by SNR
- Oversampling
  - Enables reduction in quantization noise and reduces stress on AAF. More next lecture…
- ADC Architectures
  - Flash ADCs - Word-at-a-time for high speed, low resolution applications
  - SAR ADC - Bit-at-a-time for low speed, low power applications
  - Sigma-Delta ADCs - Usually for low speed, low power applications

# Admin

- Monday: Data Converter Lab
- Wednesday: Quiz 1
  - Designed for an hour, but you have the full 1.5 hour
  - Covers Lec 1-5 and Labs 1-5