Big Idea Compilation
Lec 2: Big Idea

- MOSFET Transistor as switch
- Functionality-driven simplified modeling (Zero order)
  - Aid reasoning
  - Sanity check
  - Simplify design
Lec 2: Big Idea

- Systematic construction of any gate from transistors
  1. Use static CMOS structure
  2. Design PMOS pullup for $f$
  3. Use DeMorgan’s Law to determine $f'$
  4. Design NMOS pulldown for $f'$
Lec 3: Big Ideas

- MOSFET Transistor as switch
- Purpose-driven simplified modeling
  - Aid reasoning, sanity check, simplify design
- Analysis methodology
  - Zero order to understand switch state (logic)
  - First-order to get equivalent RC circuit (delay)
- New perspective on Rs and Cs
Lec 4: Big Idea

- Need robust logic
  - Can design into any (feed forward) graph with logic gates and tolerate loss and noise, while maintaining digital abstraction

- Regeneration and noise margins
  - Every gate makes signal “better”
  - Design level of noise tolerance
Lec 5: Big Idea: Delay is RC Charging
Lec 6-8: Big Idea

- 3 Regions of operation for MOSFET
  - Subthreshold
  - Linear
  - Saturation
    - Pinch Off
    - Velocity Saturation, DIBL
      - Short channel

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Lec 9: Big Idea

- Capacitance
  - To every terminal
  - Voltage dependent

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Lec 10: Big Idea

- Parameters Approximate
- Differ
  - Chip-to-chip, transistor-to-transistor, over time
- Robust design accommodates
  - Tolerance and Margins
  - Doesn’t depend on precise behavior
Lec 11: Big Idea

- Layouts are physical realization of circuit
  - Geometry tradeoff
    - Can decrease spacing at the cost of yield
    - Design rules

- Can go from circuit to layout or layout to circuit by inspection
Lec 12: Big Ideas

- Moderately predictable VLSI Scaling
  - unprecedented capacities/capability growth for engineered systems
  - change
  - be prepared to exploit
  - account for in comparing across time
  - …but not for much longer
Lec 13: Ideas

- First order delay reason in $\tau = R_0 C_0$ units
  - Equivalently $(C_0/I_0)$ units
- Scaling everything up doesn’t help
- Drive large capacitive loads in stages
Lec 14: Ideas

- First order reason in $\tau = R_0C_0$ units
- Gates have different efficiencies
  - Drive strength per unit input capacitance
- Without velocity saturation
  - Reason to prefer nand over nor
- With velocity saturation (short term),
  - nands and nors are similar efficiency
- Large fanin and fanout slow gates
  - Decompose into stages
  - …but not too much
Lec 15-16: Ideas

- Three components of power
  - Static
  - Dynamic
  - Short-circuit

- \( P_{tot} = P_{static} + P_{dyn} + P_{sc} \)

- Power is data dependent and a function of our switching
Lec 17: Ideas

- There are other logic disciplines
- We have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates static power in one mode
Lec 18: Ideas

- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs
  - ...don’t over-tune
Lec 19-20: Idea

- There are other circuit disciplines
- Can use pass transistors for logic
  - Even chains of pass transistors
  - Mostly gives area win, sometimes gives delay win
    - Will talk more about delay on Monday
- Do not cascade as easily as CMOS
Lec 21: Idea

- Lumped wiring calculation is conservative
  - Not all capacitance at end of wire
- Elmore delay calculation allows us to estimate delay for lumped RC network
- Wires are distributed RC
  - Half delay lumped calculation
  - Still quadratic in length
Lec 22: Idea

- To drive large loads
  - Scale buffers geometrically
  - Exponential scale up in buffer size ($\rho = e$)
- Scale factor: 3—4 typically
  - One origin of fanout 4 target
- Drains contribute capacitance, too ($C_{\text{diff}}$)
- Can formulate sizing to optimize
Lec 23: Idea

- Synchronize circuits
  - to external events
  - disciplined reuse of circuitry

- Leads to clocked circuit discipline
  - Uses state holding element
  - Prevents
    - Combinational loops
    - Timing assumptions
    - (More) complex reasoning about all possible timings
Dynamic/clocked logic

- Only build/drive one pulldown network
- Fast transition propagation
- Spend delay (capacitance) on pullup of critical path of logic
- More complicated design, power dissipation
  - Reserve for when most needed
Lec 25: Idea

- Memory for compact state storage
- Share circuitry across many bits
  - Minimize area per bit $\Rightarrow$ maximize density

- Aggressively use:
  - Pass transistors, Ratioing
  - Precharge, Amplifiers
to keep area down
Lec 26: Idea

- Memory for compact state storage
  - Minimize area per bit → maximize density
  - Requires careful sizing

- Share circuitry across many bits
  - Precharge, Amplifiers

- Serial address memories
  - Use pointers to access memory
    - Eg. FIFO queue
Lec 27: Idea

- Multiported SRAMS
  - Enable register file operation
  - Hurts read stability

- Serial access memories do not use an address
  - Shift Registers, Serial In Parallel Out (SIPO), Parallel In Serial Out (PISO), Queues (FIFO, LIFO)

- DRAM memory
  - Smaller memory cell
  - Require data refresh
  - Bootstrap wordlines
Lec 28: Idea

- Minimize area of repeated cell
- Compensate with periphery
  - Amplification (regeneration/restoration)
- Match periphery pitch to cell row/column
  - Decode
  - Sensing
  - Writer Drivers
Lec 29: Idea

- Capacitance is everywhere
- Especially between adjacent wires
- Will get “noise” from crosstalk
- Clocked and driven wires
  - Slow down transitions
- Undriven wires voltage changed
- Can cause spurious transitions
Lec 30: Idea

- Long wires are inductive
  - **Avoid** them
  - Especially on power supplies
- Bypass capacitors help

\[ V_2 = V_S + B e^{\left(-\frac{R}{2L}\right)t} \]
\[ + e^{\left(j\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}\right)t} \]

Diagram:
- L = 10 nH
- R = 100
- C = 1 pF
Lec 31-32: Idea

- Signal propagate as wave down transmission line
  - Delay linear in wire length
  - Speed
  - Impedance
- Behavior at end of line depends on termination
- Both src and sink are “ends” with reflections

\[ w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \]

\[ Z_0 = \sqrt{\frac{L}{C}} \]

\[ V_r = V_i \left( \frac{R - Z_0}{R + Z_0} \right) \]
Lec 33: Idea

- Transmission lines
  - high-speed
  - high throughput
  - long-distance signaling
- Termination
- Signal quality

\[
\begin{align*}
\omega &= \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \\
Z_0 &= \sqrt{\frac{L}{C}} \\
V_r &= V_i \left( \frac{R - Z_0}{R + Z_0} \right)
\end{align*}
\]
Lec 34: Idea

- Wire delay linear once buffered optimally
- Optimal buffering equalizes delays
  - Buffer delay
  - Delay on wire between buffers
  - Delay of wire driving buffer