• Problem weightings shown.
• Calculators allowed.
• Closed book = No text or notes allowed.
• Final answers here.
• Additional workspace in exam book. Note where to find work in exam book if relevant.
• Sign Code of Academic Integrity statement at back of exam book.

<table>
<thead>
<tr>
<th>Name: <strong>Answers</strong></th>
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|Mean: 83, Standard Deviation: 12|

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q5</th>
<th>Q6</th>
<th>Total</th>
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Default technology:

- $F=22\text{nm}$ High Performance Process (HP)
- $\gamma = 1$
- $V_{dd}=1\text{ V}$
- nominal $V_{thn} = -V_{thp} = 250\text{ mV}$
- $C_0 = 2 \times 10^{-17}\text{ F (for } W = 1 \text{ device)}$
- velocity saturated operation

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{gs}$</th>
<th>$I_{ds}$</th>
</tr>
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<tbody>
<tr>
<td>NMOS</td>
<td>$V_{gs} &lt; V_{thn}$</td>
<td>$(5 \times 10^{-7}) W e^{\frac{V_{gs} - V_{thn}}{40\text{ mV}}}$</td>
</tr>
<tr>
<td></td>
<td>$V_{gs} &gt; V_{thn}$</td>
<td>$2 \times 10^{-4}W (V_{gs} - V_{thn})$</td>
</tr>
<tr>
<td>PMOS</td>
<td>$V_{gs} &gt; V_{thp}$</td>
<td>$(-5 \times 10^{-7}) W e^{-\frac{V_{gs} - V_{thp}}{40\text{ mV}}}$</td>
</tr>
<tr>
<td></td>
<td>$V_{gs} &lt; V_{thp}$</td>
<td>$2 \times 10^{-4}W (V_{gs} - V_{thp})$</td>
</tr>
</tbody>
</table>

Transmission line:

\[
w = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\varepsilon_r \mu_r}} \tag{1}
\]

\[
Z_0 = \sqrt{\frac{L}{C}} \tag{2}
\]

\[
V_r = V_i \left( \frac{R - Z_0}{R + Z_0} \right) \tag{3}
\]

\[
V_t = V_i \left( \frac{2R}{R + Z_0} \right) \tag{4}
\]
1. Dynamic Logic (10pts). Consider the following domino logic circuit. What logic function does it evaluate?

Assume the circuit is driven by \( R_0 \) drive input and is loaded by \( 10C_0 \) output. Assume \( C_{diff} = 0.5C_{gate} \), \( \mu_n = 2\mu_p \). Assume the CLK signal is driven strongly such that the rise time on the clock is \( R_0C_0 \). Use Elmore delay calculations where appropriate. For full credit (and partial credit consideration) show your delay components (stages, components of Elmore delay calculation).

\[
\text{Out as a function of the inputs: } A, B, C, X, Y, Z \text{ and } S? (A+B+C+X+Y+Z)*S
\]

\[
\begin{align*}
\text{Evaluate Delay} & \quad \text{(show delay components)} \\
\frac{3+3+3+3+6}{8} + \frac{3+\frac{12}{3}+6}{8} & + \frac{3+\frac{12}{3}+6}{8} + \frac{\frac{5}{2}+4}{2} \\
& + \frac{2+\frac{12}{2}+6}{8} + \frac{2+\frac{12}{2}+6}{8} + \frac{2+\frac{12}{2}+6}{4} + \frac{\frac{5}{2}+10}{2}
\end{align*}
\]

The input S arrives to the second stage early and discharges the node capacitances at the drains of both size 8 NMOS early. Answers that also added input and clock drives were accepted.
2. Design Space Exploration (15 pts). Explore the methodology to design a circuit to detect when two 32b values match with the minimum energy.

\[ \text{Out} = (A[31:0] == B[31:0]) \]  

- Assume the match condition is relatively uncommon.
- This is a wakeup circuit for some larger computation. The rest of the computation is powered down to save energy. Maybe this is a battery powered device waiting for a password.

(a) How would you decompose this problem into sub-pieces? Decompose the system into bit-by-bit comparisons, and then AND the resulting bits for a single output.

(b) How would you perform the match operation using nand2 gates and inverters?
(c) Design a single gate that takes in two inputs and has one output at the transistor level that you could use to perform the match condition.

(d) List and briefly explain five things in the design space you could explore to look for an optimal design solution? (Said another way: what “knobs” are available for you to turn and “choices” are available for you to make?)

1. **Gate choice** - reduce the number of switched gates to reduce power switching energy
2. **Logic choice** - ratio, pass, domino logic to reduce delay, area, and energy
3. **Size transistors** - reduce delay by increasing drive
4. **Reduce $V_{dd}$** - reducing voltage supply to decrease energy however increases delay
5. **Fanin/Fanout** - Decrease switching capacitive loads to decrease delay however increases delay
3. SRAM memory array (30 pts). Assume we have a 5-transistor SRAM cell consisting of two inverters in feedback storing the bit value with one access transistor for both the read and write operations. The memory cell in the figure below is used to create a memory array with \(d\) rows and \(w\) columns (\(d\) words of \(w\) bits each).

(a) What is the capacitance of the bit line, BL, in terms of access transistor width \(W_{\text{access}}\), \(d\), \(\gamma\), and \(C_0\)?

\[d\gamma W_{\text{access}} C_0\]

(b) Assume bit line, BL, is pre-charged to \(V_{dd}\) prior to a read operation. During the read operation, what is the delay of the memory cell driving BL in terms of \(W_{\text{access}}\), \(d\), \(\gamma\), \(C_0\), \(R_0\), and \(W_1\).

\[\left(\frac{R_0}{W_1} + \frac{R_0}{W_{\text{access}}}\right) d\gamma W_{\text{access}} C_0\]

In the worst case when reading a 0, the node capacitance at the drain of \(W_1\) is already discharged.
(c) Calculate the delay for \( W_{\text{access}} = W1 = 1, \gamma = 1 \) in terms of \( \tau = R_0C_0 \).

<table>
<thead>
<tr>
<th>Unit</th>
<th>Delay in ( \tau )</th>
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</thead>
<tbody>
<tr>
<td>d=32 (register file)</td>
<td>64( \tau )</td>
</tr>
<tr>
<td>d=512 (BRAM or small L1 Cache)</td>
<td>1024( \tau )</td>
</tr>
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</table>

(d) What is the capacitance of the word line, WL in terms of \( W_{\text{access}}, w, \gamma, \) and \( C_0 \)?

\[ wW_{\text{access}}C_0 \]

(e) Assuming word line, WL, is driven by an inverter with transistor sizing \( W_n = W_p = W_{\text{wldrive}} \), what is the delay driving WL in terms of \( W_{\text{wldrive}}, W_{\text{access}}, w, \gamma, C_0, \) and \( R_0 \)?

\[ \frac{R_0}{W_{\text{wldrive}}} (wW_{\text{access}}C_0 + 2\gamma W_{\text{wldrive}}C_0) \]
4. Serial Access Memories (10pts). The following three circuits are built using positive-edge triggered registers and two input multiplexers. Identify the operation each memory performs and describe the operation.

(a) Parallel in, Serial Out - On shift high, parallel data inputs are sampled and when shift low, the data is shifted out in serial.

(b) Shift Register - The input is delayed by 4 clock cycles

(c) Serial in, Parallel Out - Shift the data in, and parallel output is valid every 4 clock cycles
5. Transmission Line Termination (15pts). Fill in the table below and match the following transmission line circuits (1-5) with the correct pulse propagation plot (a-d) for sending a pulse down the transmission lines to a resistive load. There is intentionally one less plot than circuit. The effective resistance seen into the source is a short circuit.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Answer</th>
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<tbody>
<tr>
<td>1)</td>
<td>B</td>
</tr>
<tr>
<td>2)</td>
<td>C</td>
</tr>
<tr>
<td>3)</td>
<td>B</td>
</tr>
<tr>
<td>4)</td>
<td>D</td>
</tr>
<tr>
<td>5)</td>
<td>A</td>
</tr>
</tbody>
</table>
6. (20 pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be clear in your explanation and handwriting.

A Identify and describe two differences between SRAM and DRAM memory cells.
   DRAM needs data refresh because of leakage. DRAM is smaller than SRAM.

B What is crosstalk and what is one engineering technique you can use to reduce crosstalk?
   Crosstalk occurs when signals on adjacent wires are coupled through the parasitic capacitance between the wires. Wires can be placed further apart, and driven shielding wires can added to reduce crosstalk.

C For the RLC circuit below driven with a step input, an expression for the voltage across the capacitor is given as

\[
V_C = 1 + e^{-\frac{R}{2L}t}e^{jt\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}}
\]

For what values of R (in terms of L and C) will the voltage across the capacitor oscillate?
   \( R < \sqrt{\frac{4L}{C}} \)
D Assume we have a minimum sized buffer in our 22nm technology driving a long
(≥1mm) wire loaded by an identical buffer as shown below. What dominates the
delay? What can you do to reduce the delay assuming you only have minimum
sized buffers available to you?

The delay is dominated by the wire capacitance. We can add buffers along the
wire to reduce the delay.

E For the same setup in part D but now with full design control (i.e not just minimum
sized buffers), describe in words the design process you would use to optimize the
delay. Equations can be used but are not necessary.
First, we find the optimal number of buffers and \( L_{seg} \). Then we size the buffers
to find the optimal drive strength for the optimal number of buffers. In doing so
the delays from the drive buffer, wire delay, and delay from load buffer are all
equalized.