Due: Wednesday, September 23, 12:00PM

REMINDER: Show/explain your work. Make your work easily readable (e.g., annotate relevant pieces and numbers by hand, remove bulky headers, etc.) don’t just do a printout dump. This goes for everything you turn in for any class.

Unless otherwise noted, assume:
- 22nm PTM Spice models that you used on HW3: /home1/e/ese370/ptm/22nm_HP.pm
- T=27 C (300K)

Temperature in SPICE:
- You control temperature in ngspice with the .temp directive in your SPICE deck (a.k.a. netlist). For example:

  .temp 27

  The transient analysis output tells you which temperature it is using. You can use that output to verify that you are successfully setting the temperature for the spice simulator. You will need to add the .temp directive manually to your SPICE file. We suggest putting it after the .include line.

  The temperature can be swept using a DC analysis For example:

  dc temp -40 125 1

Other useful Ngspice commands:
- dc (large-signal analysis), ac (transient/small-signal analysis), op (operating point analysis), plot, print, show (for non-linear devices)
- Tutorials: http://ngspice.sourceforge.net/tutorials.html ←The first link is particularly helpful
1. Using SPICE simulation, what is the equivalent source-drain resistance $R_{ds}$ for a $W = L = 1$ transistor with $V_{gs} = V_{ds} = V_{dd} = 0.8V$ (NMOS) or $V_{gs} = V_{ds} = -V_{dd} = -0.8V$ (PMOS)? Answer for both NMOS and PMOS transistors.

   - Include description of test circuit, circuit schematics, ngspice simulation commands and results in homework turnin. Part of the question is designing and understanding your test setup.

2. Assuming temperature can range from $T=-50C$ to $T=150C$
   
   (a) Using SPICE, what is the range of NMOS $R_{ds}$ resistances could you see for $V_{gs} = V_{dd} = 0.8V$ with $V_{ds} = V_{dd} = 0.8V$?
   
   (b) As a designer, what does this tell you about $R_{on}$?
   
   (c) How will temperature affect the operating speed of your circuit?

3. From a SPICE simulation, what is the RC time-constant for:
   
   (a) one transistor charging another transistor’s gate input of the same size?
   
   (b) a transistor charging the gates of 4 transistors of the same size?
   
   (c) a transistor charging the gate of a single transistor 4 times the size of the driving transistor?
   
   (d) How do your answers to (a), (b), and (c) relate?

   - Include description of test circuit, circuit schematics, ngspice simulation commands and results in homework turnin. Part of the question is designing and understanding your test setup.

4. According to your first-order transistor model, what output does a CMOS inverter produce when $V_{in} = \frac{V_{dd}}{2}$, $V_{dd}=0.8V$, $V_{thn}=250mV$, and $V_{thp}=-250mV$. Assume $R_{on,p} = R_{on,n}$.

5. Consider the following non-CMOS circuit.
$V_{dd} = 0.8V, V_{th} = 250mV$, assume $L = L_{eff} = 1$, and $W$ is the width of the transistor.

Use the following simplified transistor model:

<table>
<thead>
<tr>
<th>$V_{gs}$</th>
<th>$I_{ds}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gs} &lt; V_{th}$</td>
<td>$\approx 0$</td>
</tr>
<tr>
<td>$V_{gs} &gt; V_{th}$</td>
<td>$W \times 10^{-5}$</td>
</tr>
</tbody>
</table>

(a) Assuming $W = 10$, what function does the circuit perform?

(b) Draw its $V_{out}$ vs $V_{in}$ transfer curve.

(c) Identify noise margins that will provide restoration. Give values for $V_{OH}, V_{IH}, V_{IL}, V_{OL}$, $N M_L$, and $N M_H$.

(d) If the transistor width, $W$, is decreased, what is the effect on both low and high noise margins?

6. Consider the following circuit:

Assume: $V_{dd}=0.8V, V_{thn}=250mV, V_{thp}=-250mV$. Reason using your first-order transistor model.

(a) Is this a valid CMOS circuit? Explain why or why not?

(b) Assume $V_{out}$ starts at 0V and $V_{in}$ is increased slowly from 0V to 0.80V, then decreased slowly back to 0V, then the 0V, 0.8V, 0V triangle is repeated a second time. (Slow enough that the circuit has time to reach steady-state for an incremental change in $V_{in}$.) Identify the value of $V_{out}$ at 50mV intervals.

(c) Using your results from the previous part, plot the transfer function $V_{out} = f(V_{in})$. (Hint: assume the input has already switched from 0V to 0.80V to 0V once, and the output is not driven by any other circuit.)
7. Using a first-order model and assuming (a) each transistor has an on resistance $R_{on}$ and (b) each gate has a gate capacitance $C_{gate}$, what is the worst-case rise and fall time of the signal marked?