Due: Wednesday, October 7, 12:00 PM

Unless otherwise noted, assume:

- \( V_{dd} = 0.8 \text{V}, \ V_{thn} = 300 \text{mV}, \ V_{thp} = -300 \text{mV}, \ C_{OX} = 35 \text{fF}/(\mu \text{m})^2, \)
  \( L_{\text{drawn}} = 22 \text{nm}, \ L_{\text{eff}} = 17 \text{nm}, \ W = 44 \text{nm}, \ n = 1.5, \ \nu_{\text{SAT}} = 10^5 \text{m/s}, \ \lambda = 0 \) (probably not correct, but should be consistent where needed), \( \mu_n = 540 \text{cm}^2/(\text{V} \cdot \text{s}), \ \mu_p = 200 \text{ cm}^2/(\text{V} \cdot \text{s}), \ T = 27 \text{C} \) (300K)

- For analytic device modeling, use Equations 3.25, 3.29, 3.37, 3.38, from text.
  - instead of 3.39, use (NMOS):
    \[
    I_{DS} = I_S \left( \frac{W}{L_{\text{eff}}} \right) e^{\frac{V_{GS}-V_{thn}}{n kT/q}} \left( 1 - e^{-\frac{V_{DS}}{kT/q}} \right) (1 + \lambda V_{DS})
    \] (1)

PMOS:
\[
I_{DS} = -I_S \left( \frac{W}{L_{\text{eff}}} \right) e^{-\frac{|V_{GS}-V_{thp}|}{n kT/q}} \left( 1 - e^{\frac{V_{DS}}{kT/q}} \right) (1 - \lambda V_{DS})
\] (2)

with \( I_s = 1 \times 10^{-6} \text{A} \)

- 22nm PTM Spice models: `/home1/e/ese370/ptm/22nm_HP.pm`

NOTE: These parameters are rough approximations and will not match SPICE perfectly.

For questions 1-4 perform the calculations and simulations for an NMOS device.

1. Identify \( V_{DSAT} \).
2. What is the equivalent source-drain resistance \( R_{ds} \) for \( V_{gs} = V_{dd} \) with \( V_{ds} = V_{dd} \)?
   (a) calculate from equations
   (b) estimate from SPICE (similar to hw4)
3. Using equations, estimate worst-case gate capacitance \( C_g \).
4. What is the RC time-constant for a transistor discharging another transistor’s gate input?
   (a) based on \( R_{ds} (V_{gs} = V_{dd}) \) and \( C_g \)
   (b) compare with SPICE
We generally want $I_{on}/I_{off}$ large in order to: (a) achieve output voltages close to the rail, (b) switch quickly, and (c) leak little. Questions 5-9 provide some setup then culminates in a small design problem to select voltage to achieve a target, large $I_{on}/I_{off}$ even in the face of variation.

5. Consider an inverter with $V_{in} = V_{dd}$ after the output has settled to steady state. Using equations:

   (a) Identify the region of operation for the two transistors.
   (b) Identify the current through the transistors.
   (c) Identify $V_{ol}$. (We specifically want to know how far it is from 0; so, do not approximate it as zero as we would typically, but try to identify the small, non-zero value.)

6. At room temperature what is $I_{on}/I_{off} = I_{ds}(V_{gs} = V_h) / I_{ds}(V_{gs} = V_l)$ for an NMOS transistor used in an inverter with $W_p = W_n$; assume $V_{ds} = V_{dd}$ for both cases, so this is just after the input switching in the $V_{gs} = V_h$ case.

   (a) Ideal: $V_h = V_{dd}$, $V_l = 0V$
   (b) With 100mV noise margins: $V_h = V_{dd}-100mV$, $V_l = 100mV$

7. What is the impact of increasing $V_{th}$ on the following (we want a description with words and equations):

   (a) Speed of charging?
   (b) $I_{on}/I_{off}$ with 100mV noise margins.

8. Consider the simple CMOS inverter operated at $V_{dd}=500mV$.

   (a) What makes this case different from the $V_{dd}=0.8V$ case?
   (b) Identify $V_{oh}$, $V_{ih}$, $V_{it}$, $V_{ol}$, and the high and low noise margins that provide proper restoration.
   (c) What does this tell you about your freedom to select $V_{dd}$ and still achieve proper operation?

9. Design problem: Use equations to select $V_{dd}$, $V_{th}$ to achieve $I_{on}/I_{off} > 10^6$ for an NMOS transistor as used in an inverter. Try to keep $V_{dd}$ as small as possible. Assume 100mV noise margin, so $V_{th} \approx V_{dd} - 100mV$, $V_{it}=100mV$. This minimum $I_{on}/I_{off}$ ratio should hold across the temperature range 0C to 100C.