ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 11: September 30, 2015
Layout and Area
Today

- Layout
  - Transistors
  - Gates
- Design rules
- Standard cells
Transistor

Side view

Perspective view

contact
Channel
contact

W
Tox
L
Layout

- Sizing & positioning of transistors
- Designer controls \( W, L \)
- \( t_{\text{ox}} \) fixed for process
  - Sometimes thick/thin oxide “flavors”
NMOS Geometry

Top view

Perspective view
NMOS Geometry

- Color scheme
  - Red: gate
  - Green: source and drain areas (n type diffusion)

Top view

L

W

S

G

D
NMOS vs PMOS

- NMOS built on p substrate
- PMOS built on n substrate
  - Needs an N-well
PMOS Geometry

- Color scheme
  - Red: gate
  - Orange: source and drain areas (p type)
  - Green: n well
- NMOS built on p wafer
  - Must add n material to build PMOS
Body Contact

- “Fourth terminal”
- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = GND$
- At right: PMOS (orange) with bulk contact (dark green)
Body Contact

- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = $ GND

- What happens if NMOS body contact is $V_{dd}$?
Body Contact

- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = \text{GND}$

- What happens if NMOS body contact is $V_{dd}$?
  - Polarity of field wrong
  - Won’t invert channel
Transistor Geometry

NMOS

B  S  G  D

P+  N+  N+

PMOS

D  G  S  B

P+  P+  P+  N+

N Well

P Substrate
Interconnect

- Connect transistors
  - Different layers of metal
    - “Contact” - metal to transistor
    - “Via” - metal to metal
Interconnect

- Connect transistors
  - Different layers of metal
    - “Contact” - metal to transistor
    - “Via” - metal to metal
Interconnect Cross Section

- Passivation
- Dielectric
- Etch Stop Layer
- Dielectric Capping Layer
- Copper Conductor with Barrier/Nucleation Layer
- Pre-Metal Dielectric Tungsten Contact Plug
- Metal 1 Pitch

ITRS 2007
Masks

- Define areas want to see in layer
  - Think of “stencil” for material deposition

- Use photoresist (PR) to form the “stencil”
  - Expose PR through mask
  - PR dissolves in exposed area
  - Material is deposited
    - Only “sticks” in area w/ dissolved PR
Masking Process
Reverse Engineer Inverter Layout
Layout Revisited

- How to “decode” circuit from layout?
Reverse Engineer Inverter Layout

Power (Vdd)

GND
Reverse Engineer Inverter Layout

- Where is PMOS transistor?
- NMOS?
1. Identify transistors
Inverter Layout

- Where is Input?
Inverter Layout

- Where is Input?
Inverter Layout

- Where is Output?
Inverter Layout

- Where is Output?
Layout to Circuit

- 2. Add wires
Layout to Circuit

- 2. Add wires
Layout to Circuit

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Layout to Circuit

- 2. Add wires
Design Rules

- Why not adjacent transistors?
  - Plenty of empty space
  - If area is money, pack in as much as possible

- Recall: processing imprecise
  - Margin of error for process variation
Design Rules

- Contract between process engineer & designer
  - Minimum width/spacing
  - Can be (often are) process specific

- Lambda rules: scalable design rules
  - In terms of $\lambda = 0.5 L_{\text{min}} (L_{\text{drawn}})$
  - Can migrate designs from similar process
Design Rules: Some Examples

![Diagram showing design rules examples with labels: 2\(\lambda\), 3\(\lambda\), 6\(\lambda\), 1.5\(\lambda\), n doping, p doping, gate, metal 1, metal 2, via.]

Legend:
- Blue: contact
- Green: n doping
- Red: gate
- Orange: p doping
- Light Blue: metal 1
- Black: via
- Pink: metal 2

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Layout #2 (practice)
Layout #2 (practice)

- How many transistors?
  - PMOS?
  - NMOS?
- How connected?
  - PMOS, NMOS?
- Inputs connected?
- Outputs?
- What is it?
Standard Cells

- Lay out gates so that heights match
  - Rows of adjacent cells
  - Standardized sizes

- Motivation: automated place and route
  - EDA tools convert HDL to layout
Standard Cell Area

All cells uniform height

Width of channel determined by routing

Cell area
Standard Cell Layout Example

Big Idea

- Layouts are physical realization of circuit
  - Geometry tradeoff
    - Can decrease spacing at the cost of yield
    - Design rules
  - Can go from circuit to layout or layout to circuit by inspection
Admin

- HW5 out
  - Due Wednesday
- Exam back on Friday