Today

- Layout
  - Transistors
  - Gates
- Design rules
- Standard cells

Transistor

- Sizing & positioning of transistors
- Designer controls W, L
- \( t_{ox} \) fixed for process
  - Sometimes thick/thin oxide “flavors”

NMOS Geometry

- Color scheme
  - Red: gate
  - Green: source and drain areas (n type diffusion)
NMOS vs PMOS
- NMOS built on p substrate
- PMOS built on n substrate
  - Needs an N-well

PMOS Geometry
- Color scheme
  - Red: gate
  - Orange: source and drain areas (p type)
  - Green: n well
- NMOS built on p wafer
  - Must add n material to build PMOS

Body Contact
- “Fourth terminal”
- Needed to set voltage around device
  - PMOS: $V_B = V_{dd}$
  - NMOS: $V_B = GND$
- At right: PMOS (orange) with bulk contact (dark green)

Body Contact
- Needed to set voltage around device
  - PMOS: $V_B = V_{dd}$
  - NMOS: $V_B = GND$
- What happens if NMOS body contact is $V_{dd}$?
  - Polarity of field wrong
  - Won’t invert channel

Transistor Geometry
Interconnect

- Connect transistors
  - Different layers of metal
    - "Contact" - metal to transistor
    - "Via" - metal to metal

Masks

- Define areas want to see in layer
  - Think of "stencil" for material deposition
- Use photoresist (PR) to form the "stencil"
  - Expose PR through mask
  - PR dissolves in exposed area
  - Material is deposited
    - Only "sticks" in area w/ dissolved PR

Reverse Engineer Inverter Layout
How to “decode” circuit from layout? 

Where is PMOS transistor? 
Where is NMOS? 

1. Identify transistors 

Where is Input? 

Where is Input?
Inverter Layout

- Where is Output?

Layout to Circuit

- 2. Add wires
Design Rules

- Why not adjacent transistors?
  - Plenty of empty space
  - If area is money, pack in as much as possible
- Recall: processing imprecise
  - Margin of error for process variation

Design Rules

- Contract between process engineer & designer
  - Minimum width/spacing
  - Can be (often are) process specific
- Lambda rules: scalable design rules
  - In terms of $\lambda = 0.5 L_{\text{min}} \left( L_{\text{drawn}} \right)$
  - Can migrate designs from similar process

Design Rules: Some Examples

Layout #2 (practice)

- How many transistors?
  - PMOS?
  - NMOS?
- How connected?
  - PMOS, NMOS?
- Inputs connected?
- Outputs?
- What is it?

Standard Cells

- Lay out gates so that heights match
  - Rows of adjacent cells
  - Standardized sizes
- Motivation: automated place and route
  - EDA tools convert HDL to layout
**Standard Cell Area**

All cells uniform height

Width of channel determined by routing

**Standard Cell Layout Example**


**Big Idea**

- Layouts are physical realization of circuit
  - Geometry tradeoff
    - Can decrease spacing at the cost of yield
    - Design rules
  - Can go from circuit to layout or layout to circuit by inspection

**Admin**

- HW5 out
  - Due Wednesday
- Exam back on Friday