Today

- Finish Ratioed Gates (quickly)
- Example to discuss and illustrate design space
  - You will want to be exploring design space for Project 1
  - Chance to talk about trends

Ratioed Inverter

- Build NFET pulldown
  - Exploit high N mobility
  - Traditional

DC Transfer Function

\[
\text{V}_{OL} \leq 0.1 \text{V}_{dd} = 0.08V \\
\text{V}_{OH} \geq 0.9 \text{V}_{dd} = 0.72V
\]
Noise Margin Tradeoff
- What is the impact of increasing noise margin?
  - On size
  - On input capacitance

P vs. N
- Conclude: prefer N to P for ratioed logic

Ratioed Inverter Sizing
- What causes the knee in the curve at high end?

Size for $R_0/2$ drive?
- How do we size for $R_0/2$ drive?

$$R_{\text{drive}} \cdot \frac{R_w}{W_p} = 2R_w \Rightarrow W_p = 4$$
Compare Static CMOS

For $R_{\text{drive}} = R_o/2$ inverter
- Total Transistor Width?
- Input capacitance load?

Static Power

- $I_{\text{sub}}$?
- Input low-Output high?
  - $I_{\text{leak}}$
- Input high-Output low?
  - $I_{\text{pmos on}}$
  - $-V_{dd}/(R_o/2)$ -- for our sample case

Total Power

- $P_{\text{tot}} \approx a(\frac{1}{2}C_{\text{load}} + C_{\text{sc}})V^2f$

How do we size for $R_o/2$ drive?

- $R_{\text{drive}} \frac{R_{\text{on}}}{W_p} = \frac{2R_o}{W_p}$
  - $\Rightarrow W_p = 4$
How do we size for \( R_0/2 \) drive?

\[
R_{\text{drive}} = \frac{R_0}{W_p} = \frac{2R_0}{W_p} = \frac{R_0}{2}
\]

\[\Rightarrow W_p = 4\]

\[
R_{\text{drive, pull}} = \frac{2R_0}{W_n} = \frac{R_0}{W_n/2}
\]

\[W_n/2 > 8W_p\]

\[\Rightarrow W_n = 64\]
Design Space Exploration

Function: Identify equivalence of two 32bit inputs
Optimize: Minimize total energy
Assumptions: Match case uncommon
  I.e. Most of the time, the inputs won’t be matched
Deliberately focus on Energy to complement project
  …but will still talk about delay

Idea: Design Space Explore
- Identify options
  - All the knobs you can turn
- Explore space systematically
- Formulate continuum where possible
  - i.e. formulate trends

Problem Solvable
- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization
- How do we decompose the problem?
  - What look like built out of nand2 gates and inverters?

Total Power
- Static CMOS:
  \[ P_{\text{tot}} \approx \frac{a}{2} (C_{\text{load}} + C_{\text{sc}}) V^2 f + \frac{V T}{W L} e^{-V_t/(nkT/q)} \]
- Ratioed Logic:
  \[ P_{\text{tot}} \approx \frac{a}{2} (C_{\text{load}} + C_{\text{sc}}) V^2 f + \left( p(V_{\text{out}=\text{high}}) V^2 / R_{\text{out}} + (1-p(V_{\text{out}=\text{low}})) V T / (W L) e^{-V_t/(nkT/q)} \right) \]
- What can we do to reduce power?
Knobs

- What are the options and knobs we can turn?

Design Space Dimensions

- Vdd
- Topology
  - Gate choice, logical optimization
  - Fanin, fanout, Serial vs. parallel
- Gate style / logic family
  - CMOS, Ratioed (N load, P load)
- Transistor Sizing
- Vdd
- Vth

How Reduce Short-Circuit Power?

- $P_{sc} = \alpha C_{sc} V^2 f$

  $$E = V_{dd} \times \left( I_{peak} \times t_{sc} \times \left( \frac{1}{2} \right) \right)$$

Gate

- What gates might we build?
  - High fanin?
  - Serial-Parallel?

Logic Family

- Considerations for each logic family?
  - CMOS
  - Ratioed with PMOS load
  - Ratioed with NMOS load

Sizing

- How do we want to size gates?
Reduce $V_{dd}$

- What happens as $V$ decreases?
  - Energy?
  - Dynamic
  - Static
  - Switching Delay?

- How low can we push $V_{dd}$?

Reduce $V$ (no $V_{sat}$)

- $\tau_{gl} = \frac{Q}{I} = \frac{(CV)}{I}$
- $I_s = \frac{\mu C_{ox} W}{2 (W/L)} (V_{gs} - V_{th})^2$
- $\tau_{gl}$ impact?
- $\tau_{gl} \propto \frac{1}{V}$

Increase $V_{th}$?

- What is the impact of increasing threshold on?
  - Dynamic Energy?
  - Leakage Energy?
  - Delay?

Increase $V_{th}$

- $\tau_{gl} = \frac{Q}{I} = \frac{(CV)}{I}$
- $I_s = \frac{(V_{sat} C_{ox}) (W)}{2 (W/L)} (V_{gs} - V_{th} - V_{DSAT} / 2)$

Ideas

- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs
  - ...don’t over-tune

Admin

- Project
  - Should have simulated baseline
  - List of optimizations to try
    - If don’t have list talk with Hans and Tania during office hours
  - Milestone is a bare minimum
    - Really should be into exploring options this week

- Shouldn’t have to state:
  - Report should be typed with all figures, schematics, graphs, equations, etc. computer generated.
  - YOUR OWN WORK!
    - You should understand everything you turn in, and I reserve the right to test you on that.