Design Problem:

- Design a circuit to detect when 32-bit values match with the minimum energy.
  
  \[ \text{Out} = (A_{31:0} = B_{31:0}) \]

- Assume that the match is uncommon

1. How to decompose the problem?
   - bit-by-bit comparison
   - And outputs for final detection bit

2. How to perform with nand2 and inverters?
   - bit-by-bit comparison
     
     \[ A_{i} \oplus B_{i} = (A_{i} \oplus B_{i}) = 0_{i} \]

     XNOR
     
     \[ 0_{i} = A \cdot \overline{B} + \overline{A} \cdot B \]
     
     \[ = (A \cdot \overline{B}) \cdot (\overline{A} \cdot B) \]

- Diagram: 32 outputs, 16 outputs, 8 outputs, 4 outputs, ..., 1 output
3 Design one gate at the transistor level to use in the match.

\[ \text{XOR} = A \cdot \overline{B} + \overline{A} \cdot B \]

\[ \text{NAND2/INV} = (\overline{A \cdot B}) \cdot (\overline{A + B}) \]

Compare with NAND2/INV implementation.

If everything min sized:

Delay of XOR:

\[ \text{delay} = 2R_o C_o + 2R_o C_o + 4R_o C_o = 8R_o C_o = 8T \]

Delay of NAND2/INV:

\[ \text{delay} = 2R_o C_o + 2R_o C_o + 2R_o C_o + 2R_o C_o = 12R_o C_o = 12T \]

4 What can you explore? knobs?

A Gate choice:

Reduced switching
\[ P_{\text{total}} = a \left( \frac{1}{2} C_{\text{load}} + C_{sc} \right) V^2 f + V I_s \left( \frac{W}{L} \right) e^{-\frac{V_T}{n k T}} \]

- reduced activity factor by replacing nand2/inv w/ nor

B. Fanin/Fanout

32 outputs

8 outputs

2 outputs

out

- reduced switching because we know inputs don't match often.
- increased load on gates \(\Rightarrow\) Pain ↑

C. Serial vs. Parallel

- benefits as soon as mismatch is found all switching stops
- increased delay, but if we only care about power, willing to make tradeoff
3. **Radio Logic**
- Reduced $C_{load}$ results in lower switching power ($P_{dyn}$)
- Increased static power

2. **Transistor Sizing**
- Size transistor to reduce delay $\Rightarrow$ reduction in short-circuit current $\Rightarrow I_{sc} \downarrow$
- Size of transistors also affects switching loads, sized too big and $P_{dyn} \uparrow$

1. **Reduced Vdd**

Vdd $\downarrow \Rightarrow$ delay $\uparrow$
- While the rail-to-rail difference is decreased, drive currents are reduced, resulting in increased delay

Vdd $\downarrow \Rightarrow$ Power $\downarrow$
- What is limit on Vdd?

1. **$V_{TH}$**

$\Rightarrow I_{ds} \downarrow \Rightarrow P_{dyn} \downarrow$
$\Rightarrow I_{leak} \downarrow \Rightarrow P_{stat} \downarrow$
$\Rightarrow \uparrow$ delay