Today
- Memory
  - Classification
  - Architecture
  - Memory core
  - Periphery (time permitting)
- Project 2 is on this

Semiconductor Memory Classification

<table>
<thead>
<tr>
<th>RWM</th>
<th>NVRWM</th>
<th>ROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
<td>EPROM</td>
</tr>
<tr>
<td>SRAM</td>
<td>EPROM</td>
<td>Mask-Programmed Programmable (PROM)</td>
</tr>
<tr>
<td>DRAM</td>
<td>Flash</td>
<td></td>
</tr>
<tr>
<td>FIFO</td>
<td>LIFO</td>
<td></td>
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<tr>
<td>Shift Register</td>
<td>CAM</td>
<td></td>
</tr>
</tbody>
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Memory Architecture: Core

Memory Architecture: Decoders

N words => N select signals
Too many select signals
Decoder reduces # of select signals
$K = \log_2 N$
Array-Structured Memory Architecture

**Problem:** ASPECT RATIO or HEIGHT >> WIDTH

- Amplify swing to rail-to-rail amplitude
- Selects appropriate word

Latches/Register – Can Store a State

- Build master-slave register from pair of latches
- Control with non-overlapping clocks

**MOS NOR ROM**

- \( V_{DD} \) Pull-up devices

**MOS NAND ROM**

- All word lines high by default with exception of selected row
Read-Write Memories (RAM)

- **STATIC (SRAM)**
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- **DYNAMIC (DRAM)**
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended

### Gate Based Latch

- How many transistors in this latch?

### Latches/Register – Can Store a State

- Build master-slave register from pair of latches
- Control with non-overlapping clocks

### 6-transistor CMOS SRAM Cell
6-transistor CMOS SRAM Cell

Assume 1 is stored (Q=1)

Assume bitlines precharged to Vdd

Read Operation

CMOS SRAM Analysis (Read)

Assume 1 is stored (Q=1)

CMOS SRAM Analysis (Write)

Assume 1 is stored

Write 0 to cell

Periphery

- Decoders
- Sense Amplifiers
- Input/Output Buffers
- Control / Timing Circuitry

4 input pass-transistor based column decoder

- Advantage: speed (t_{pd} does not add to overall memory access time)
- only 1 extra transistor in signal path
- Advantage: large transistor count
Sense Amplifiers

\[ I_p = \frac{C \Delta V}{I_{av}} \]

- make \( \Delta V \) as small as possible
- \( I_p \) large \( \rightarrow \) small

Idea: Use Sense Amplifier

- small transition
- input
- output

<table>
<thead>
<tr>
<th>Idea</th>
</tr>
</thead>
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<tr>
<td>- Memory for compact state storage</td>
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</tbody>
</table>
| - Share circuitry across many bits
  - Minimize area per bit \( \rightarrow \) maximize density |
| - Aggressively use:
  - Pass transistors, Rationing
  - Precharge, Amplifiers
  - to keep area down |

Admin

- Homework 7 due Wednesday
- Midterm 2 solutions posted later today
- Today is withdraw date