ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 28: November 13, 2015
RAM Periphery
Today

- Memory Periphery
  - Sensing
  - Decode
  - Column Drivers
Sensing
6T SRAM Memory bit
Simulation

Precharge 6T SRAM Read

WL
bit
notbit
BL
/BL

V

S

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Sense Small Swings

- What do we have to worry about?
Sense Small Swings

- **Variation**
  - Shift where inverter “trip point” is

- **Systematic shifts that effect both bitlines**
  - “Common mode” noise
  - E.g.
    - Noise
      - Switching spikes on supplies
      - Capacitive cross talk
    - Voltage droop
Two Sense Amps

- Goal: amplify small signal difference
  reject common mode noise

Not Clocked Diff Amp

Clocked/Regenerative Feedback

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Goal:
- Reject common shift

Differential Sense Amp
Warmup

- What does this do?
- How do we size transistor?
Voltage Controlled

- Consider $V_{\text{ctrl}}$ as an analog input between 0 and $V_{\text{dd}} - V_{\text{th}}$
- What does this do?
- How does the voltage on $V_{\text{ctrl}}$ control operation?
DC Transfer

*** spice deck for cell test_inv_ratio_vctrl{sch} from library test

![Graph showing In vs. Out with different Vctrl values](image)

Vctrl=0.2  (red)
Vctrl=0.3  (green dashed)
Vctrl=0.4  (blue dashed)
Vctrl=0.5  (magenta dashed)

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Idea

- Control Resistance to control “trip point”
What does this do?

- Output when:
  - $\text{In}=\text{Gnd}$?
  - $\text{In}=V_{dd}$?
  - Transfer curve?
“Inverter”

- Input low
  - Pulls itself up
  - Until $V_{dd}-V_{TP}$
- Input high
  - Like ratioed device with $V_{ctrl}$ low
DC Transfer Function
Differential Sense Amp
Differential Sense Amp

- “se” – sense enable
  - Inputs precharged to common value
  - After read operation is initiated, one bitline begins to drop
  - After bitlines have reached sufficient differential value, se is enabled and amplifier evaluates
Differential Sense Amp

- If “se” enabled, how does bottom transistor behave?
Differential Sense Amp
Differential Sense Amp
Differential Sense Amp
Diffamp Transfer Function

- looks like “inverter” with low gain in mid region
Differential Sense Amp

- “Inverter” output controls PMOS for second inverter
- Sets PMOS operating point
  - Voltage controlled resistance
  - Sets “trip point”
Differential Sense Amp

- What happens when
  - \( \text{in}=\text{in} \)?
Differential Sense Amp

- What happens when
  - $/\text{in} > \text{in}$?
  - $/\text{in} < \text{in}$?
Differential Sense Amp

- **View:**
  - “inverter” biases to operating point
Differential Sense Amp

- View:
  - “inverter” biases to operating point
  - Biasing sets $V_{ctrl}$ for second inverter
    - Current mirror
    - Adjusts pull up resistance to set inverter “trip point”
DC Transfer $/in$ with $in=0.5V$

diffamp with $in$ at 0.5V

diffamp out after inv

$V_{out}$

$V_{in} (\text{/in})$
DC Transfer Various ins

![diffamp with different ins](image)

- in 0.3V
- in 0.4V
- in 0.5V
- in 0.6V
- in 0.7V

Vout vs Vin (/in)
DC Transfer Various in

- What is trip point when:
  - \( I_n = 0.3\text{V} \)?
  - \( I_n = 0.4\text{V} \)?
  - \( I_n = 0.5\text{V} \)?
  - \( I_n = 0.6\text{V} \)?
  - \( I_n = 0.7\text{V} \)?
After Inverter

Inverter after diffamp with different ins

- in 0.5V
- in 0.3V
- in 0.7V

Vout

Vin (/in)
Differential Sense Amp

- Does need to be sized
- There is a ratioed logic effect here
  - NMOS must overcome pullup resistance
Regenerative Feedback

- bit-lines disconnected at sensing to avoid their high capacitive load
- The regenerative feedback loop is now isolated
- When sense clock is high the values stored in bit-lines are regenerated, while the lines are disconnected, speeding up response
Decode
Memory Bank
Row Select

- Compute inversions outside array
  - Just AND appropriate line (bit or /bit)
Row Select

- Share common terms
- Multi-level decode
Row Select

- Same number of lines
- Half as many AND inputs inside the row
Row Select: Precharge NAND
Row Select: Precharge NOR
Bitline Drivers
Tristate Driver
Tristate Drivers
Idea

- Minimize area of repeated cell
- Compensate with periphery
  - Amplification (regeneration/restoration)
- Match periphery pitch to cell row/column
  - Decode
  - Sensing
  - Writer Drivers
Admin

- **Monday: in Detkin Lab**
  - Attendance and participation mandatory!
    - Can’t get HW8 points without coming to lab
  - Read lab2 assignment and HW8 before coming to class
  - HW 8 due Monday 11/23

- **Project 2 Out**
  - A lot of work. Start now.
    - Can work in pairs, and extra credit possible
  - Milestone due Wednesday 11/25
  - Final report due Friday 12/4 ➡️ UPDATED