Today
- Memory Periphery
  - Sensing
  - Decode
  - Column Drivers
- Crosstalk
  - Characterization
  - Magnitude
  - Avoiding
  - Design practices

Decode: Row Select
- Compute inversions outside array
  - Just AND appropriate line (bit or /bit)

Row Select
- Share common terms
- Multi-level decode

Row Select: Precharge NAND
Row Select: Precharge NAND

Row Select: Precharge NOR

Row Select: Precharge NOR

Column Drivers: Memory Bank

Tristate Buffer

- Typically used for signal traveling, e.g. bus
- Ideally all devices connected to a bus should be disconnected except for active device reading or writing to bus
- Use high-impedance state to simulate disconnecting

<table>
<thead>
<tr>
<th>Input</th>
<th>En</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Z</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Active-high buffer

Tristate Buffer
Tristate Inverters

8x4 Memory with column decoder

Read/Write Memory

Crosstalk
Capacitance Everywhere
- Potentially a capacitor between any two conductors
  - On the chip
  - On the package
  - On the board
- All wires
  - Package pins
  - PCB traces
  - Cable wires
  - Bit/word lines

Capacitance
- There are capacitors everywhere
- Already talked about
  - Wires modeled as a distributed RC network
  - Parasitic capacitances between terminals on transistor

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Wire Capacitance
- Changes in voltage on one wire may couple through parasitic capacitance to an adjacent wire

Wire step response
- Step response for isolated wire?
Undriven Adjacent Wire

- $V_1$ transitions from 0 to $V$
  - How big is the noise on $V_2$?

\[ I(t) = C \frac{dV(t)}{dt} \]

\[ C_1 \frac{d(V_1(t) - V_2(t))}{dt} = C_2 \frac{dV_2(t)}{dt} \]

\[ C_1 V_1(t) = (C_1 + C_2) V_2 \]

SPICE $C_1 = 10\,\text{pF}$, $C_2 = 20\,\text{pF}$

Good (?) Capacitance

- High capacitance to ground plane
  - Limits node swing from adjacent conductors

\[ V_2 = \left( \frac{C_1}{C_1 + C_2} \right) V_1 \]

Driven Adjacent Wire

- What happens when victim line is driven?
Driven Adjacent Wire

- What happens when victim line is driven?
  - Recovers with time constant: \( R_2(C_1 + C_2) \)

Magnitude of Noise on Driven Line

- Magnitude of diversion depends on relative time constants
  - \( \tau_1 << \tau_2 \)
  - \( \tau_1 >> \tau_2 \)
  - \( \tau_1 \sim \tau_2 \)

Spice: \( R_2 = 1\,\text{K}, \quad C_1 = 10\,\text{pF}, \quad C_2 = 20\,\text{pF} \)

Noise Implications

- So what if we have noise?
  - If the noise is less than the noise margin, nothing happens
  - Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
    - But glitches cause extra delay
    - Also cause extra power from false transitions
  - Dynamic logic never recovers from glitches
  - Memories and other sensitive circuits also can produce the wrong answer
Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:
  - Width
  - Spacing
  - Layer
  - Shielding

Idea

- Capacitance is everywhere
- Especially between adjacent wires
- Will get “noise” from crosstalk
- Clocked and driven wires
  - Slow down transitions
- Undriven wires voltage changed
- Can cause spurious transitions

Admin

- In lab on Friday
  - Attendance mandatory
  - Read lab handout in advance!
- HW 8 due Monday
- Proj2.M due Wednesday