ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 33: December 2, 2015
Transmission Lines
Implications

Transmission Line Agenda
- See in action in lab
- Where transmission lines arise?
- General wire formulation
- Lossless Transmission Line
- Impedance
- End of Transmission Line?
- Open, short, matched
- Termination
- Discuss Lossy
- Implications/Effects

Reminder: Transmission Line
- Data travels as waves
- Line has Impedance
- May reflect at end of line

\[ W = \sqrt{\frac{1}{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \]
\[ Z_0 = \sqrt{\frac{L}{C}} \]
\[ V = \frac{R - Z_0}{R + Z_0} \]
\[ V = \frac{2R}{R + Z_0} \]

Reminder: End of Line
- What happens at the end of the transmission line?

Source Series Termination
- What happens here?

Simulation
- Series Terminated Transmission Line

\[ Z_0 = \sqrt{\frac{L}{C}} \]
\[ \text{Delay} = 10 \text{ns} \]
Series Termination

- $R_{\text{series}} = Z_0$
- Initial voltage divider
  - Half voltage pulse propagates down line
- End of line open circuit
  - Sees single transition to full voltage (full reflection)
- Reflection returns to source and sees termination $R_{\text{series}} = Z_0$
- No further reflections

Termination Cases

- Termination in parallel at Sink

- Termination in series at Source

CMOS Driver / Receiver

- **Driver:** What does a CMOS driver look like at the source?
  - $I_{\text{drive}} = 1200 \mu A/\mu m \times 45\text{nm} = 54 \mu A$
- **Receiver:** What does a CMOS inverter look like at the sink?

CMOS Driver

- Driver: What does a CMOS driver look like at the source?
  - $I_{\text{drive}} = 1200 \mu A/\mu m @ 45\text{nm}, V_{dd} = 1V$
  - Min size:
    - $I_{\text{drive}} = 1200 \mu A/\mu m \times 45\text{nm} = 54 \mu A$
    - $R_{\text{out}} = \frac{V_{dd}}{I_{\text{drive}}} = 18 \Omega$
    - $W = 370$
    - $I_{\text{drive}} = 1200 \mu A/\mu m \times 45\text{nm} \times 370 = 20mA$
    - $R_{\text{out}} = \frac{V_{dd}}{I_{\text{drive}}} = 50 \Omega$

CMOS Receiver

- Receiver: What does a CMOS inverter look like at the sink?
Transmission Lines Specifics

Characteristics arise from their geometry

Coaxial Cable
- Inner core conductor: radius $r$
- Insulator: out to radius $R$
- Outer core shield (ground)

$$L = \left( \frac{\mu}{2\pi} \right) \ln \left( \frac{R}{r} \right)$$
$$Z_0 = \left( \frac{1}{2\pi} \right) \sqrt{\left( \frac{\mu}{\varepsilon} \right) \ln \left( \frac{R}{r} \right)}$$
- RG-58 $Z_0 = 50\,\Omega$ – networking, lab
- RG-59 $Z_0 = 75\,\Omega$ – video

Printed Circuit Board
- Stripline
  - Trace between ground planes

$$Z_0 = \left( \frac{1}{4} \right) \left( \frac{\mu}{\varepsilon} \right) \ln \left( \frac{1 + W/b}{t/b + W/b} \right)$$

Printed Circuit Board
- Microstrip line
  - Trace over single supply plane

$$Z_0 = \left( \frac{1}{2\pi} \right) \sqrt{\left( \frac{\mu}{0.475\varepsilon_r + 0.67\varepsilon_0} \right) \ln \left( \frac{4h}{0.536W + 0.67t} \right)}$$

Twisted Pair
- Category 5 ethernet cable
  - $100\,\Omega$
  - $V=0.64c_0$

Implications
(you should be able to reason about this)
Example

- 25 meter category-5e cable (100Ω, 0.64c)
- Supporting 1Gbps ethernet
  - 4 pairs at 250Mbps
- Time to send data from one end to the other?
- Time between bits at 250Mbps?
- Bits on each pair in the cable?

Pipeline Bits

- For properly terminated transmission line
  - Do not need to wait for bits to arrive at sink
  - Can stick new bits onto wire

Limits to Bit Pipelining

- What limits? (why only 250Mbps)
  - Rise time / signal distortion
  - Clocking
    - Skew
    - Jitter
  - For bus
    - Wire length differences between lines

Eye Diagrams

- Watch bits over line on scope
  - Look at distortion
  - "open" eye clean place to sample
    - Consistent timing of transitions
    - Well defined high/low voltage levels

Construct Eye Diagram

- Generate an input bit sequence pattern that contains all possible combinations of B bits (e.g., B=3 or 4), so a sequence of 2^B bits. (Otherwise, a random sequence of comparable length is fine.)
- Transmit the corresponding x[n] over the channel (2 BBN samples, if there are N samples/bit)
- Instead of one long plot of y[n], plot the response as an eye diagram: a. break the plot up into short segments, each containing KN samples, starting at sample 0, KN, 2KN, 3KN, ... (e.g., K=2 or 3) b. plot all the short segments on top of each other
Interpretation of Eye Diagram

Bad “eye”

Receiver deconvolution

Termination / Mismatch
- Wires do look like these transmission lines
- We are terminating them in some way when we connect to chip (gate)
  - Need to be deliberate about how terminate, if we care about high performance

Where Mismatch?
- Vias
- Wire corners
- Branches
- Connectors
- Board-to-cable
- Cable-to-cable

Lossless Transmission Line
- What prevents us from having a 500km cat-5 cable?
Lossless Transmission Line

- How to measure resistance across a cable?
- If resistance \( R \) across 100m cable, what is resistance across 200m cable?

Lossy Transmission Line

- Each \( R \) is a mismatched termination
- Each \( R \) is a voltage divider

\[
V_i = V \left( \frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right)
\]

\[
V_{i+1} = V \left( \frac{Z_0}{R + Z_0} \right)
\]

More Examples…

Time Permitting
Bus

- Common to have many modules on a bus
  - E.g. PCI slots
  - DIMM slots for memory
- High speed → bus lines are trans. lines

**Multi-drop Bus**

- Ideal
  - Open circuit, no load

**Multi-Drop Bus**

- Impact of capacitive load (stub) at drop?
  - If tight/regular enough, change Z of line

\[ Z_0 = \sqrt{\frac{L}{C}} \]

**Impedance Change**

- What happens if there is an impedance change in the wire? \(Z_0=75\Omega, Z_1=50\Omega\)
- What reflections and transmission do we get?

\[ V_r = \frac{R-Z_0}{R+Z_0} V_i \quad V_t = \frac{2R}{R+Z_0} V_i \]
At junction:
- Reflects
  \[ V_r = \frac{(Z_0 - Z_1)}{(Z_0 + Z_1)} V_i \]
- Transmits
  \[ V_t = \frac{Z_0}{(Z_0 + Z_1)} V_i \]

\[ V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_r \]
\[ V_i \left( \frac{2R}{R + Z_0} \right) = V_t \]

What happens at branch?
- Transmission line sees two \( Z_0 \) in parallel
  - Looks like \( Z_0/2 \)

At junction:
- Reflects
  \[ V_r = \frac{(Z_0 - Z_1)}{(Z_0 + Z_1)} V_i \]
- Transmits
  \[ V_t = \frac{Z_0}{(Z_0 + Z_1)} V_i \]

\[ V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_r \]
\[ V_i \left( \frac{2R}{R + Z_0} \right) = V_t \]

End of Branch
- What happens at end?
  - If ends in matched, parallel termination
    - No further reflections
Branch Simulation

Branch with Open Circuit?

- What happens if branch open circuit?

Branch with Open Circuit

- Reflects at end of open-circuit stub
- Reflection returns to branch
  - ...and encounters branch again
  - Send transmission pulse to both
    - Source and other branch
- Sink sees original pulse as multiple smaller pulses spread out over time

Open Branch Simulation

Transmission Line Noise

- Frequency limits
- Imperfect termination
- Mismatched segments/junctions/vias/connectors
- Loss due to resistance in line
  - Limits length
Idea

- Transmission lines
  - high-speed
  - high throughput
  - long-distance signaling
- Termination
- Signal quality

\[ w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \]

\[ Z_0 = \sqrt{\frac{L}{C}} \]

\[ V_r = V_i \left( \frac{R - Z_0}{R + Z_0} \right) \]

Admin

- Project due Friday
  - Allowed to submit in Canvas until 11:59pm
  - Submit SINGLE PDF or word DOC (can still submit in class)
  - Only one person needs to submit
  - Make sure division of labor and partner contributions are included
- Last Tania lecture Friday
- Hans Review Monday (12/7)
- Final (12/15) noon Towne 311