ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 3: September 2, 2015
Gates from Transistors (concl) and Transistor Introduction (first order)

Previously on ESE 370...
- Zero order transistor model
  - Not ideal case, but simplified model for circuit analysis and design

Today!
- Transistor first order model
  - There are always $R_s$ and $C_s$!

Preclass
- What voltage do the cases converge to?

Final Voltage?
- $R=1000 \text{ Ohm}$
- $C=10\text{pF}$
- $V_{\text{in}}$
- $V_{\text{measure}}$

Final Voltage?
- $R=1000 \text{ Ohm}$
- $C=1\text{nF}$
- $V_{\text{in}}$
- $V_{\text{measure}}$
Final Voltage?

- Bonus question: Which one will settle faster?

MOSFET – Zeroth Order Model

- Ideal Switch
  - $V_{GS} > V_{th}$ → switch is closed, conducts
  - $V_{GS} < V_{th}$ → switch is open, does not conduct
- Gate draws no current from input
  - Loads input capacitively (gate capacitance)

First Order Model

- Switch
  - Loads gate input capacitatively
  - $C_{gs}$
  - Has finite drive strength
  - $R_{on}$

Conclusion?

- DC/Steady-State
  - Ignore the capacitors
  - Look like “open circuit”
Buffer Gate (Source Follower)

- Is this a CMOS gate?

Buffer Gate (Source Follower)

- What is $V_{\text{OUT}}$ for unloaded gate?

Graph showing:
- $V_{\text{in}}$ connected to $V_{\text{out}}$ with a resistor $R = 1 \Omega$.
- Equivalent circuit gate output stage.

Gate Output Load

- What happens to $V_{\text{out}}$ when the output is loaded?

Graph showing:
- Equivalent circuit gate output stage.
- Load: $R = 1\Omega$, $R = 1000\Omega$.

Gate Output Resistive Load

- What happens when load is resistive? What is $V_{\text{OUT}}$?

Graph showing:
- Equivalent circuit gate output stage.
- Load: $R = 10\Omega$, $R = 1000\Omega$.

Gate Output Capacitive Load

- What happens when load is capacitive? What is $V_{\text{OUT}}$?

Graph showing:
- Equivalent circuit gate output stage.
- Load: $C = 1\text{pF}$.
Switch
- Loads gate input capacitively
- Draw no steady-state current
- Does not impact steady-state output voltage
- Has finite drive strength
- Could form voltage divider with resistive load
- Impacts settling time/Delay

First Order Model (I_D vs. V_GS)

First Order Model (I_D vs. V_DS)

CMOS Buffer Gate - First Order

Reminder: Zero-Order Model?

What happens when V_{in} = V_{dd} > V_{th}? 

V_{GS} = 0 > V_{th,p} 

V_{GS} = 0 < V_{th,n} 

V_{GS} = V_G - V_S = V_{dd} > V_{th,p} 

V_{GS} = V_G - V_S = V_{dd} < V_{th,n} 

V_{GS} = V_{th,p}
Zero-Order Model to Set Switches

CMOS Buffer Gate - First Order

- Leaves an RC Circuit we can analyze

CMOS Buffer Gate - First Order

- Look at intermediary node $V_2$
  - Connected to output of stage 1 and input of stage 2

CMOS Buffer Gate - First Order

- What is equivalent circuit gate output for stage 1 driving $V_2$? What is load of output for stage 1?

CMOS Buffer Gate - First Order

- Stage 1 equivalent circuit gate output
- Load on $V_2$
  - Capacitive, input of stage 2

CMOS Buffer Gate - First Order

- Stage 1 equivalent circuit gate output
- Load on $V_2$
  - Capacitive, input of stage 2
What is settling time of $V_2$ when $V_{in}$ switches from $V_{DD}$ to 0?

First-Order Model

- Includes settling times/delay
- Quasistatic behavior
  - Steady-state enough
- Voltage settling with resistive loads
  - At least some basis for reasoning

What is still missing?

- What happens at intermediate voltages
  - Input is not rail-to-rail (not just ground or $V_{dd}$ inputs)
- Details of dynamics, including...
  - Input transition is not a step
  - Intermediate drive strengths change with $V_{GS}$
- Sub-threshold operation
Design: Engineering Control

- $V_{th}$
  - Process engineer
- Drive strength ($R_{on}$)
  - Circuit engineer
  - Control with sizing transistors
- Supply voltages ($V_{dd}$)
  - Range set by process engineer
  - Detail use by circuit engineer

Wire Resistance

$R = \frac{\rho L}{A}$

- Sanity check
  - Wire twice as long = resistors in series
  - Wire twice as wide = resistors in parallel

Wire Capacitance

$C = \frac{\varepsilon d}{A}$

- Sanity check
  - Wire twice as long = capacitors in parallel
  - Wire twice as wide = capacitors in parallel

There are always Rs and Cs

- Every wire (connection) has resistance
- Every wire has capacitance
- (Every wire has inductance)
- Modeling vs. discrete components
- Dominant effects
  - $R_{big} + R_{small} \approx R_{big}$ ($R_{wire} << R_{on}$)
  - $C_{big} \parallel C_{small} \approx C_{big}$ ($C_{wire} << C_{g}$)
  - Today more likely ($C_{wire} >> C_{g}$)
Big Ideas

- MOSFET Transistor as switch
- Purpose-driven simplified modeling
  - Aid reasoning, sanity check, simplify design
- Analysis methodology
  - Zero order to understand switch state (logic)
  - First-order to get equivalent RC circuit (delay)
- New perspective on $R_s$ and $C_s$

Admin

- Diagnostic grades recorded
  - Solutions posted online
  - Make sure you understand
  - Diagnose what you need to review and study