ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 4: September 4, 2015
Regenerative Property
Today

- How do we make sure logic is robust
  - To enable design cascading gates into any (feed forward) graph and still tolerate voltage drops and noise, while maintaining digital abstraction
Outline

- Two signal problems
  - Gate Cascade failure
- Regeneration Solution
  - Transfer Curves
  - Noise Margins
  - Non-linearity
Two Problems

1. Output not go to rail
   - Stops short of $V_{dd}$ or Gnd
2. Signals may be perturbed by noise
   \[ V_x = V_{\text{ideal}} \pm V_{\text{noise}} \]
Wire Resistance

\[ R = \frac{\rho L}{A} \]

\[ R = \frac{10^{-7} \Omega \cdot m \cdot 100\mu m}{1\mu m \cdot 1\mu m} = 10\Omega \]
Wire Resistance

- 1000 µm long wire?
- 1 cm long wire?
- Length of integrated circuit chip side?
  - (we often call an IC chip a “die”)
## Die Sizes

<table>
<thead>
<tr>
<th>Chip</th>
<th>Trans.</th>
<th>Year</th>
<th>Maker</th>
<th>feature</th>
<th>mm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulldozer</td>
<td>1.2B</td>
<td>2012</td>
<td>AMD</td>
<td>32nm</td>
<td>315</td>
</tr>
<tr>
<td>Core i7</td>
<td>1.4B</td>
<td>2012</td>
<td>Intel</td>
<td>22nm</td>
<td>160</td>
</tr>
<tr>
<td>GK10 Kepler</td>
<td>7B</td>
<td>2012</td>
<td>NVIDIA</td>
<td>28nm</td>
<td>561</td>
</tr>
</tbody>
</table>

source: http://en.wikipedia.org/wiki/Transistor_count
Implications

- What does the circuit really look like for an inverter in the middle of the chip?
Die With Pads for packaging
Die With Pads for Packaging
Implications

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IR-Drop

- Since interconnect is resistive and gates pull current off the supply interconnect
  - The $V_{dd}$ seen by a gate is lower than the supply Voltage by
    - $V_{drop} = I_{supply} \times R_{distribute}$
  - Two gates in different locations
    - See different $R_{distribute}$
    - Therefore, see different $V_{drop}$
Output not go to Rail

- Due to $V_{\text{drop}}$, “rails” for two communicating gates may not match

$R_{\text{rest\_of\_chip}}$
Two Signal Problems

1. Output not go to rail
   - Is this tolerable?

2. Signals may be perturbed by noise
   - Voltage seen at input to a gate may not lower/higher than input voltage
Noise Sources?

- What did we see in lab when zoomed in on signal transition?
- Signal coupling
  - Crosstalk
- Leakage
- Ionizing particles (shot noise)
Signals will be degraded

1. Output not go to rail
   - Is this tolerable?

2. Signals may be perturbed by noise
   - Voltage seen at input to a gate may not lower/higher than input voltage

What happens to degraded signals?
Preclass

What is the output when all inputs are all 1s?
What is the output when all inputs are all 1.0 and \( \text{NAND}(A, B) = 1 - A \times B \)?
What is the output when all inputs are all 0.95 and $\text{NAND}(A, B) = 1 - A \times B$?
Degradation

- Cannot have signal degrade across cascaded gates
- Want to be able to cascade arbitrary set of gates
  - No limit on number of gates to maintain signal integrity
Gate Creed

- Gates should leave the signal “better” than they found it
  - “better” → closer to the rails
Regeneration Discipline

- Define legal inputs
  - Gate works if $V_{in}$ “close enough” to the rail

- Regeneration
  - Gate produces $V_{out}$ “closer to rail”
    - This tolerates some drop between one gate and next (between out and in)
    - Call this our “Noise Margin”

Regeneration/Restoration/Static Discipline
Noise Margin

- $V_{OH}$ – output high
- $V_{OL}$ – output low
- $V_{IH}$ – input high
- $V_{IL}$ – input low

- $NM_H = V_{OH} - V_{IH}$
- $NM_L = V_{IL} - V_{OL}$
Regeneration Discipline (getting precise)

- Define legal inputs
  - Gate works if $V_{in}$ “close enough” to the rail
  - $V_{in} > V_{IH}$ or $V_{in} < V_{IL}$

- Regeneration
  - Gate produces $V_{out}$ “closer to rail”
    - $V_{out} < V_{OL}$ or $V_{out} > V_{OH}$
Transfer Function

- What gate is this?

\[ V_{out} = f(V_{in}) \]
Regenerating Transfer Function

- Use gain (i.e. slope) to define noise margins

![Graph showing Vout vs. Vin with labels Vdd, V_{OH}, V_{IH}, V_{IL}, V_{OL}, V_{IN}, NM_L, NM_H]
Decomposing

- What is gain? 
  \[ \frac{\Delta V_{out}}{\Delta V_{in}} > 1 \]
- Where is there gain?
- Where is there **not** gain?
- Dividing point?
Decomposing

- What is gain?
  \[ \left| \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \right| > 1 \]
- Where is there gain?
- Where is there **not** gain?
- Dividing point?

\[
\left. \frac{\delta V_{\text{out}}}{\delta V_{\text{in}}} \right|_{V_{IL}} = \left. \frac{\delta V_{\text{out}}}{\delta V_{\text{in}}} \right|_{V_{IH}} = -1
\]

\[
V_{OH} = f(V_{IL})
\]

\[
V_{OL} = f(V_{IH})
\]
Decomposing

- An input closer to rail than $V_{IL}$, $V_{IH}$ doesn’t make much difference on $V_{out}$
  - i.e transfer function is flat close to rails
- Defining $V_{IL}$ lower ($V_{IH}$ higher) would reduce NMs and increase our undefined region

\[
\frac{\delta V_{out}}{\delta V_{in}} \bigg|_{V_{IL}} = \frac{\delta V_{out}}{\delta V_{in}} \bigg|_{V_{IH}} = -1
\]

$V_{OH} = f(V_{IL})$
$V_{OL} = f(V_{IH})$
Transfer Function for Multiple Inputs

$$V_{out} = f(V_{in1}, V_{in2})$$
Controlling Input

- Consider a nor2 gate
  - If want A to control the output
  - What value should B be?

- We call B the **non-controlling** input since it does not determine the output

- What should the non-controlling input value be for a nand2 gate?
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<th>NOR</th>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
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<td>0</td>
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<td>0</td>
</tr>
<tr>
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<td>1</td>
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Controlling Input for Worst Case

- Consider a nand2 gate
  - If want A to control the output
  - What value should B be?
    - $V_{IL}$, $V_{IH}$
Ideal Transfer Function for Inverter

![Graph showing the ideal transfer function for an inverter, with voltage levels Voh, Vdd, Vih, Vil, Vol, Vin, and Vout.]
Linear Transfer Function?

- \( V_{out} = V_{dd} - V_{in} \)

Noise Margin?
Linear Transfer Function?

- Consider two in a row (buffer)

\[ V_{\text{out1}} = V_{\text{dd}} - V_{\text{in1}} \]

- What is transfer function to buffer output \( V_{\text{out2}} \)?

\[ V_{\text{out2}} = V_{\text{dd}} - V_{\text{out1}} = V_{\text{dd}} - (V_{\text{dd}} - V_{\text{in1}}) = V_{\text{in1}} \]

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Linear Transfer Function?

- For buffer: $V_{out2} = V_{in1}$
- Consider a chain of buffers
- What happens if $V_{in1}$ drops $\Delta$ volts between each buffer?

$$A_{i+1} = A_i - \Delta$$

**Conclude:** Linear transfer functions do not provide restoration.
Linear Transfer Function?

- For buffer: \( V_{\text{out2}} = V_{\text{in1}} \)
- Consider a chain of buffers
- What happens if \( V_{\text{in1}} \) drops \( \Delta \) volts between each buffer?

\[ A_{i+1} = A_i - \Delta \]

**Conclude:** Linear transfer functions do not provide restoration.
Non-linearity

- **Need** non-linearity in transfer function
- Could not have built restoring gates with R, L, C circuit
  - R, L, C are all linear elements
Transistor Non-Linearity

- Linear region
- Saturation region

Drain to source voltage [V] vs. Drain current [arbitrary unit]

Gate to source voltage [V] vs. Drain current [arbitrary unit]
All Gates

- If we hope to assemble design from collection of gates,
  - Voltage levels must be consistent and supported across all gates
  - Must adhere to a $V_{\text{IL}}$, $V_{\text{IH}}$, $V_{\text{OL}}$, $V_{\text{OH}}$ that is valid across entire gate set of digital circuit

\[
V_{\text{ol}} = \max_{g \in G} (g \cdot V_{\text{ol}}) \quad V_{\text{il}} = \min_{g \in G} (g \cdot V_{\text{il}})
\]

\[
V_{\text{oh}} = \min_{g \in G} (g \cdot V_{\text{oh}}) \quad V_{\text{ih}} = \max_{g \in G} (g \cdot V_{\text{ih}})
\]
Big Idea

- Need robust logic
  - Can design into any (feed forward) graph with logic gates and tolerate loss and noise, while maintaining digital abstraction

- Regeneration and noise margins
  - Every gate makes signal “better”
  - Design level of noise tolerance

\[
\begin{align*}
V_{IL} & \quad V_{IH} \\
V_{OL} & \quad V_{OH}
\end{align*}
\]

\[
\begin{align*}
NM_L & \quad NM_H
\end{align*}
\]
Admin

- Monday, Labor Day – no class
- Wednesday
  - HW 2 due
    - Explain your data. If you don’t like your data, redo and get new data.
  - SpaceX speaker ~20 minutes
  - Lab ~40 min
    - Might need to finish on own time.
    - Use Piazza for technical difficulty questions!
  - Read through HW3 before lab
    - Transfer library/schematics to eniac
    - Be ready to run electric and spice on linux
      - Use CETS machines in lab or your own laptop that you bring with you