Delay is RC Charging

Strategy:
- Use zero-order model to understand switch state
- Break into output/input stages
- For each stage
  - Understand $R_{drive}$
  - Understand $C_{load}$

Today
- RC Charging
  - RC Step Response Curve
- What is the $C$?
  - Capacitive Load on Gate Output
- What is the $R$?
  - Equivalent Output Resistance
- Approximating and Measuring Delay

90% Rise Time?

$R=1000\text{ Ohm}$

$C=1\text{fF}$

What is time constant, $\tau$?

What does response look like?

~ 2ps for 90% rise
Governing Equations? (KCL)

- KCL @ \( V_{\text{measure}} \)
  - Kirchhoff's Current Law
  - Sum of all currents into a node = 0
  - Current entering a node = current exiting a node

\[
K_V @ \text{measure}
\]

- \( \text{Kirchoff's Current Law} \)
- Sum of all currents into a node = 0
- Current entering a node = current exiting a node

\( I_R = I_C \)

\[
I_R = \frac{V_C}{R} = C \frac{dV_C}{dt}
\]

\[
\frac{V_C - V_{\text{measure}}}{R} = C \frac{dV_{\text{measure}}}{dt}
\]

What does look like?

Shape of Curve

<table>
<thead>
<tr>
<th>( t ) (in ps)</th>
<th>( e^{-t/RC} )</th>
<th>( 1-e^{-t/RC} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.3</td>
<td></td>
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\[
V_{\text{measure}} = V_{\text{in}} \left( 1 - \left( e^{-t/RC} \right) \right)
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### Shape of Curve

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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0.1</td>
<td>0.9</td>
<td>0.1 10%</td>
</tr>
<tr>
<td>1</td>
<td>$1/e = 0.37$</td>
<td>0.66</td>
</tr>
<tr>
<td>2</td>
<td>$1/e^2 = 0.14$</td>
<td>0.86</td>
</tr>
<tr>
<td>2.3</td>
<td>0.1</td>
<td>0.9 90%</td>
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$V_{in} = 1$

$$V_{measure} = V_{in}(1 - (e^{-t/RC}))$$

### Rise Time: 10—90%

$$T_{rise} \approx 2.2 \text{ps} \approx 2.2 \tau$$

### What is C?

- Capacitance
- Wire
- Fanout: Total gate load
  - Logical Gate
  - MOSFET gate

### Fanout

- Number of things to which a gate output connects
Fanout in Circuit

- Output routed to many gate inputs

Fanout in Circuit

- Maximum fanout?
- Second?
- Min?
MOSFET Capacitance

"load of 1"?
- Capacitive

First Order Model

Switch
- Loads input capacitively

Lumped Capacitive Load

\[ C_{load} = \sum_{i \in \text{fanout}} C_{g_i} + \sum_{i \in \text{wires}} C_{w_i} \]
Wire resistance
- From supply (Vdd or Gnd) to transistor source
- From transistor output to gate it is driving
- Transistor equivalent resistance \( R_{on} \)

First Order Model
- Switch
  - Resistive driver
- As we dig into the device structure understand:
  - More sophisticated view, not just \( R_{ON} \)
  - How to engineer device parameters like \( C_g, R_{ON}, V_{th} \)
- Tradeoffs

Equivalent Resistance

What resistances might transistors contribute?
- How many cases?
- Assume \( R_{on} = R_{on,p} = R_{on,n} \)

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</tr>
<tr>
<td>01</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
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<tr>
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<td>( R_{on} )</td>
</tr>
<tr>
<td>10</td>
<td>( R_{on} )</td>
</tr>
<tr>
<td>11</td>
<td>( 2R_{on} )</td>
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 Rise/Fall Times

- Rise and Fall time may differ
  - Why?
  - What is ratio?

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Lumped Resistive Source

\[ R_{\text{drive}} = R_{\text{tr,net}} + \sum_{i\in\text{wires}} R_{w_i} \]

\( R_{\text{tr,net}} \) = transistor network resistance = parallel and series combination of \( R_{w} \)

Voltage Waveform at Input/Output Node

\( R_{\text{drive}} \) from output stages and wires
\( C_{\text{Load}} \) from input stages and wires

Measuring Delay

\( t_{\text{del}} = 13\text{ps} \)

Next stage starts to switch before first finishes
Measure from 50% of input swing to 50% of output swing

Characterizing Gate/Technology

- Delay measure will be
  - Function of load on gate
  - Function of input rise time
  - Which, in turn, may be a function of input loading
Delay vs. Risetime

- If we didn’t know the input rise time, we wouldn’t know what a 15ps delay meant.

Characterizing Gate/Technology

- Delay measure will be:
  - Function of load on gate
  - Function of input rise time
  - Which, in turn, may be a function of input loading
- Want to understand typical delay times:
  - Allows us to compare designs with a (somewhat) normalized delay metric.

Standard Measurement for Characterization

- Drive with a gate:
  - Not an ideal source
  - Input rise time typically would see in circuit
- Measure loaded gate:
  - Typical loading – FO4

HW3 Measurement Setup

- Measure loaded gate:
  - Typical loading – FO4 (how does delay change if gate is unloaded?)

Measurement for Characterization

- Drive with a gate:
  - Not an ideal source (how does delay change if drive is ideal?)
  - Input rise time typically would see in circuit
- Measure loaded gate:
  - Typical loading – FO4
Delay is RC Charging

Admin

- “Normal Week”
  - 3 Lecture Week (all here)
  - MOS Operation and Devices
- Spice Flow
  - access to electric, setup for spice, run ngspice
- HW quality
  - Show your work
  - Label axes, explain your results
  - If we can’t understand it, we can’t grade it
- HW turnin
  - Must turn in by the time I start lecturing (12:05)
  - Won’t accept any more after that