Lec 7: September 16, 2015
MOS Transistor Operating Regions
Part 1
Today

- PN Junction
- MOS Transistor Topology
- Threshold
- Operating Regions
  - Resistive
  - Saturation
  - Subthreshold (next class)
  - Velocity Saturation (next class)
Last Time – MOS model
Refinement

- Depletion region $\rightarrow$ excess carriers depleted
Bulk/Body Contact

- MOS actually has four contacts
- Also effects fields
- Usually common across transistors
  - Gnd for nmos, $V_{dd}$ for pmos
No Field

- $V_{GS}=0$, $V_{DS}=0$
Apply $V_{GS} > 0$

- Accumulate negative charge
  - Repel holes (fill holes)
Channel Evolution -- Increasing $V_{gs}$

The diagrams illustrate the channel evolution in a MOSFET as the gate voltage ($V_{gs}$) increases. The depletion region expands from the initial state (left) to a fully depleted state (right) as $V_{gs}$ is increased. The depletion region is indicated by a darker shade of green in the $n^+$ regions of the $p$-substrate.
Gate Capacitance

Changes based on operating region.
Gate Capacitance

- Depletion capacitance dependent on width of depletion region and potential at oxide-silicon border
Channel Evolution -- Increasing Vgs
Inversion

- Surface builds electrons
  - Inverts to n-type
  - Draws electrons from n\(^+\) source terminal
Threshold

- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \approx 2\phi_F$
  - Engineer by controlling doping ($N_A$) $\phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right)$
Linear Region
Linear Region

- $V_{GS} > V_{th}$ and $V_{DS}$ small

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$
Linear Region

- $V_{GS} > V_{th}$ and $V_{DS}$ small
- $V_{GS}$ fixed $\rightarrow$ looks like resistor
  - Current linear in $V_{DS}$

\[
I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

\[
I_{DS} \approx \mu_n C_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_{th}) V_{DS}
\]

\[
I_{DS} \propto V_{DS}
\]
MOSFET – IV Characteristics

\[ V_{DS} < V_{GS} - V_{TH} \]

\[ V_{DS} \geq V_{GS} - V_{TH} \]

\[ V_{GS} - V_{th} = 7 \text{ V} \]

\[ V_{GS} - V_{th} = 6 \text{ V} \]

\[ V_{GS} - V_{th} = 5 \text{ V} \]

\[ V_{GS} - V_{th} = 3 \text{ V} \]

\[ V_{GS} - V_{th} = 2 \text{ V} \]

\[ V_{GS} - V_{th} = 1 \text{ V} \]
Dimensions

- Channel Length (L)
- Channel Width (W)
- Oxide Thickness ($T_{ox}$)
Preclass

- $I_{ds}$ for identical transistors in parallel?
I\textsubscript{ds} for identical transistors in series?
- (V\textsubscript{ds} small)
Transistor Strength (W/L)

\[ C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \]

\[ I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \]
Transistor Strength (W/L)

- Shape dependence match Resistance intuition
  - Wider = parallel resistors $\rightarrow$ decrease R
  - Longer = series resistors $\rightarrow$ increase R

\[ R = \frac{\rho L}{A} \]

\[ I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \]
\( L_{\text{drawn}} \) vs. \( L_{\text{effective}} \)

- Doping not perfectly straight
- Spreads under gate
- Effective \( L \) smaller than draw gate width
Channel Voltage

- Voltage varies along channel
- Think of channel as resistor
What is voltage in the middle of a resistive medium? 
(halfway between terminals)
Voltage in Channel

- Think of channel as resistive medium
  - Length = L
  - Area = Width * Depth (inversion)
- What is voltage in the middle of the channel?
  - L/2 from S and D?
Channel Voltage

- Voltage varies along channel
- If think of channel as resistor
  - Serves as a voltage divider between $V_S$ and $V_D$
Voltage along Channel

- What does voltage along the channel look like?

\[ V(x) \]

\[ x = 0 \quad x = L \]
What does voltage along the channel look like?
What does voltage along the channel look like?

\[ V(x) = V_d \]

Voltage along Channel

\[ x = 0 \quad x = L \]

p-substrate

depletion region

G

S

D

n^+
What does voltage along the channel look like?

\[ V(x) = V_d \]

\[ V_s \]

\[ x = 0 \]
\[ x = L \]
Channel Field

- When voltage gap $V_G - V_x$ drops below $V_{th}$, drops out of inversion
  - If $V_{DS} = V_{GS} - V_{th}$, then $V_{DS} - V_{GS} = V_{th}$
Channel Field

- When voltage gap $V_G - V_x$ drops below $V_{th}$, drops out of inversion
  - What if $V_{DS} > V_{GS} - V_{th} \Rightarrow V_{DS} - V_{GS} > V_{th}$?
    - Upper limit on current, channel is “pinched off”
Pinch Off

- When voltage along the channel drops below $V_{th}$, the channel drops out of inversion
  - Occurs when: $V_{GS} - V_{DS} < V_T \Rightarrow V_{DS} > V_{GS} - V_{th}$

- Conclusion:
  - Current cannot increase with $V_{DS}$ once $V_{DS} > V_{GS} - V_T$
Saturation

- In saturation, $V_{DS\text{-effective}} = V_x = V_{GS} - V_T$

$$I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T)^2 - \frac{(V_{GS} - V_T)^2}{2} \right]$$

$$I_{DS} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T)^2 \right]$$
MOSFET – IV Characteristics

\[ V_{DS} < V_{GS} - V_{TH} \] linear region

\[ V_{DS} \geq V_{GS} - V_{TH} \] saturation region

\[ V_{GS} - V_{th} = 7 \text{ V} \]

\[ V_{GS} - V_{th} = 6 \text{ V} \]

\[ V_{GS} - V_{th} = 5 \text{ V} \]

\[ V_{GS} - V_{th} = 3 \text{ V} \]

\[ V_{GS} - V_{th} = 2 \text{ V} \]

\[ V_{GS} - V_{th} = 1 \text{ V} \]
Approach

- Identify Region
- Drives governing equations
  - See preclass reference
- Use region and equations to understand operation
Big Idea

- 3 Regions of operation for MOSFET
  - Subthreshold
  - Linear
  - Saturation
Admin

- Text 3.3.2 – highly recommend read!!
  - Second half on Friday
- HW4 out
  - Get started over weekend
  - Long and time-consuming