ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 8: September 18, 2015
MOS Transistor Operating Regions
Part 2
Today

- Operating Regions (continued)
  - Resistive
  - Saturation
  - Velocity Saturation
  - Subthreshold
- Drain Induced Barrier Lowering
  - $V_{th}$
Last Time...
Channel Evolution - Increasing Vgs
Threshold

- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \sim 2\phi_F$
  - Engineer by controlling doping ($N_A$) $\phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right)$
Linear Region

- \( V_{GS} > V_{th} \) and \( V_{DS} \) small

\[
I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

\[
C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}
\]
Voltage along Channel

- What does voltage along the channel look like?

\[ V(x) = V_s + \frac{V_d - V_s}{L} x \]

\[ V_g - V(x) = V_g - V_s + \frac{V_d - V_s}{L} x \]
Channel Field

- When voltage gap $V_G - V_x$ drops below $V_{th}$, drops out of inversion
  - What if $V_{DS} > V_{GS} - V_{th} \Rightarrow V_{DS} - V_{GS} > V_{th}$?
    - Upper limit on current, channel is “pinched off”

$$V_G - V(x) = V_G - V_S + \frac{V_D - V_S}{L}x = V_T$$

$$x = \frac{V_G - V_S - V_T}{V_D - V_S}L = \frac{V_{GS} - V_T}{V_{DS}}L$$

$V_{DS} > V_{GS} - V_T \Rightarrow x < L$

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Saturation

- In saturation, $V_{DS-effective} = V_x = V_{GS} - V_T$

$$I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T)^2 - \frac{(V_{GS} - V_T)^2}{2} \right]$$

$$I_{DS} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T)^2 \right]$$
MOSFET – IV Characteristics

\[ V_{DS} < V_{GS} - V_{TH} \]

linear region

\[ V_{DS} \geq V_{GS} - V_{TH} \]

saturation region

\[ V_{GS} - V_{th} = 7 \text{ V} \]

\[ V_{GS} - V_{th} = 6 \text{ V} \]

\[ V_{GS} - V_{th} = 5 \text{ V} \]

\[ V_{GS} - V_{th} = 3 \text{ V} \]

\[ V_{GS} - V_{th} = 2 \text{ V} \]

\[ V_{GS} - V_{th} = 1 \text{ V} \]
New Stuff
Preclass 1

- What is electrical field in channel?

  \[ L_{\text{eff}} = 25 \text{nm}, V_{DS} = 1V \]
  \[ Field = \frac{V_{DS}}{L_{\text{eff}}} \]

- Velocity:

  \[ v = F \cdot \mu_n \]

- Electron mobility: \( \mu_n = 500 \text{cm}^2 / (V \cdot s) \)

- What is electron velocity?
Moving Charge

\[ I = \left( \frac{1}{R} \right) V \]

- I increases linearly in V

Field = \( \frac{V_{DS}}{L_{eff}} \), \( v = \mu_n \cdot F \)

\[ v = \mu \cdot \frac{V_{DS}}{L_{eff}} = \left( \frac{\mu_n}{L_{eff}} \right) V_{DS} \]

- Velocity increases linearly in V

- What’s I?
  - \( \Delta Q / \Delta t \)
  - Speed at which charge moves

- What’s a moving electron?
Short Channel

- Model assumes carrier velocity increases with field
  - Increases with voltage
- Are there limits to how fast things (including electrons) can move?

![Speed Limit Sign](image)

3 \times 10^5 km/sec
Short Channel

- Model assumes carrier velocity increases with field
  - Increases with voltage
- There is a limit to how fast carriers can move
  - Limited by scattering effects
    - $\sim 10^5$ m/s
- How does this relate to preclass 1b calculated velocity?
- Encounter *velocity saturation* when channel short
  - Modern processes, L is short enough to reach this region of operation
Velocity Saturation

- At what voltage do we hit the speed limit? (preclass 1d)
  - $V_{\text{dsat}} =$ voltage at which velocity (current) saturates
Velocity Saturation

- Once velocity saturates:

\[
I_{DS} = \mu_n C_{OX} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

\[
V_{DS} = V_{DSAT} \quad \Rightarrow \quad I_{DS} = \left( \mu_n \frac{V_{DSAT}}{L} \right) C_{OX} W \left[ (V_{GS} - V_{th}) - \frac{V_{DSAT}}{2} \right]
\]

\[
V_{DSAT} \approx \frac{L\nu_{SAT}}{\mu_n} \quad \Rightarrow \quad I_{DS} \approx \nu_{sat} C_{OX} W \left[ (V_{GS} - V_{th}) - \frac{V_{DSAT}}{2} \right]
\]
Velocity Saturation

- **Long Channel**

- **Short Channel**
Velocity Saturation

\[ V_{GS} = V_{DD} \]

Long channel devices

Short channel devices

\[ V_{DSAT} \quad V_{GS-V_T} \]
Velocity Saturation

- Once velocity saturates we can still increase current with parallelism
  - Effectively make a wider device
Subthreshold
Below Threshold

- Transition from insulating to conducting is non-linear, but not abrupt
- Current does flow
  - But exponentially dependent on $V_{GS}$
Subthreshold

If \( V_{GS} < V_{th} \),

\[
I_{DS} = I_S \left( \frac{W}{L} \right) e^{\frac{V_{GS}-V_{th}}{nkT/q}} \left( 1 - e^{\frac{V_{DS}}{kT/q}} \right) (1 + \lambda V_{DS})
\]

- Current is from the parasitic NPN BJT transistor when gate is unbiased and there is no conducting channel.
Subthreshold

- W/L dependence follow from resistor behavior (parallel, series)
  - Not shown explicitly in text
- \( \lambda \) is a channel-length modulation parameter
  - Defined empirically

\[
I_{DS} = I_S \left( \frac{W}{L} \right) e^{\left( \frac{V_{GS} - V_{th}}{n k T / q} \right)} \left( 1 - e^{\left( \frac{V_{DS}}{k T / q} \right)} \right) \left( 1 + \lambda V_{DS} \right)
\]
Steady State

- What current flows in steady state?
- What causes (and determines) the magnitude of current flow?
- Which device?
Leakage

- Call this steady-state current flow leakage
- $I_{ds_{leak}}$
Subthreshold Slope

- Exponent in $V_{GS}$ determines how steep the turnon is

\[ S = n \left( \frac{kT}{q} \right) \ln(10) \]

- Units: V/dec
- Every S Volts, $I_{DS}$ is scaled by factor of 10

\[ I_{DS} = I_s \left( \frac{W}{L} \right) e^{\left( \frac{V_{GS} - V_{th}}{nkT/q} \right)} \left( 1 - e^{\left( \frac{V_{DS}}{kT/q} \right)} \right) \left( 1 + \lambda V_{DS} \right) \]
Subthreshold Slope

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$$S = n \left( \frac{kT}{q} \right) \ln(10)$$

- Units: V/dec
- Every S Volts, $I_{DS}$ is scaled by factor of 10

- $n$ – depends on electrostatics
  - $n=1 \Rightarrow S=60\text{mV}$ at Room Temp. (ideal)
  - $n=1.5 \Rightarrow S=90\text{mV}$
  - Single gate structure showing $S=90-110\text{mV}$
\( I_{DS} \) vs. \( V_{GS} \)

(Logscale)
$I_{DS}$ vs. $V_{GS}$

(Logscale)
Subthreshold Slope

- If $S=100\text{mV}$ and $V_{\text{th}}=300\text{mV}$, what is $I_{\text{ds}}(V_{\text{gs}}=300\text{mV})/I_{\text{ds}}(V_{\text{gs}}=0\text{V})$?

- What if $S=60\text{mV}$?

\[ S = n \left( \frac{kT}{q} \right) \ln(10) \]

\[ I_{\text{DS}} = I_{S} \left( \frac{W}{L} \right) e^{\left( \frac{V_{GS}-V_{\text{th}}}{nkT/q} \right)} \left( 1 - e^{\left( \frac{V_{DS}}{kT/q} \right)} \right) \left( 1 + \lambda V_{DS} \right) \]
Threshold
Threshold

- Describe $V_T$ as a constant
- Induce enough electron collection to invert channel
$V_{DS}$ impact

- In practice, $V_{DS}$ impacts state of channel
$V_{DS}$ impact

- Increasing $V_{DS}$, already depletes portions of channel
$V_{DS}$ impact

- Increasing $V_{DS}$, already depletes portions of channel
- Need less charge, less voltage to create inversion layer

![Diagrams showing the impact of $V_{DS}$ on channel depletion and inversion layer creation.](image-url)
Drain-Induced Barrier Lowering (DIBL)
DIBL Impact
In a Gate?

- What does it impact most?
  - Which device, has large $V_{ds}$?
    - $V_{in} = V_{dd}$?
    - $V_{in} = Gnd$?
  - How effect operation?
    - Speed of switching?
    - Leakage?
In a Gate

- $V_{DS}$ largest for output charging/discharging device
  - Easier to turn on

$$I_{DS} \approx \nu_{sat} C_O X W \left( V_{GS} - V_{th} - \frac{V_{DSAT}}{2} \right)$$
In a Gate

- $V_{DS}$ largest for off device
  - Easier to turn on
  - Leak more

\[
I_{DS} = I_S \left( \frac{W}{L} \right) e^{\left( \frac{V_{GS}-V_{th}}{nkT/q} \right)} \left( 1 - e^{\left( \frac{V_{DS}}{kT/q} \right)} \right) \left( 1 + \lambda V_{DS} \right)
\]
PMOS

- Analogous phenomena to NMOS
- Signs different
  - Negative $V_{th}$
- Reason based on oppositely charged carriers
Big Idea

- 3 Regions of operation for MOSFET
  - Subthreshold
  - Linear
  - Saturation
    - Pinch Off
    - Velocity Saturation, DIBL
    - Short channel
Text 3.3.2 – highly recommend read

Office Hours: M (Khanna), T (Giesen)

HW4 due Wednesday
  • If you haven’t looked at it yet, you’re behind!

Midterm 1 Review session on Thursday
  • 5pm? 6pm? 7pm?

Midterm 1 Monday 9/28
  • No Lecture
    • All online with and without answers
    • Suggest start without answers