

University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021

Final

Friday, December 17

- Problem weightings shown.
- Calculators allowed.
- Closed book = No text or notes allowed.
- Additional workspace in exam book. Note where to find work in exam book if relevant.

Name:

Q1	
Q2	
Q3	
Q4	
Q5	
Total	

Default technology:

- 22nm Low Standby Power Process (LSTP)
- $\gamma = 1$
- $V_{dd}=1V$
- nominal $V_{thn} = -V_{thp}=300mV$
- $C_0 = 2 \times 10^{-17}F$ (for $W = 1$ device)
- $I_{d,sat_0} = 10\mu A$ (for $W = 1$ device)
- $I_{sd,leak_0} = 0.3$ pA (for $W = 1$ device)
- velocity saturated operation
- $R_{wire} = 700K\Omega/cm$
- $C_{wire} = 1.7pF/cm$

Transmission line:

$$w = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\epsilon_r \mu_r}} \quad (1)$$

$$Z_0 = \sqrt{\frac{L}{C}} \quad (2)$$

$$V_r = V_i \left(\frac{R - Z_0}{R + Z_0} \right) \quad (3)$$

$$V_t = V_i \left(\frac{2R}{R + Z_0} \right) \quad (4)$$

Timing constraints:

$$T \geq t_{clk \rightarrow q} + t_{plogic} + t_{setup} \quad (5)$$

$$t_{cdlatch} + t_{cdlogic} \geq t_{hold} \quad (6)$$

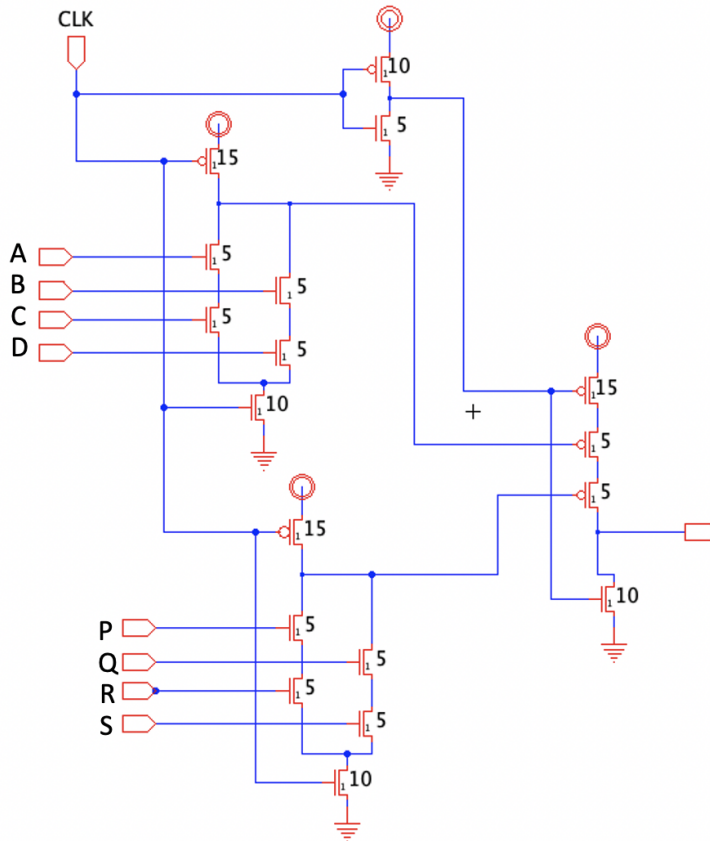
Optimal buffering:

$$L_{seg} = 2\sqrt{\frac{R_0(\gamma + 1)C_0}{R_{wire}C_{wire}}} \quad (7)$$

$$W_{buf} = \sqrt{\frac{R_0C_{wire}}{2R_{wire}C_0}} \quad (8)$$

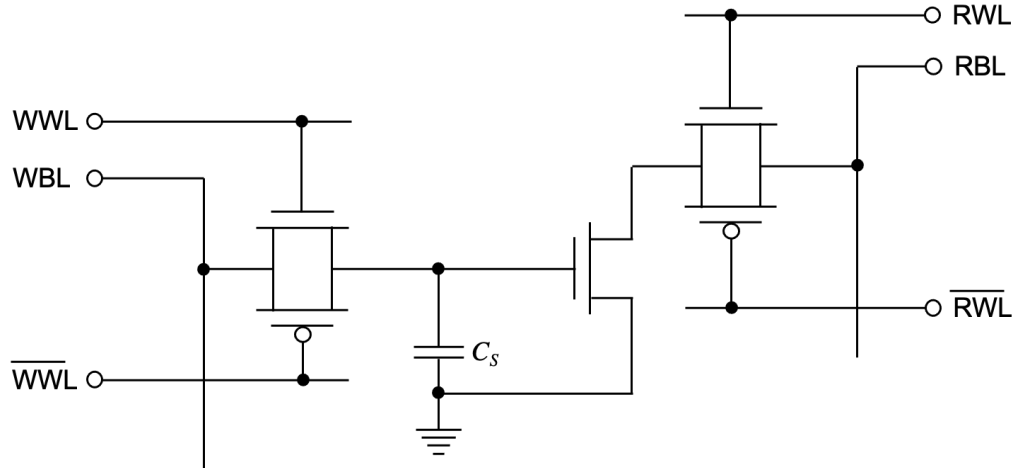
- (15pts) Consider the following dynamic logic circuit. What logic function does it evaluate?

Assume the circuit is loaded by $10C_0$ output. Assume $C_{diff} = 0.5C_{gate}$, $\mu_n = 2\mu_p$. Assume the CLK signal is driven strongly such that the rise time on the clock is R_0C_0 . Use Elmore delay calculations where appropriate. For full credit (and partial credit consideration) show your delay components (stages, components of Elmore delay calculation).



Out as a function of the inputs: A, B, C, D, P, Q, R, S?	
Evaluate Delay in units of τ (show delay components)	
Precharge Time	

2. (25pts) Assume we have a 5-transistor bitcell as shown below. It is used to design a memory with 32 words of 16 bits each. The storage capacitor C_S is not an explicit capacitor and is equal to the parasitic capacitance at that node from the cell transistors (you can ignore any wiring parasitics). Assume all bitlines are driven with minimum size buffers during a write, and pre-charged to V_{dd} during a read. All driving/pre-charging is fully complete before any wordlines are raised. $V_{dd} = 1V$ and $\gamma = 0.5$.

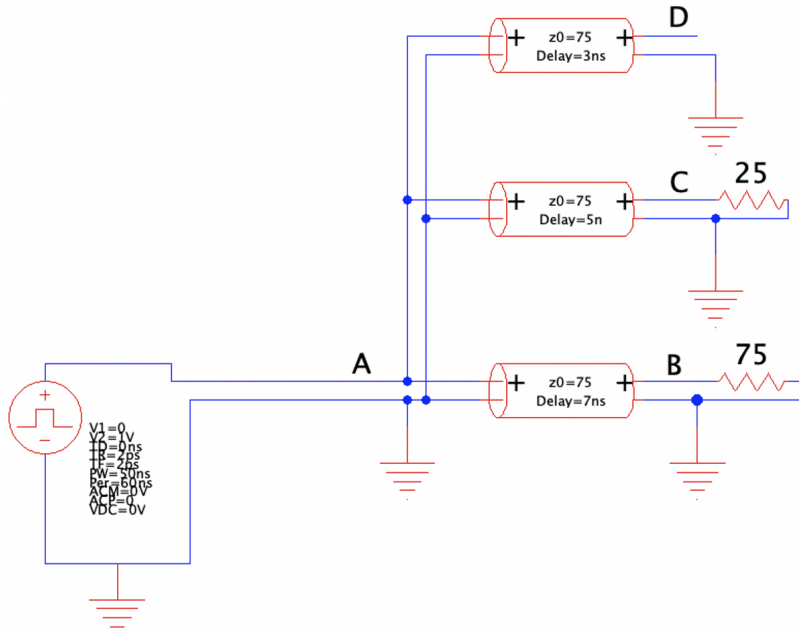


(a) Is this a SRAM or DRAM cell? Explain your reasoning?

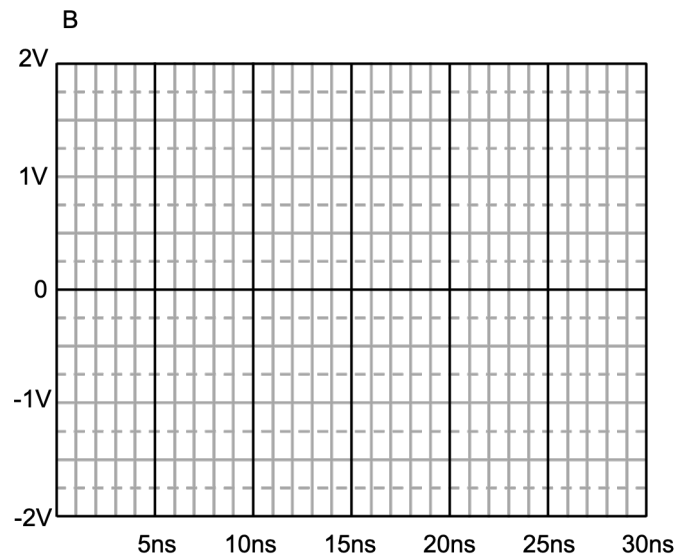
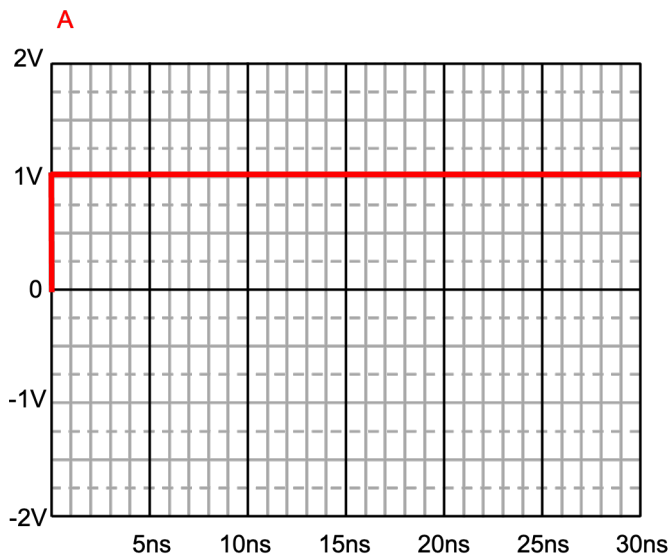
(b) What is the worst case delay after the wordline is raised to write into the cell in units of τ ?

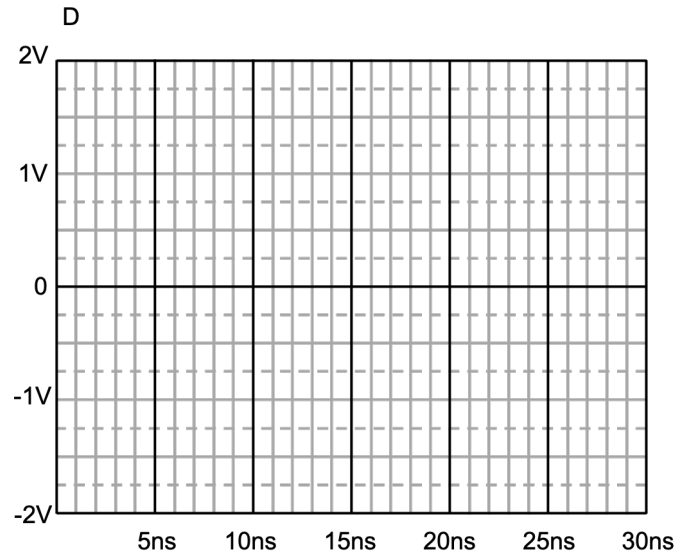
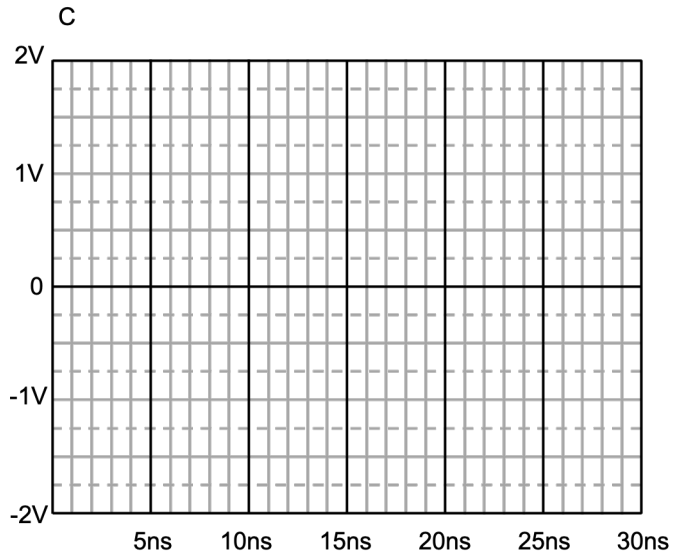
- (c) What voltage does RBL evaluate to when reading a 0? What is the delay after the wordline is raised in units of τ when reading a 0? (You can assume any column driver capacitance is negligible)
- (d) What voltage does RBL evaluate to when reading a 1? What is the delay after the wordline is raised in units of τ when reading a 1? (You can assume any column driver capacitance is negligible)

3. Transmission Line Termination (20pts). A single IC driving 3 ICs connected with PCB traces on a PCB is modeled as 3 transmission lines with matched termination. However, after manufacturing the termination of the three lines have varied and are given in the model below. The schematic shows a source end, *A*, and three destinations, *B*, *C*, and *D*. The intent of the design is for the waveforms on *B*, *C* and *D* to be identical in shape to the source waveform with some propagation delay. Reminder: The ideal voltage source looks like a short circuit.



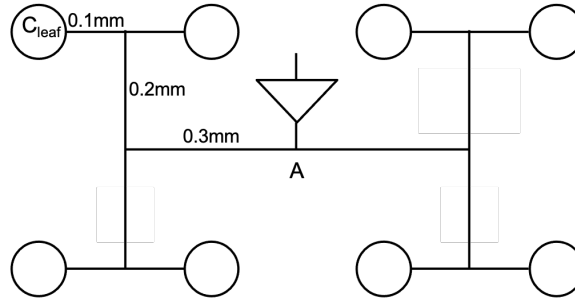
- (a) Given the source waveform is a 1V step at 0ns (shown below), draw the expected waveforms seen at *B*, *C*, and *D* from 0ns to 30ns.





- (b) Comment on the data transmission quality of the PCB traces. (I.e. is the data at the destinations accurate?)

4. (25pts) To drive all the clocks for our clocked circuits on a chip, we often build a clock tree. This way, we physically distribute the clock to all the circuits while trying to guarantee all paths are of equal length and equal delay. Consider the small clock tree as shown.

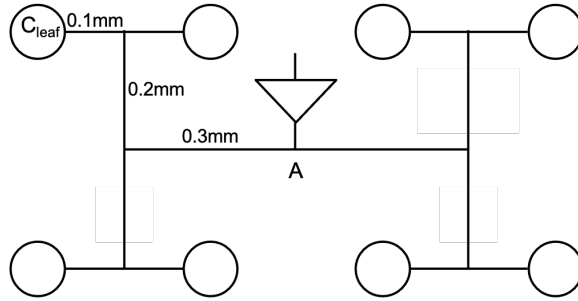


C_{leaf} is the total capacitance for some number of clocked circuits in a region of the chip (we might just keep branching the clock tree until it gets down to a single output; for this problem we're building a small tree and lumping a group of circuits together at the leaf to keep the problem size small).

- $R_{wire} = 60\text{K}\Omega/\text{mm}$
- $C_{wire} = 0.16\text{pF}/\text{mm}$
- $C_{leaf} = 5\text{fF}$
- $R_0 = 25\text{K}\Omega$
- $C_0 = 0.01\text{fF}$
- $\mu_n = 2\mu_p$
- Assume $C_{diff} = 0$ (to simplify problem)
- Use $R_0/50$ buffers (ideally, you would also determine buffer sizing and staging. We specify a fixed buffer size to simplify the problem.)

- (a) If driven by a single $R_0/50$ buffer at (A), what is the delay driving the leaf capacitance loads? (Use an Elmore delay calculation)

- (b) How would you buffer this tree to minimize delay? Describe buffer placement. Start from the single $R_0/50$ buffer root of tree (A).



- (c) What is the delay driving the leaf capacitance loads after buffering?

5. (15pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be **clear** in your explanation and **handwriting**.

A Given there are two parallel switching wires, what crosstalk could occur considering all the different switching cases? Comment on the worst case and best case scenarios.

B What is the difference between dynamic logic and static logic?

C How does the increasing the threshold voltage of a device impact delay and energy?

For the next two questions, two identical adder circuits are being used A and B. A is run at $\frac{1}{2}V_{dd}$ and B is run at V_{dd} . At $\frac{1}{2}V_{dd}$, the maximum frequency is $\frac{1}{5}$ the maximum frequency at V_{dd} . Both circuits are used for 10 ADD operations at the corresponding maximum frequency.

D How much less average dynamic power was consumed by A? Give a percentage.

E How much slower was A at completing the 10 operations than B? Give a percentage.