**University of Pennsylvania**
**Department of Electrical and System Engineering**
**Circuit-Level Modeling, Design, and Optimization for Digital Systems**

ESE370, Fall 2021 Final Friday, December 17

---

- Problem weightings shown.
- Calculators allowed.
- Closed book = No text or notes allowed.
- Additional workspace in exam book. Note where to find work in exam book if relevant.

**Name: Answers**

| | |
|---|---|
| Q1 | |
| Q2 | |
| Q3 | |
| Q4 | |
| Q5 | |
| Total | Mean: 67.8, Stdev: 12.7 |

Default technology:

- 22nm Low Standby Power Process (LSTP)
- $\gamma = 1$
- $V_{dd}$=1V
- nominal $V_{thn} = -V_{thp}$=300mV
- $C_0 = 2 \times 10^{-17}$F (for $W = 1$ device)
- $I_{d,sat_0} = 10\mu$A (for $W = 1$ device)
- $I_{sd,leak_0} = 0.3$ pA (for $W = 1$ device)
- velocity saturated operation
- $R_{wire} = 700\text{K}\Omega/\text{cm}$
- $C_{wire} = 1.7\text{pF}/\text{cm}$

Transmission line:

$$w = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\epsilon_r \mu_r}} \tag{1}$$

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2}$$

$$V_r = V_i \left( \frac{R - Z_0}{R + Z_0} \right) \tag{3}$$

$$V_t = V_i \left( \frac{2R}{R + Z_0} \right) \tag{4}$$

Timing constraints:

$$T \geq t_{clk \to q} + t_{plogic} + t_{setup} \tag{5}$$

$$t_{cdlatch} + t_{cdlogic} \geq t_{hold} \tag{6}$$

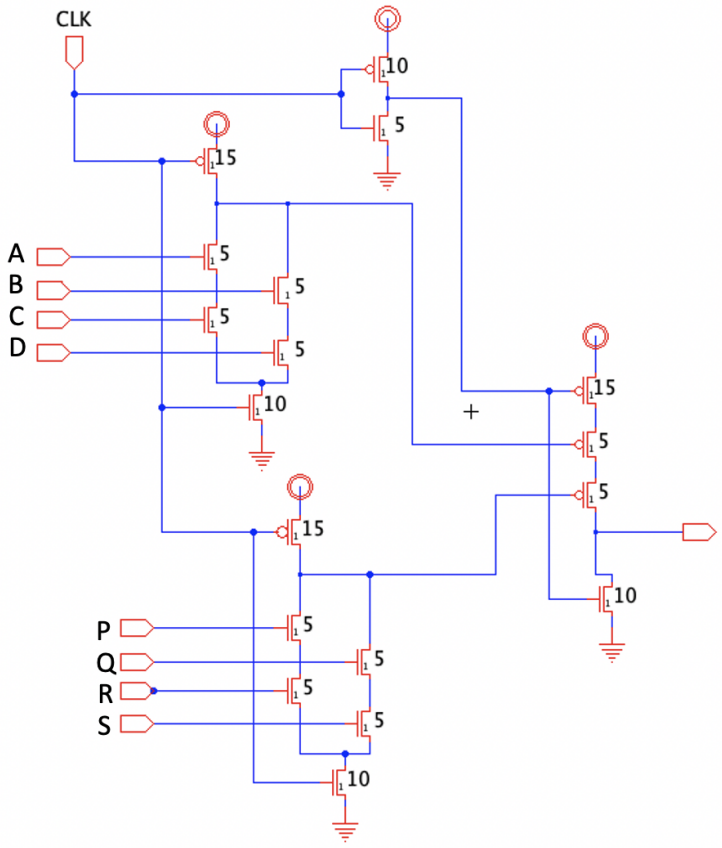
Optimal buffering:

$$L_{seg} = 2\sqrt{\frac{R_0(\gamma + 1)C_0}{R_{wire}C_{wire}}} \tag{7}$$

$$W_{buf} = \sqrt{\frac{R_0 C_{wire}}{2R_{wire}C_0}} \tag{8}$$

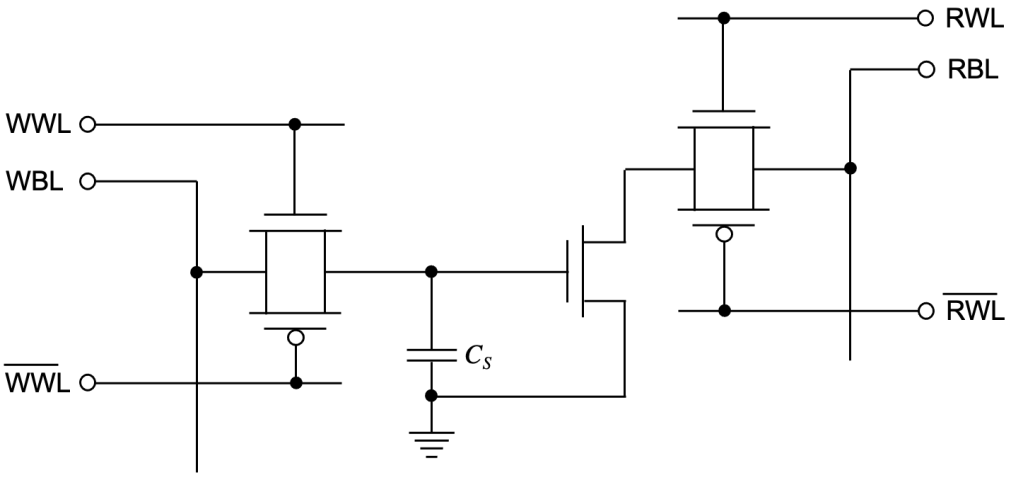
1. (15pts) Consider the following dynamic logic circuit. What logic function does it evaluate?

   Assume the circuit is loaded by $10C_0$ output. Assume $C_{diff} = 0.5C_{gate}$, $\mu_n = 2\mu_p$. Assume the CLK signal is driven strongly such that the rise time on the clock is $R_0C_0$. Use Elmore delay calculations where appropriate. For full credit (and partial credit consideration) show your delay components (stages, components of Elmore delay calculation).




| | |
|---|---|
| Out as a function of the inputs: A, B, C, D, P, Q, R, S? | $(A \cdot C + B \cdot D)(P \cdot R + Q \cdot S)$ |
| Evaluate Delay in units of $\tau$ (show delay components) | $\frac{\frac{15}{2}+3\times5+\frac{10}{2}+5}{10} + \frac{\frac{15}{2}+4\times\frac{5}{2}+5}{5} + \frac{\frac{15}{2}+5+5}{5}$ $+ \frac{\frac{15}{2}+2\times5+\frac{10}{2}+10}{\frac{15}{2}} + \frac{5+\frac{5}{2}+10+\frac{10}{2}}{\frac{5}{2}} + \frac{\frac{5}{2}+\frac{10}{2}+10}{\frac{5}{2}}$ $= 31.583\tau$ |
| Precharge Time | $\max\left(\frac{\frac{15}{2}+5\times3+\frac{10}{2}+5}{\frac{15}{2}} + \frac{2\times5+\frac{10}{2}}{5} + \frac{5+\frac{10}{2}}{5}, \frac{25+\frac{15}{2}}{5} + \frac{\frac{15}{2}+2\times5+\frac{10}{2}+10}{10} + \frac{3\times\frac{5}{2}+\frac{15}{2}}{\frac{5}{2}} + \frac{\frac{5}{2}+\frac{15}{2}}{\frac{5}{2}}\right)\tau$ $= 19.75\tau$ |

2. (25pts) Assume we have a 5-transistor bitcell as shown below. It is used to design a memory with 32 words of 16 bits each. The storage capacitor $C_S$ is not an explicit capacitor and is equal to the parasitic capacitance at that node from the cell transistors (you can ignore any wiring parasitics). Assume all bitlines are driven with minimum size buffers during a write, and pre-charged to $V_{dd}$ during a read. All driving/pre-charging is fully complete before any wordlines are raised. $V_{dd} = 1V$ and $\gamma = 0.5$. All transistors in bitcell are minimum sized and $\mu_n = \mu_p$.



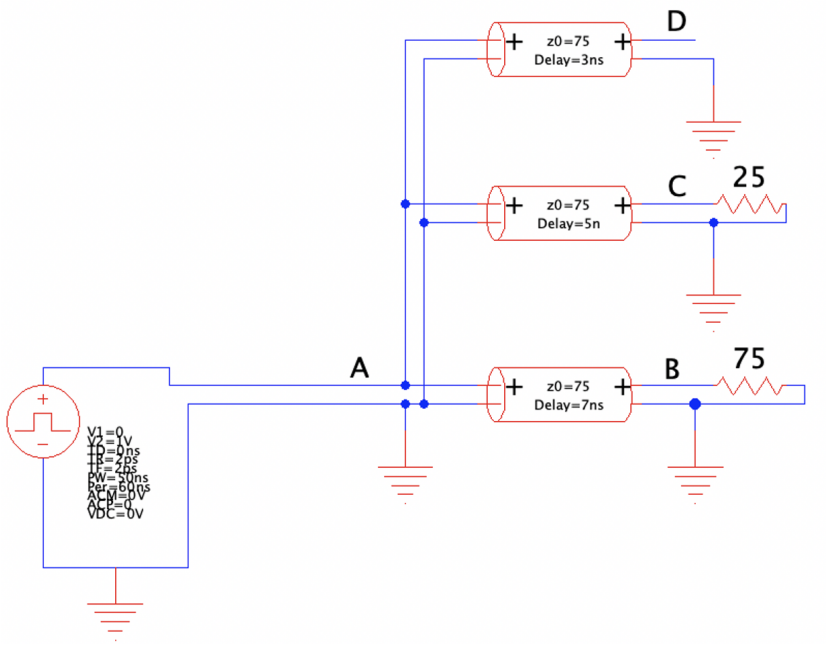

(a) Is this a SRAM or DRAM cell? Explain your reasoning?
DRAM. The data is stored on a capacitive node and is not actively driven

(b) What is the worst case delay after the wordline is raised to write into the cell in units of $\tau$?
WBL capacitance already charge before WL raises. Delay is through buffer and transmission gate drive charging $C_S$.
$\left(R_0 + \frac{R_0}{2}\right) \times (2\gamma + 1)C_0 = 3\tau$

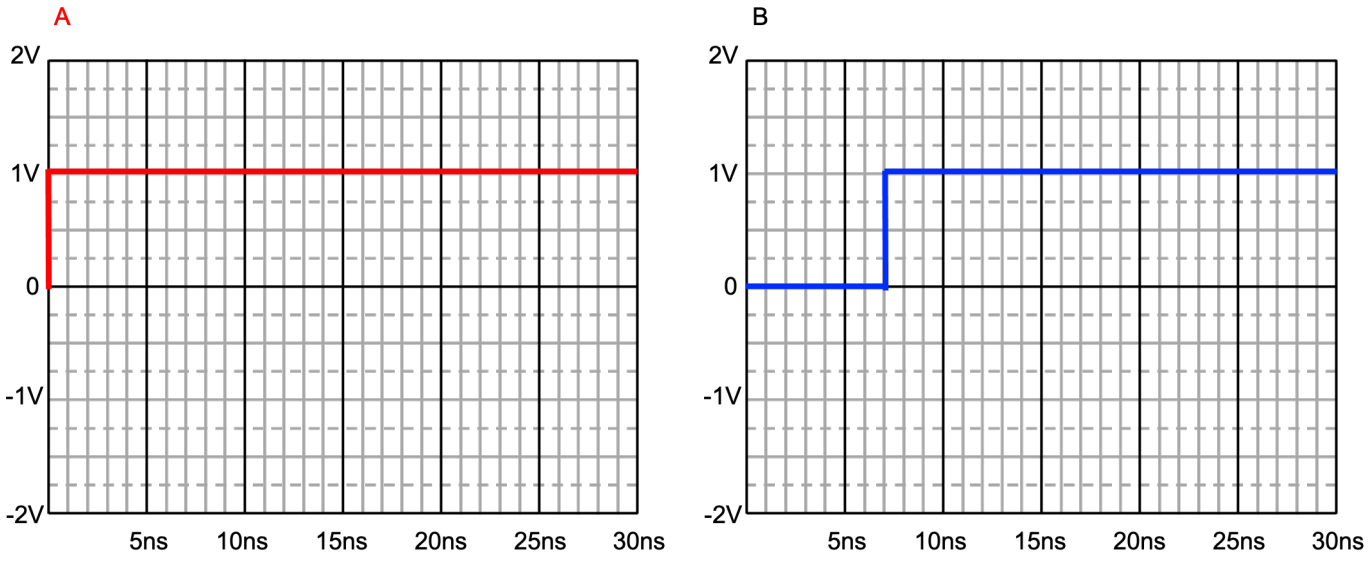
(c) What voltage does RBL evaluate to when reading a 0? What is the delay after the wordline is raised in units of $\tau$ when reading a 0? (You can assume any column driver capacitance is negligible)
This DRAM cell has inverted reads, so RBL is $V_{dd}$ when reading a 0. The delay is $0\tau$ because RBL is precharged and holds its value.

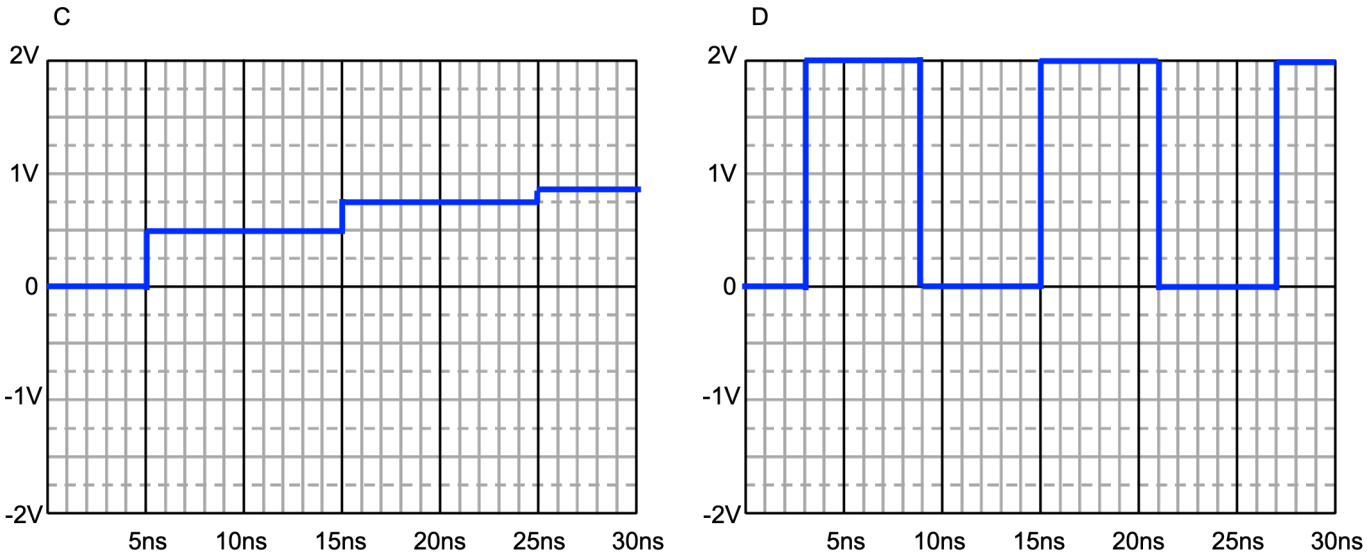
(d) What voltage does RBL evaluate to when reading a 1? What is the delay after the wordline is raised in units of $\tau$ when reading a 1? (You can assume any column driver capacitance is negligible)
This DRAM cell has inverted reads, so RBL is 0 when reading a 1. The delay is discharging RBL through transmission gate and nMOS device. Drain of nMOS already discharged before WL raised.
$\left(R_0 + \frac{R_0}{2}\right) \times 32 \cdot 2\gamma C_0 = 48\tau$

3. Transmission Line Termination (20pts). A single IC driving 3 ICs connected with PCB traces on a PCB is modeled as 3 transmission lines with matched termination. However, after manufacturing the termination of the three lines have varied and are given in the model below. The schematic shows a source end, $A$, and three destinations, $B$, $C$, and $D$. The intent of the design is for the waveforms on $B$, $C$ and $D$ to be identical in shape to the source waveform with some propagation delay. Reminder: The ideal voltage source looks like a short circuit.




(a) Given the source waveform is a 1V step at 0ns (shown below), draw the expected waveforms seen at $B$, $C$, and $D$ from 0ns to 30ns.

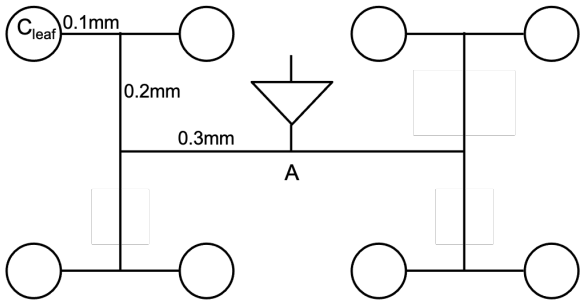





(b) Comment on the data transmission quality of the PCB traces. (I.e is the data at the destinations accurate?)

B and C settle to the correct data with some delay, but D oscillates between 2V and 0V and is corrupted data.

4. (25pts) To drive all the clocks for our clocked circuits on a chip, we often build a clock tree. This way, we physically distribute the clock to all the circuits while trying to guarantee all paths are of equal length and equal delay. Consider the small clock tree as shown.

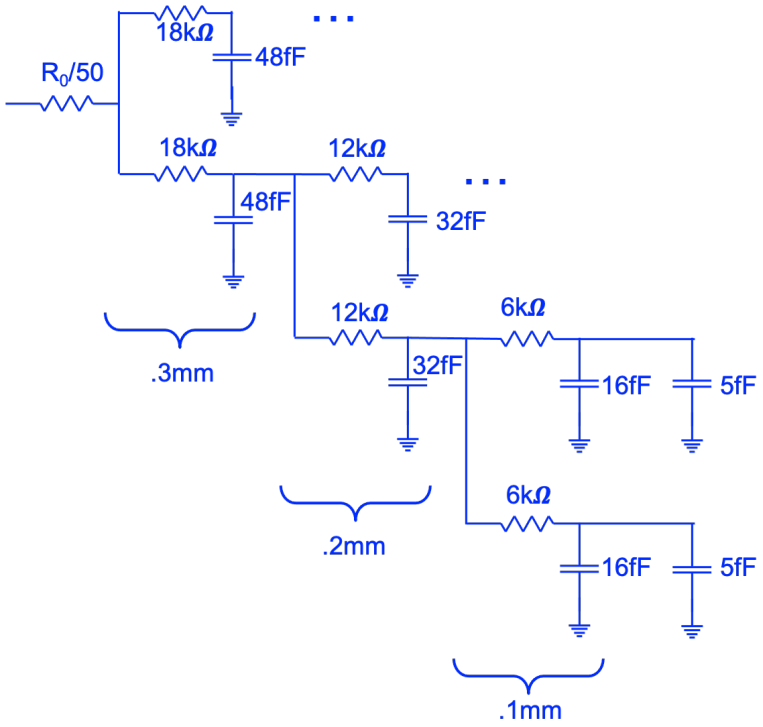



$C_{leaf}$ is the total capacitance for some number of clocked circuits in a region of the chip (we might just keep branching the clock tree until it gets down to a single output; for this problem we're building a small tree and lumping a group of circuits together at the leaf to keep the problem size small).

- $R_{wire}$ =60KΩ/mm
- $C_{wire}$ =0.16pF/mm
- $C_{leaf}$ =5fF
- $R_0$ =25KΩ
- $C_0$=0.01fF
- $\mu_n = 2\mu_p$
- Assume $C_{diff} = 0$ (to simplify problem)
- Use $R_0/50$ buffers (ideally, you would also determine buffer sizing and staging. We specify a fixed buffer size to simplify the problem.)

(a) If driven by a single $R_0/50$ buffer at (A), what is the delay driving the leaf capacitance loads? (Use an Elmore delay calculation)

The equivalent RC circuit is as follows:



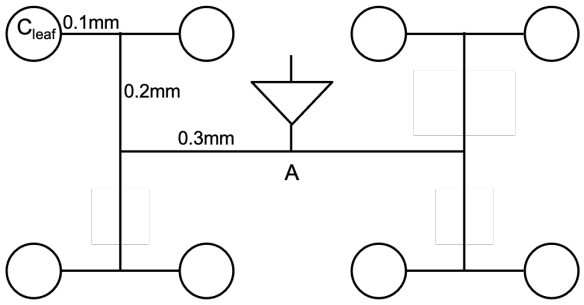

Using straight Elmore delay with lumped wire model, we can get the delay to any leaf node:

$$\tau = 500\Omega(48fF \times 2 + 32fF \times 4 + (16fF + 5fF) \times 8) + 18k\Omega(48fF + 32fF \times 2 + (16fF + 5fF) \times 4) + 12k\Omega(32fF + (16fF + 5fF) \times 2) + 6k\Omega(16fF + 5fF) = 4.738ns$$

If you accounted for the distributed wire delay versus lumped:

$$\begin{aligned}\tau = 500\Omega(48fF \times 2 + 32fF \times 4 + (16fF + 5fF) \times 8) \\ +\frac{1}{2}18k\Omega(48fF) + 18k\Omega(32fF \times 2 + (16fF + 5fF) \times 4) \\ +\frac{1}{2}12k\Omega(32fF) + 12k\Omega((16fF + 5fF) \times 2) \\ +\frac{1}{2}6k\Omega(16fF) + 6k\Omega(5fF) \\ = 4.064ns\end{aligned}$$

(b) How would you buffer this tree to minimize delay? Describe buffer placement. Start from the single $R_0/50$ buffer root of tree (A).




Optimal segment length from data sheet on front of exam:

$$2\sqrt{\frac{25k\Omega \cdot 0.01fF}{60k\Omega \cdot 0.16pF}} = .01mm \tag{9}$$

Place buffers every 0.01mm along all wires from the buffer to each leaf node. Each 0.3mm wire will have 30 buffers; each 0.2mm wire will have 20 buffers; and, each 0.1mm wire will have 10 buffers.

(c) What is the delay driving the leaf capacitance loads after buffering? 142.8ps

Delay is dominated by the buffered wire delay. For 0.01mm wire segment, we have $R_{wire} = 600\Omega$ and $C_{wire} = 1.6fF$. Each segment with $R_0/50$ buffers will have new delay of:

$$\frac{25k\Omega}{50}(1.6fF + 2 \cdot 50 \cdot 0.01fF) + \frac{1}{2}(1.6fF) * 600\Omega + 600\Omega(2 \cdot 50 \cdot 0.01fF) = 2.38ps$$

We have 60 total segments from A to each leaf node resulting in a delay of $60 * 2.38ps = 142.8ps$. This ignores any branch buffer loading and driving the $C_{leaf}$ nodes which is negligible compared to the wire delay ($< 5ps$).

5. (15pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be **clear** in your explanation and **handwriting**.

**A** Given there are two parallel switching wires, what crosstalk could occur considering all the different switching cases? Comment on the worst case and best case scenarios.

Switching on the lines can be in opposite directions, same directions or only one switching at a time. If the lines switch in opposite directions, the crosstalk is the worst case and it appears as if the coupling capacitance is twice as large. If the lines switch in the same direction, the crosstalk is the best case and it is effectively as if there is no coupling capacitance.

**B** What is the difference between dynamic logic and static logic?

Static logic has the output always actively driven and is connected via an impedance path to a supply rail. Dynamic logic stores output values on capacitive nodes and has precharge and evaluate phases.

**C** How does the increasing the threshold voltage of a device impact delay and energy?

Increasing the threshold voltage decreases all current levels, so delay increase and energy decreases.

For the next two questions, two identical adder circuits are being used A and B. A is run at $\frac{1}{2}V_{dd}$ and B is run at $V_{dd}$. At $\frac{1}{2}V_{dd}$, the maximum frequency is $\frac{1}{5}$ the maximum frequency at $V_{dd}$. Both circuits are used for 10 ADD operations at the corresponding maximum frequency.

**D** How much less average dynamic power was consumed by A? Give a percentage.

$V_A = \frac{1}{2}V_{dd}$, $V_B = V_{dd}$, $f_A = \frac{1}{5}f_B$:

$\frac{P_A}{P_B} = \frac{\frac{1}{2}CV_A^2 f_A}{\frac{1}{2}CV_B^2 f_B} = \frac{\left(\frac{1}{2}\right)^2 \times \frac{1}{5}}{1} = 5\%$

This means Adder A uses 95% less power.

**E** How much slower was A at completing the 10 operations than B? Give a percentage.

The clock period of adder A is 5 times larger than that of B, so it is 5 times slower, or 500% slower.