

University of Pennsylvania  
 Department of Electrical and System Engineering  
 Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021

HW4: Delay, MOS Transistor

Friday, October 1

**Due:** Friday, October 8, 11:59PM

Unless otherwise noted, assume:

- 22nm PTM Spice models that you used on HW2: /home1/e/ese370/ptm/22nm\_HP.pm
- $V_{dd} = 0.8V$ ,  $V_{thn} = 300mV$ ,  $V_{thp} = -300mV$ ,  $C_{OX} = 35 \frac{fF}{\mu m^2}$ ,  $L_{drawn} = 22nm$ ,  $L_{eff} = 17nm$ ,  $W = 44nm$ ,  $n = 1.5$ ,  $\nu_{SAT} = 10^5 \frac{m}{s}$ ,  $\lambda = 0$ ,  $\mu_n = 540 \frac{cm^2}{V \cdot s}$ ,  $\mu_p = 200 \frac{cm^2}{V \cdot s}$ ,  $T=27C$  (300K)
- For analytic device modeling, use the follow NMOS IV Model Equations

– Resistive:

$$I_D = \mu_n C_{OX} \left( \frac{W}{L} \right) \left( (V_{GS} - V_{th}) V_{DS} - \frac{(V_{DS})^2}{2} \right) \quad (1)$$

– Saturated (Pinch Off):

$$I_D = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_{th})^2 \quad (2)$$

– Velocity Saturated:

$$I_D = \nu_{sat} C_{OX} W \left( V_{GS} - V_{th} - \frac{V_{DSAT}}{2} \right) \quad (3)$$

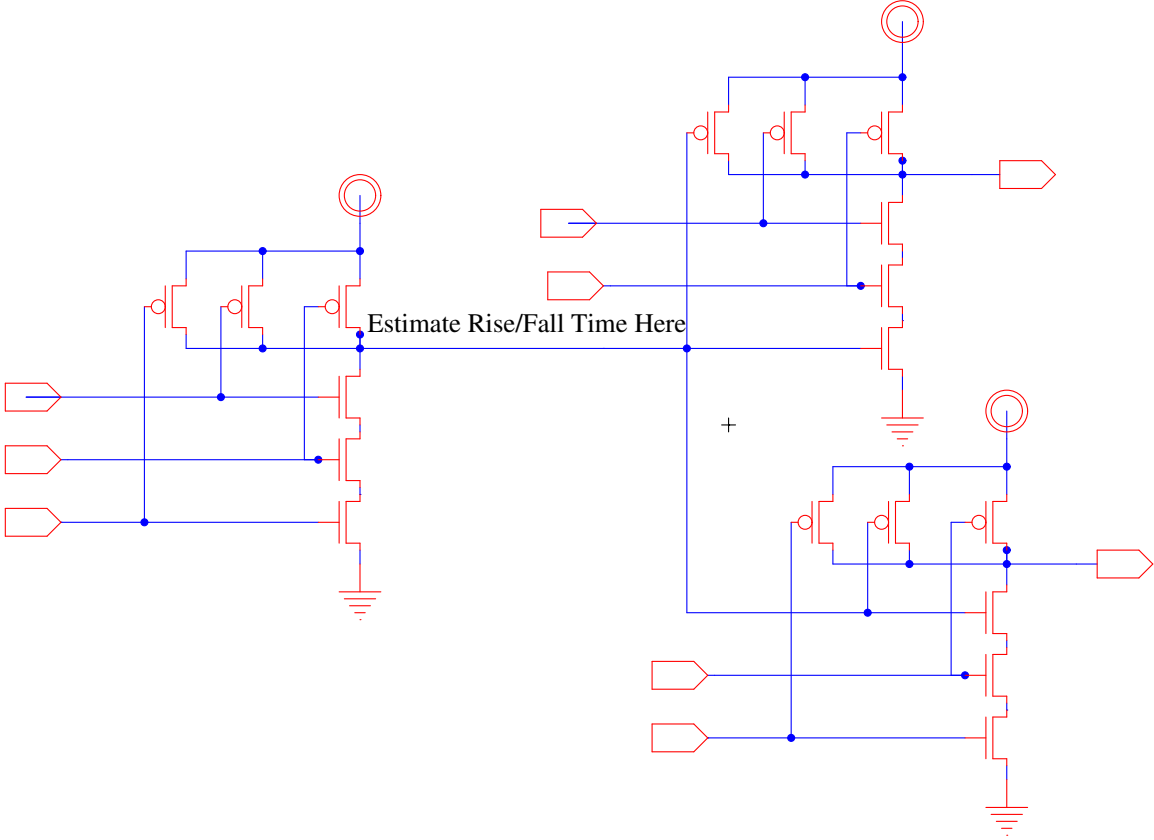
– Subthreshold:

$$I_D = I_S \left( \frac{W}{L} \right) e^{\frac{V_{GS} - V_{th}}{nkT/q}} \quad (4)$$

with  $I_S = 1\mu A$ 

NOTE: The parameters are rough approximations and will not match SPICE perfectly.

- 1. Using a first-order model and assuming (a) each transistors has an on resistance  $R_{on}$  and (b) each gate has a gate capacitance  $C_{gate}$ , what is the worst-case rise and fall time of the signal marked?



For a CMOS circuit, we generally want  $I_{on}/I_{off}$  large in order to: (a) achieve output voltages close to the rail, (b) switch quickly, and (c) leak little. Questions 2-5 provide some setup then culminates in a small design problem to select voltage to achieve a target, large  $I_{on}/I_{off}$  even in the face of variation.

2. Consider an inverter with  $V_{in} = V_{dd}$  after the output has settled to steady state. Using equations:
  - (a) Identify the region of operation for the two transistors.
  - (b) Identify the current through the transistors.
  - (c) Identify  $V_{ol}$ . (We specifically want to know how far it is from 0; so, do not approximate it as zero as we would typically, but try to identify the small, non-zero value.)
  
3. At room temperature what is  $I_{on}/I_{off} = I_{ds}(V_{gs} = V_h) / I_{ds}(V_{gs} = V_l)$  for an NMOS transistor used in an inverter with  $W_p = W_n$ ; assume  $V_{ds} = V_{dd}$  for the NMOS in both the ideal case (a) and worst case (b), so this is just after the input switches from  $V_{gs} = V_l$  to  $V_{gs} = V_h$ .
  - (a) Ideal:  $V_h = V_{dd}$ ,  $V_l = 0V$
  - (b) With 100mV noise margins:  $V_h = V_{dd}-100mV$ ,  $V_l = 100mV$
  
4. What is the impact of increasing  $V_{th}$  on the following: (we want a description with words and equations.)
  - (a) Speed of charging?
  - (b)  $I_{on}/I_{off}$  with 100mV noise margins (case b above).
  
5. Consider the simple CMOS inverter operated at  $V_{dd}=500mV$ .
  - (a) What makes this case different from the  $V_{dd}=0.8V$  case?
  - (b) Identify  $V_{oh}$ ,  $V_{ih}$ ,  $V_{il}$ ,  $V_{ol}$ , and the high and low noise margins that provide proper restoration. Hint: Think about the extreme ends of the VTC.
  - (c) What does this tell you about your freedom to select  $V_{dd}$  and still achieve proper operation?
  
6. Design problem: Use equations to select  $V_{dd}$ ,  $V_{th}$  to achieve  $I_{on}/I_{off} > 10^6$  for an NMOS transistor as used in an inverter. Try to keep  $V_{dd}$  as small as possible. Assume 100mV noise margin, so  $V_{ih} \approx V_{dd} - 100mV$ ,  $V_{il}=100mV$ . This minimum  $I_{on}/I_{off}$  ratio should hold across the temperature range 0C to 100C. It might be helpful to set up an excel sheet to make the design problem easier.