University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021 HW7: Noise and Transmission Lines Friday, December 3

Due: Friday, December 10, 11:59PM

1. "Inductive Noise and Crosstalk" Lab 2 summary and post-lab questions:
   (a) Summarize raw data collected
   (b) Working individually, describe your observations (each answer should be 2–3 sentences; most answers must be qualitative, but one or two of these might benefit from an equation connected to the material covered in the lectures following the lab).
      i. Impact of bypass capacitors?
      ii. Impact of crosstalk on driven vs. undriven signals?
      iii. Impact of adjacent wire length on signal crosstalk?

      The observations and insight should come out of your team data collection and discussion. Nonetheless, this writeup should be done independently and expressed in your individual words.
2. "Transmission Line" Lab 3 summary and post-lab calculations:
   (a) Provide a summary of your answers to in-lab questions. In other words, make sure your lab handout is completed.
   (b) Working individually, answer the following questions:
      i. Using the result from in-lab-2(b), what is the propagation speed of signals along the 5.34m trace?
      ii. What does in-lab-3(a) tell you about the impedance of the stripline trace?
      iii. Use reflection equations and transmission line behavior to explain your observations for in-lab-6(a).
3. Lab attendance.

4. Consider an SRAM with 2K (2048) words of 32 bits each.

   (a) How many address bits are needed to address these words?

   (b) Assuming that the central memory array is designed to have the same number of rows as it has columns, how many rows are there?

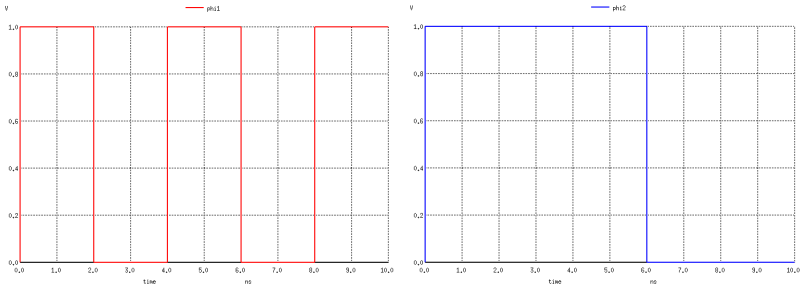
   (c) How many words are stored in each row?

   (d) How many of the address bits are used by the row decoder?

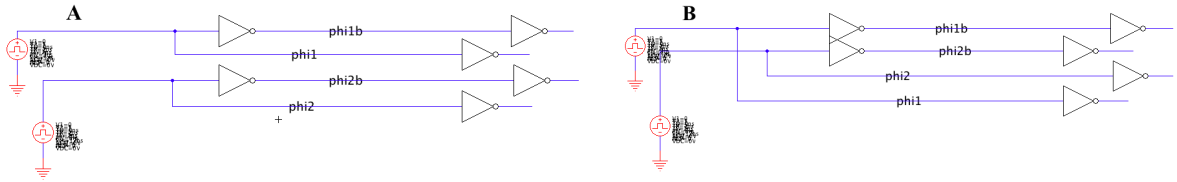
   (e) How many are used by the column decoder?

   (f) Assuming a min-sized 5T SRAM cell is used in your design, estimate the capacitance of the word line in terms of C_0 and the capacitance of the bit line in terms of C_{diff0}.

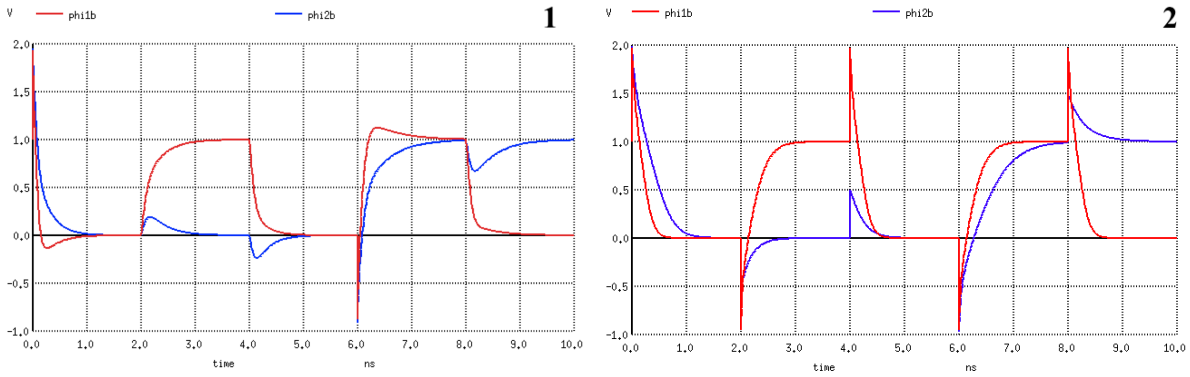
5. Two clocks are used on chip, **phi1** and **phi2** and are shown below where **phi1** is 3 times the frequency of **phi2**.



They are inputs into two inverters and the clocks and inverted clocks run adjacent to each other for a long distance on a chip. Two different configurations are designed with identical inverters and labeled below with A and B.



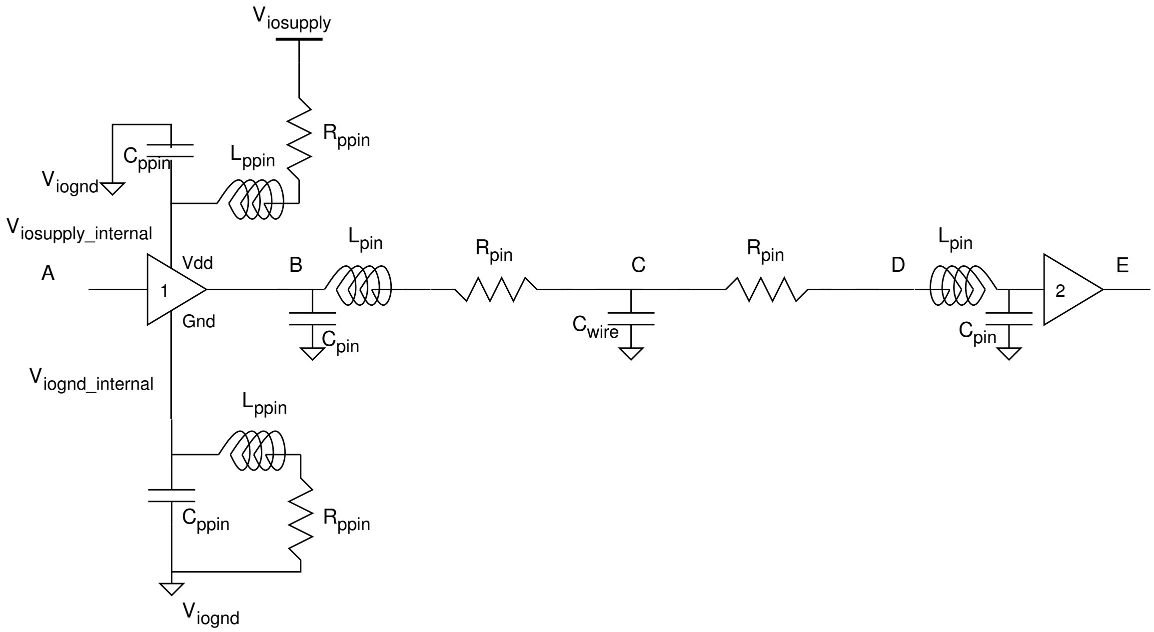
The waveforms from the configuration have different delays and are labeled below with 1 and 2.



(a) Identify which configuration (A and B) and waveforms (1 and 2) match. Explain your reasoning.

(b) Identify which configuration has the smaller delay and what about the configuration results in the smaller delay.

6. Simulate Off Chip I/O Signalling: Consider the following I/O pin and board model signalling between two chips.



L_{pin}	C_{pin}	R_{pin}	C_{wire}
2nH	1pF	0.3Ω	3pF

To roughly model the fact that you will have N output drivers per power/ground pair (*e.g.* in the 74X04 example used in Lab 2, you had $N = 6$ outputs sharing a single I/O pair):

- $L_{ppin} = N \times L_{pin}$, $R_{ppin} = N \times R_{pin}$, $C_{ppin} = \frac{C_{pin}}{N}$

The current per pin is actually larger ($I_{shared} = N \times I_{single}$). But you want to just simulate one pin, so this pushes that factor into the power/ground pin L, R, C parameters to model the effect.

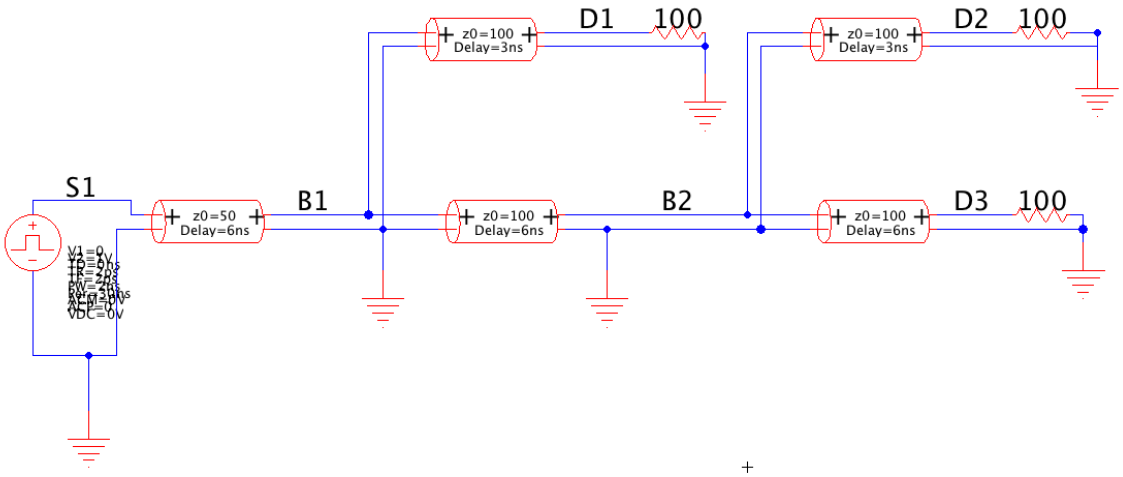
(a) Using SPICE and the 22nm PTM model, size inverter 1 to minimize the delay from A to a settled value at D for $N = 6$.

- Only consider D settled when it stays within 1/4 V_{dd} of its final value (*i.e.* below 1/4 V_{dd} or above 3/4 V_{dd}.

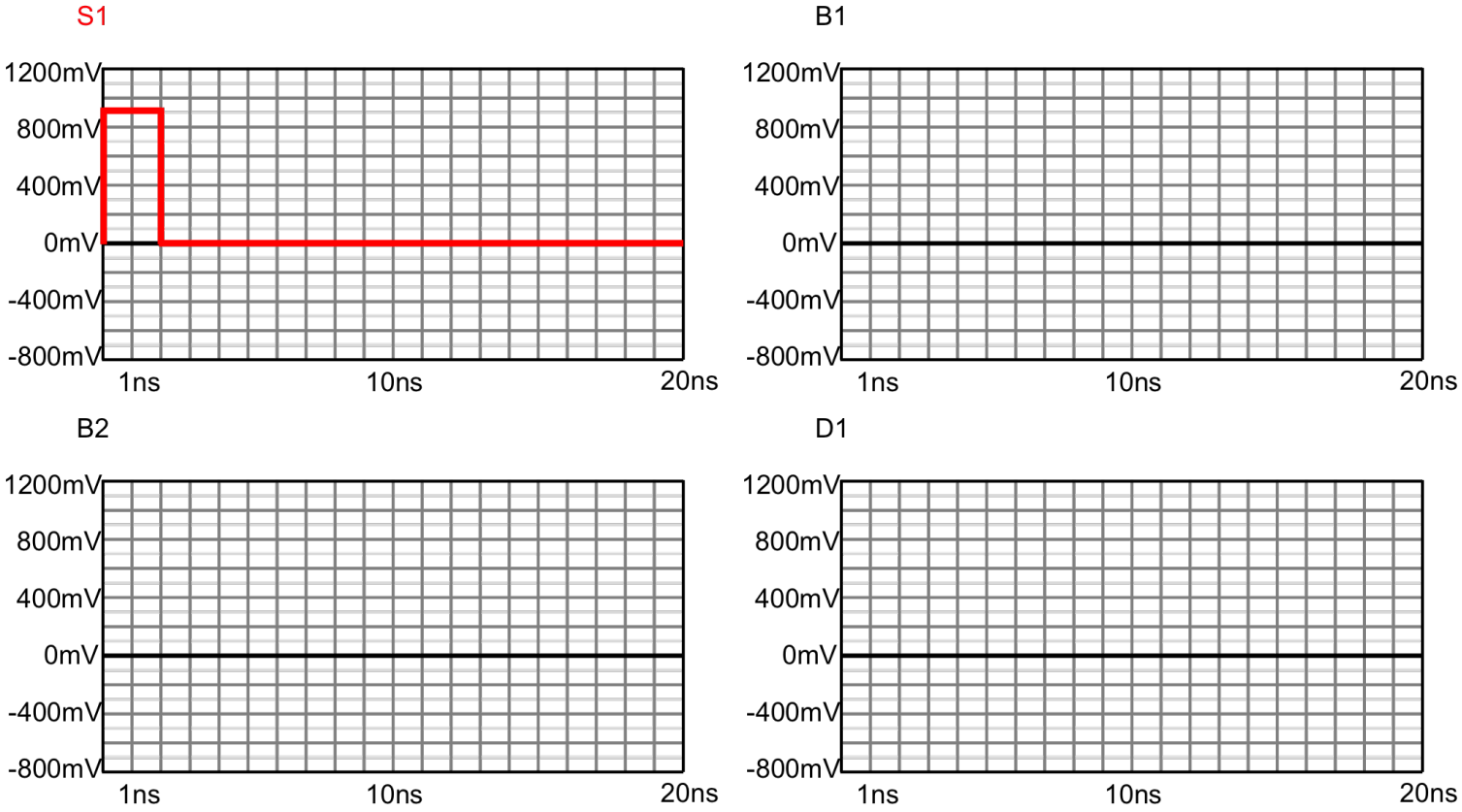
(b) Can you make the inverter too large? why?

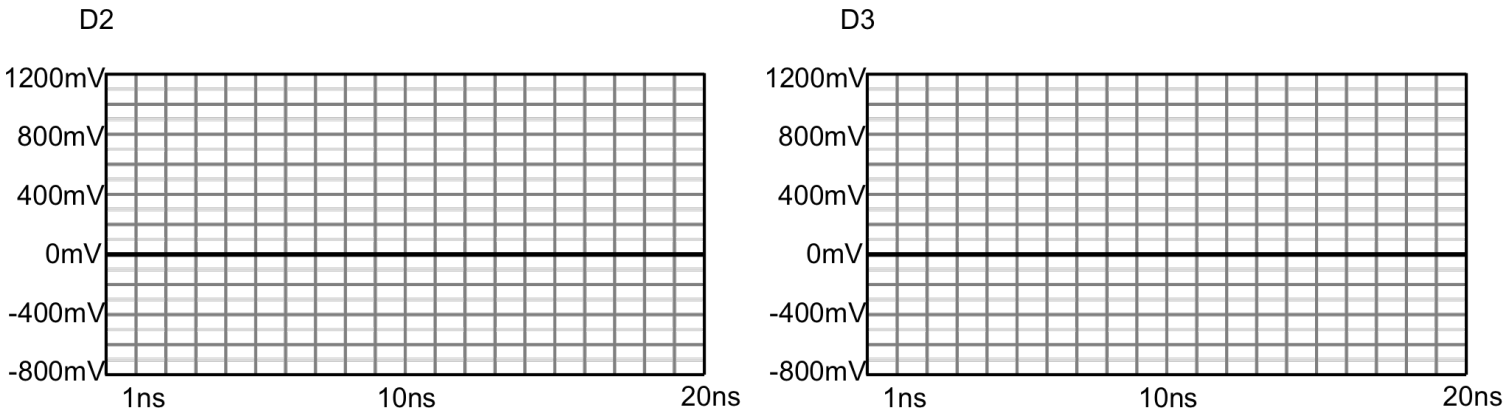
(c) Can you make the inverter too small? why?

7. Transmission Line Termination. A long data bus is designed and is modeled as a transmission line with transmission lines branched off it as shown below. The schematic shows a source end, $S1$, two branches, $B1$ and $B2$, and three destinations, $D1$, $D2$, and $D3$. The intent of the design is for the waveforms on $D1$, $D2$ and $D3$ to be identical in shape to the source waveform with some propagation delay, but the design fails to do that.



(a) Given the source waveform is a 900mV 2ns pulse at 0ns (shown below), draw the waveforms seen at $B1$, $B2$, $D1$, $D2$, and $D3$ from 0ns to 20ns.





(b) Fix the design so that $D1$, $D2$ and $D3$ are identical to the source waveform with the same propagation delay as the design model in part (a). Draw the new design model and clearly label the parameters ($z0$ and Delay) of each transmission line segment as well as any resistors.