# ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 11: September 29, 2021

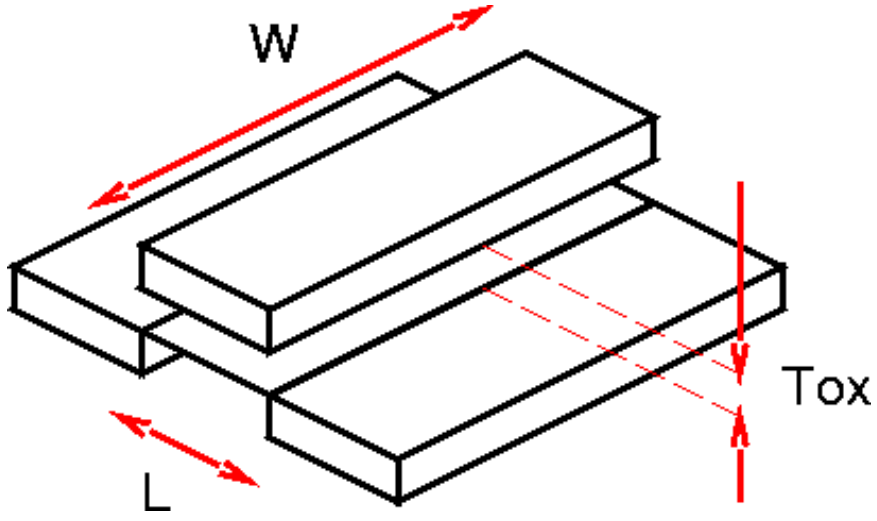
Layout and Area

# Today

- Layout
  - Transistors
  - Gates
- Design rules
- Standard cells

# Transistor

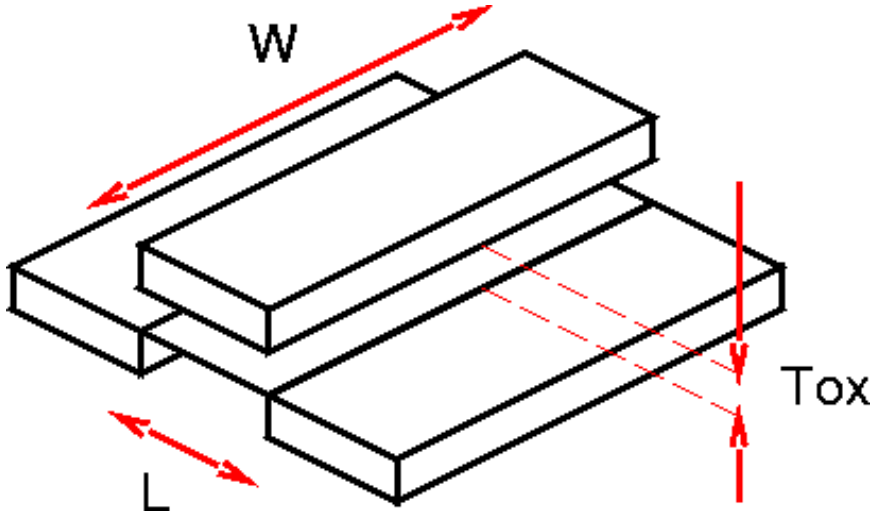

Side view



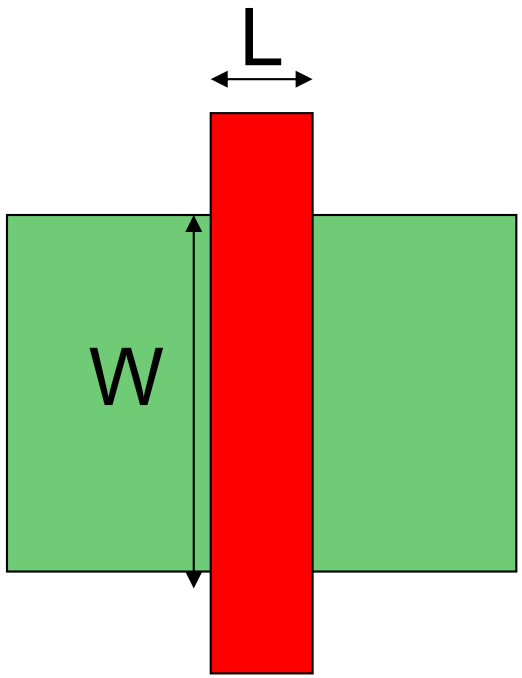

Perspective view

# Layout

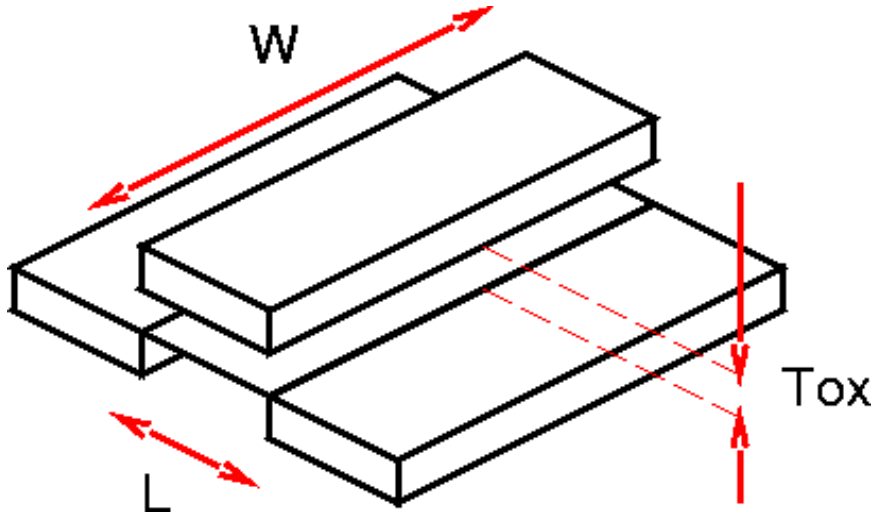
- Sizing & positioning of transistors
- Designer controls W, L
- $t_{ox}$ fixed for process
  - Sometimes thick/thin oxide "flavors"



# NMOS Geometry



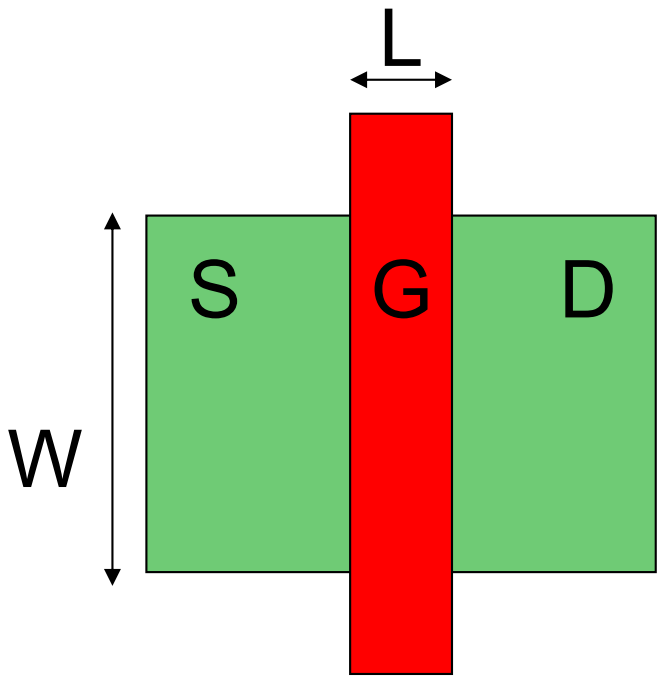

Top view




Perspective view

# NMOS Geometry

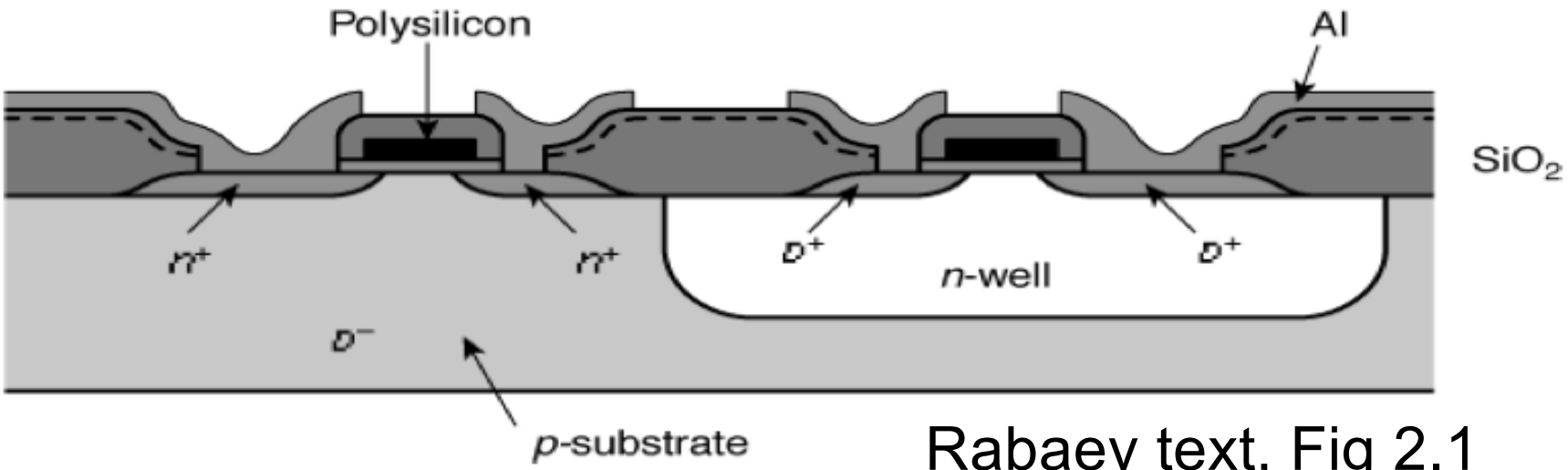
- Color scheme
  - Red: gate (polysilicon material)
  - Green: source and drain areas (n type diffusion)




Top view

# NMOS vs PMOS

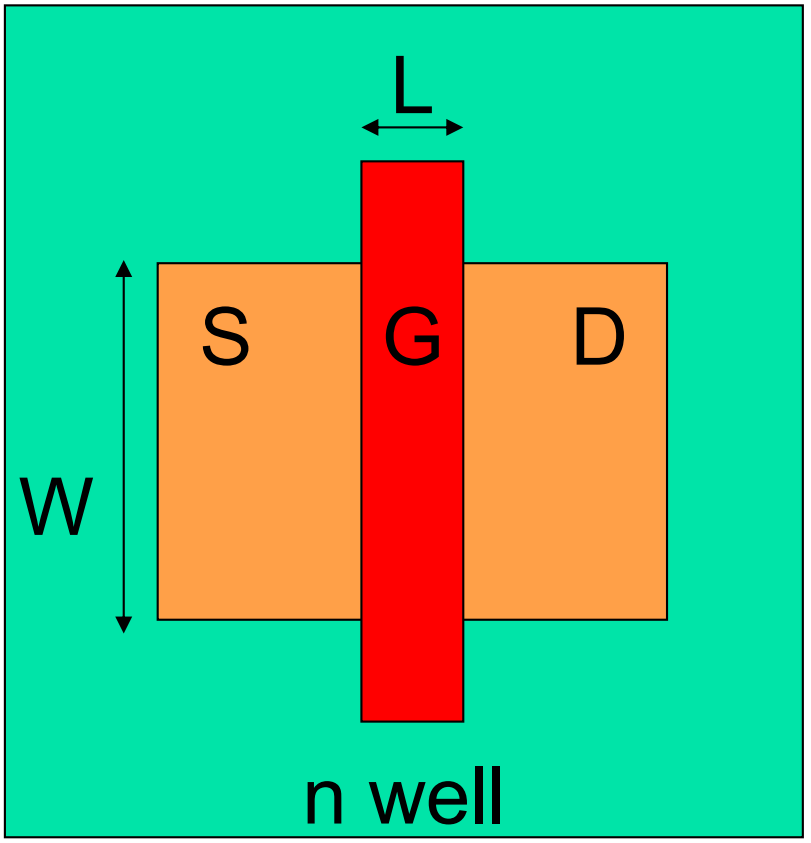
- NMOS built on p substrate
- PMOS built on n substrate
  - Needs an N-well




Rabaey text, Fig 2.1

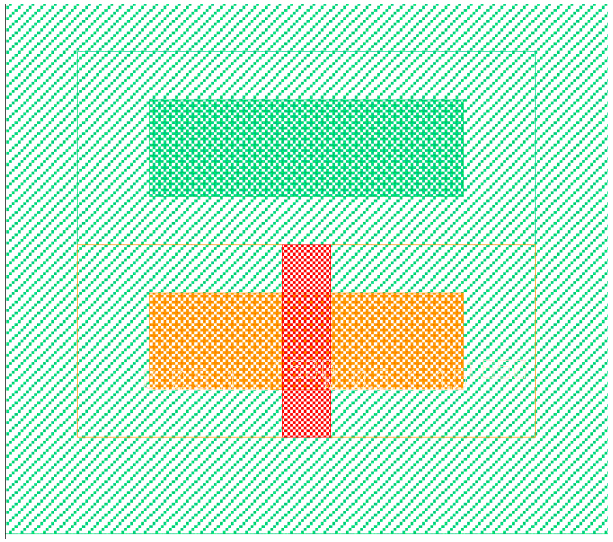
# PMOS Geometry

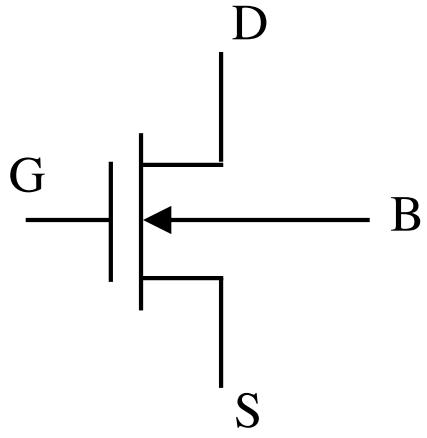
- Color scheme
  - Red: gate
  - Orange: source and drain areas (p type)
  - Green: n well
- NMOS built on p wafer
  - Must add n well material to build PMOS

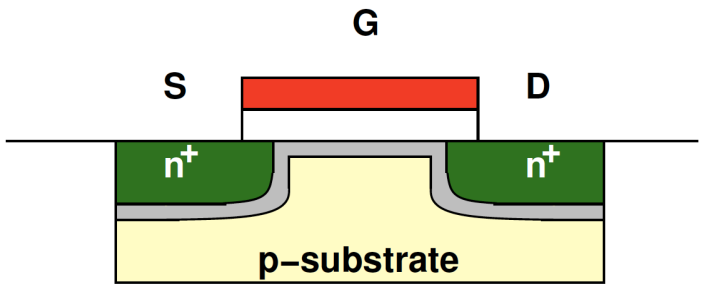


# Body Contact

- "Fourth terminal"
- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = GND$
- At right: PMOS (orange) with bulk contact (dark green)

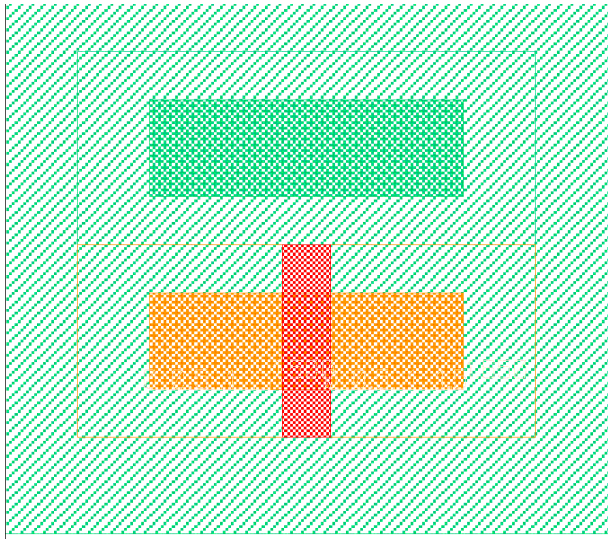


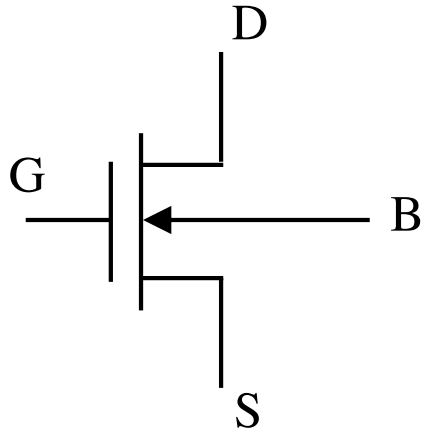


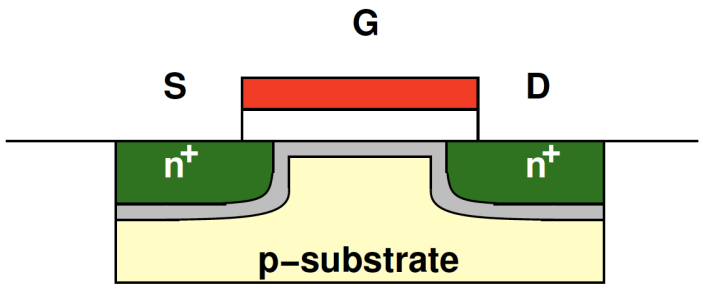



# Body Contact

- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = GND$
- What happens if NMOS body contact is $V_{dd}$?

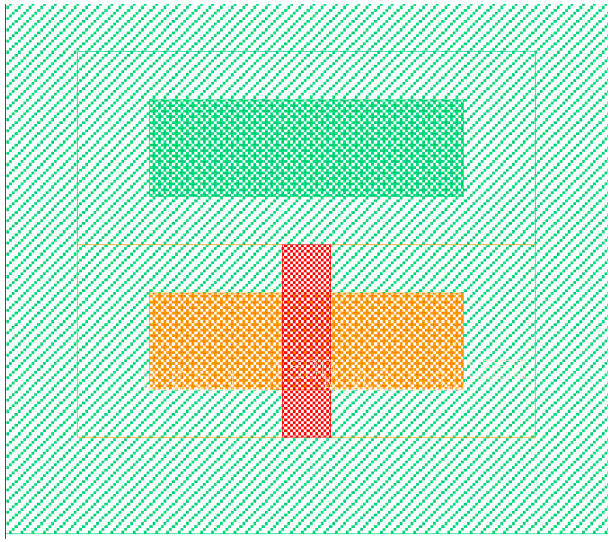


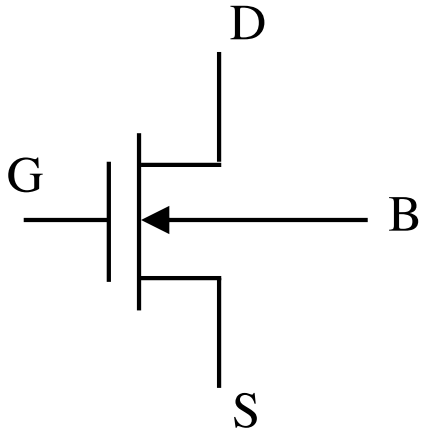


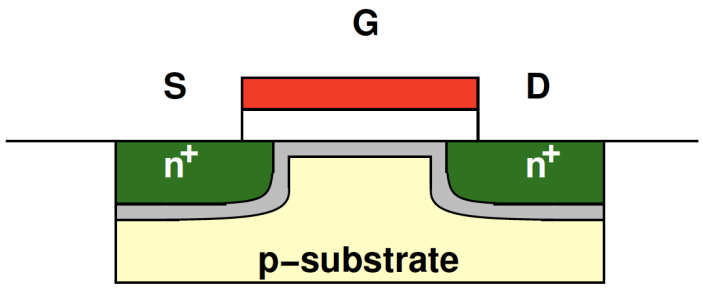



# Body Contact

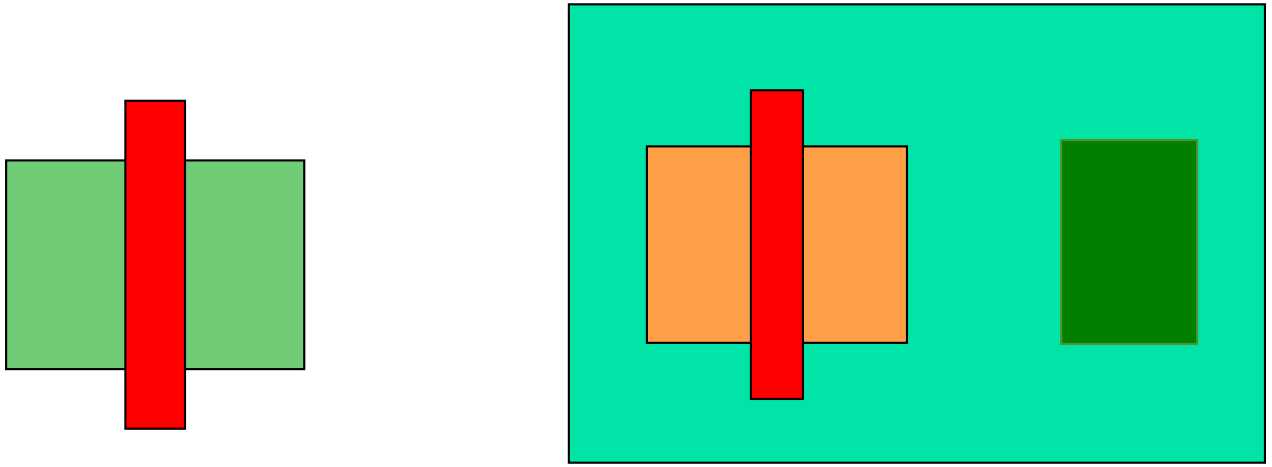
- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = GND$
- What happens if NMOS body contact is $V_{dd}$?
  - Polarity of field wrong
  - Won't invert channel

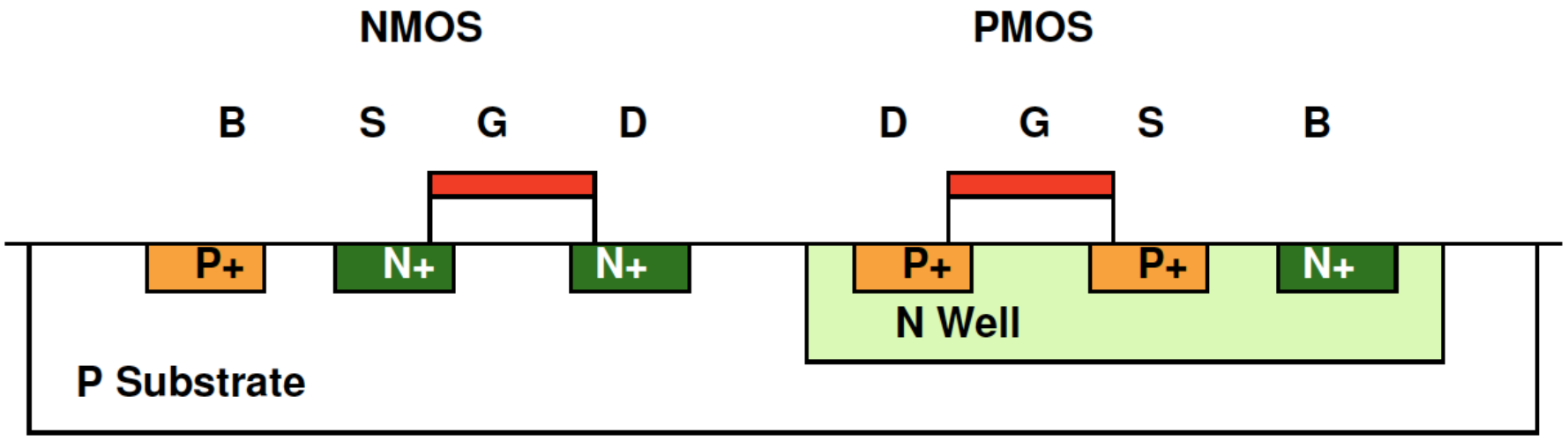




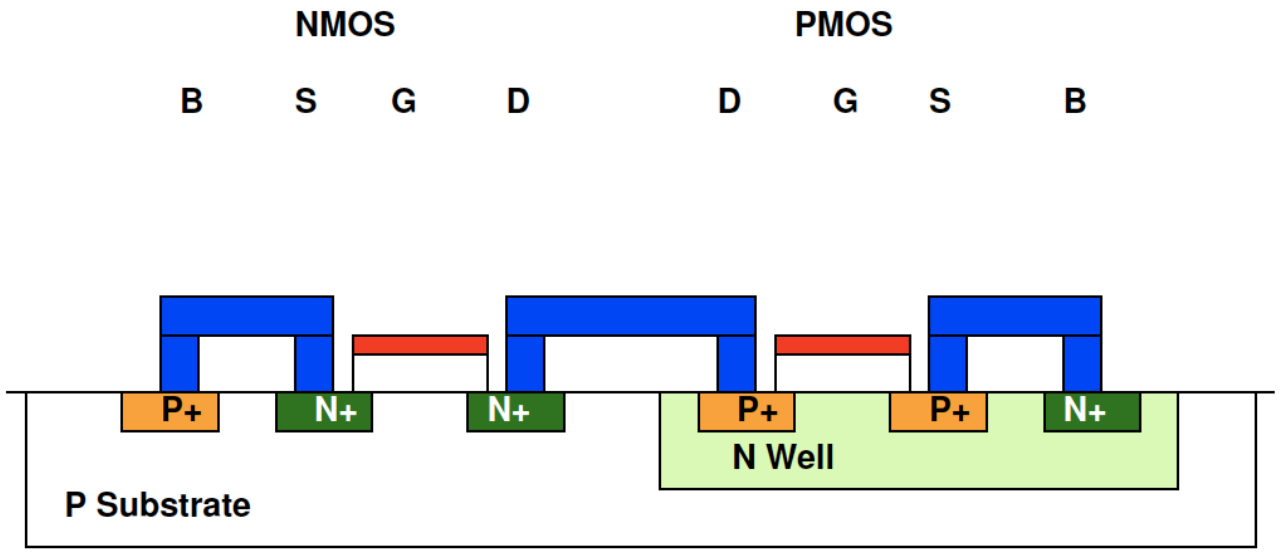
# Transistor Geometry





# Interconnect

- Connect transistors
  - Different layers of metal
    - "Contact" - metal to transistor
    - "Via" - metal to metal



# Interconnect

- Connect transistors
  - Different layers of metal
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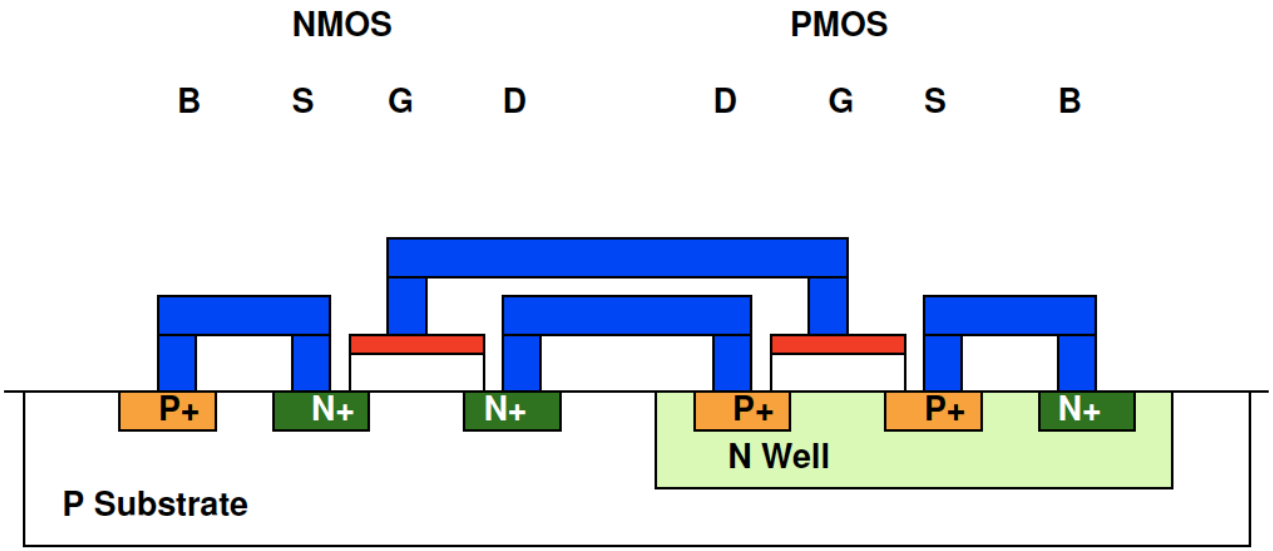
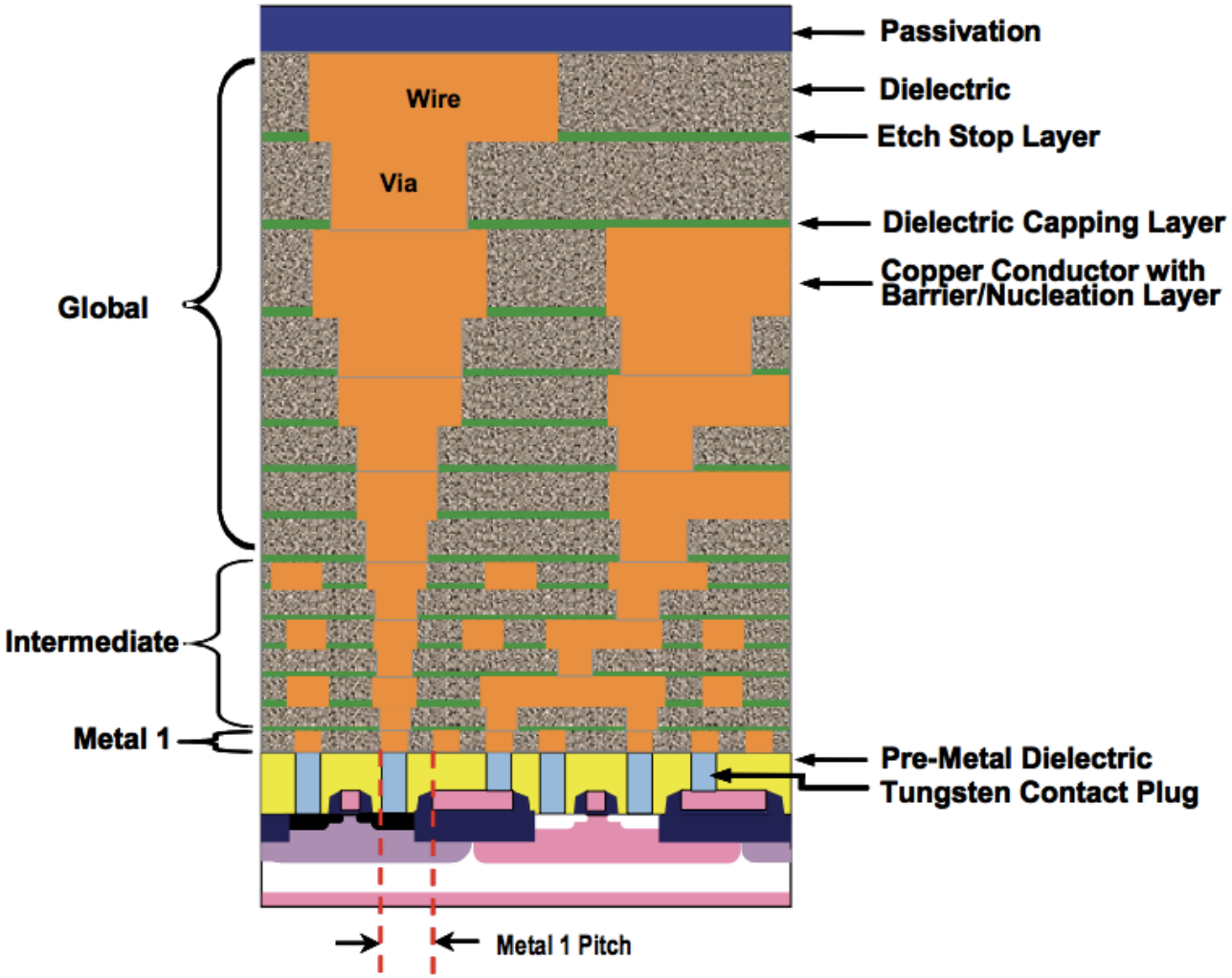
    - "Via" - metal to metal



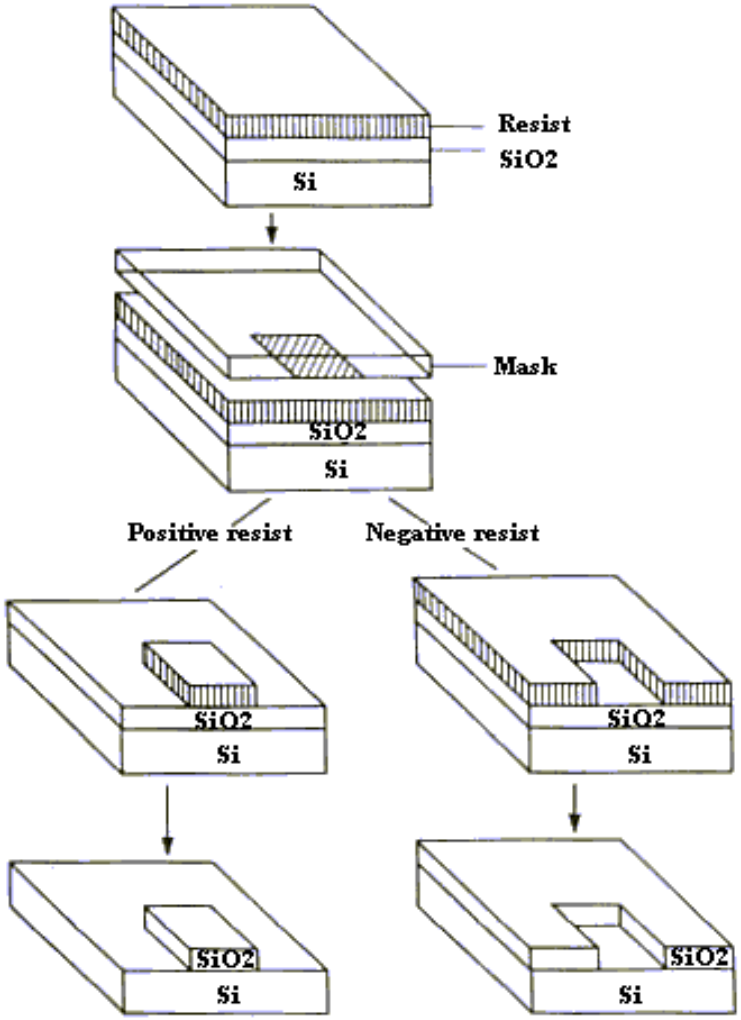
# Interconnect Cross Section



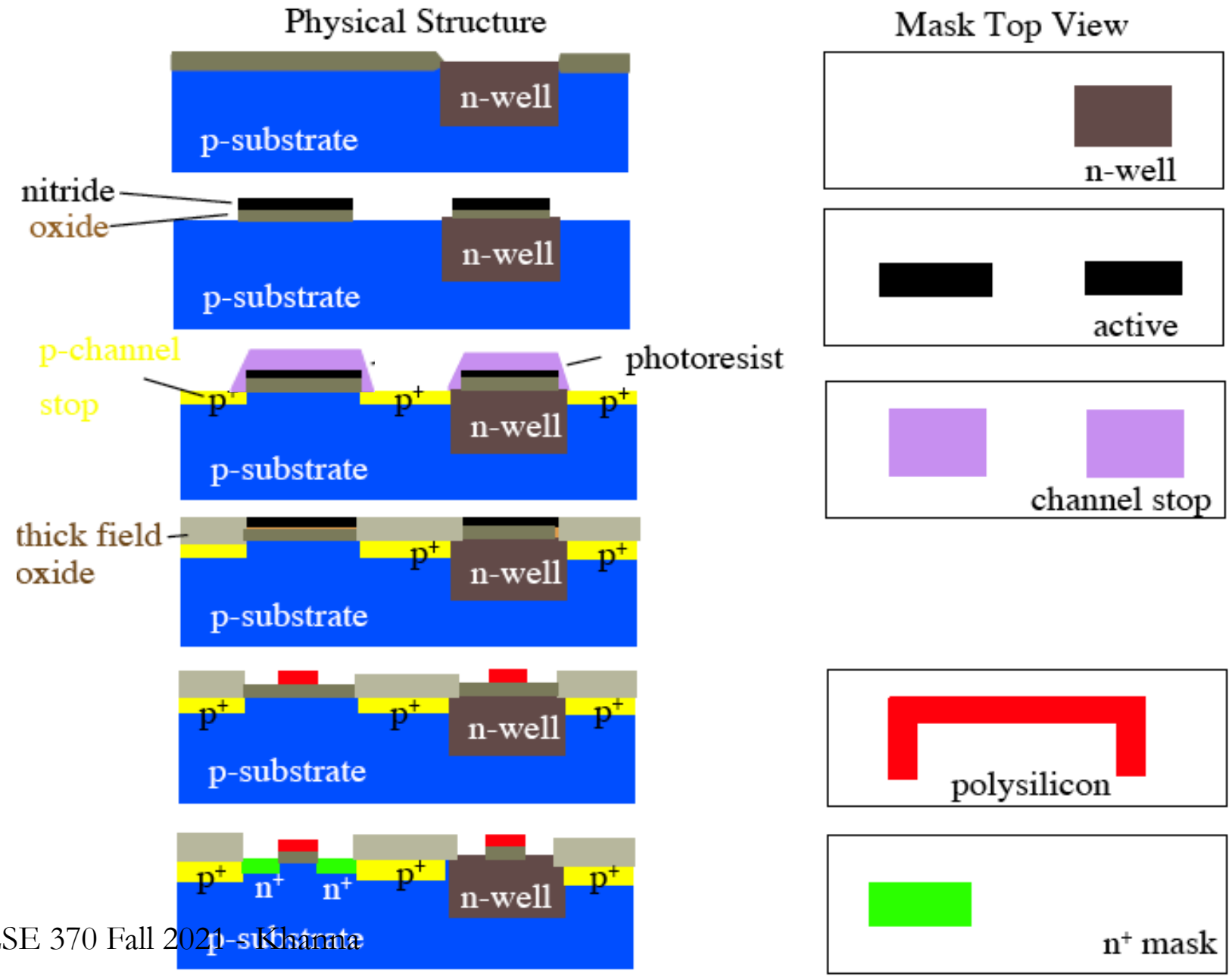

ITRS 2007

# Masks

- Define areas want to see in layer
  - Think of "stencil" for material deposition
- Use photoresist (PR) to form the "stencil"
  - Grow PR over entire wafer
  - Expose PR through mask
  - PR dissolves in exposed areas
  - Material is deposited/etched
    - Only "sticks" in area w/ dissolved PR



# Typical N-Well CMOS Process



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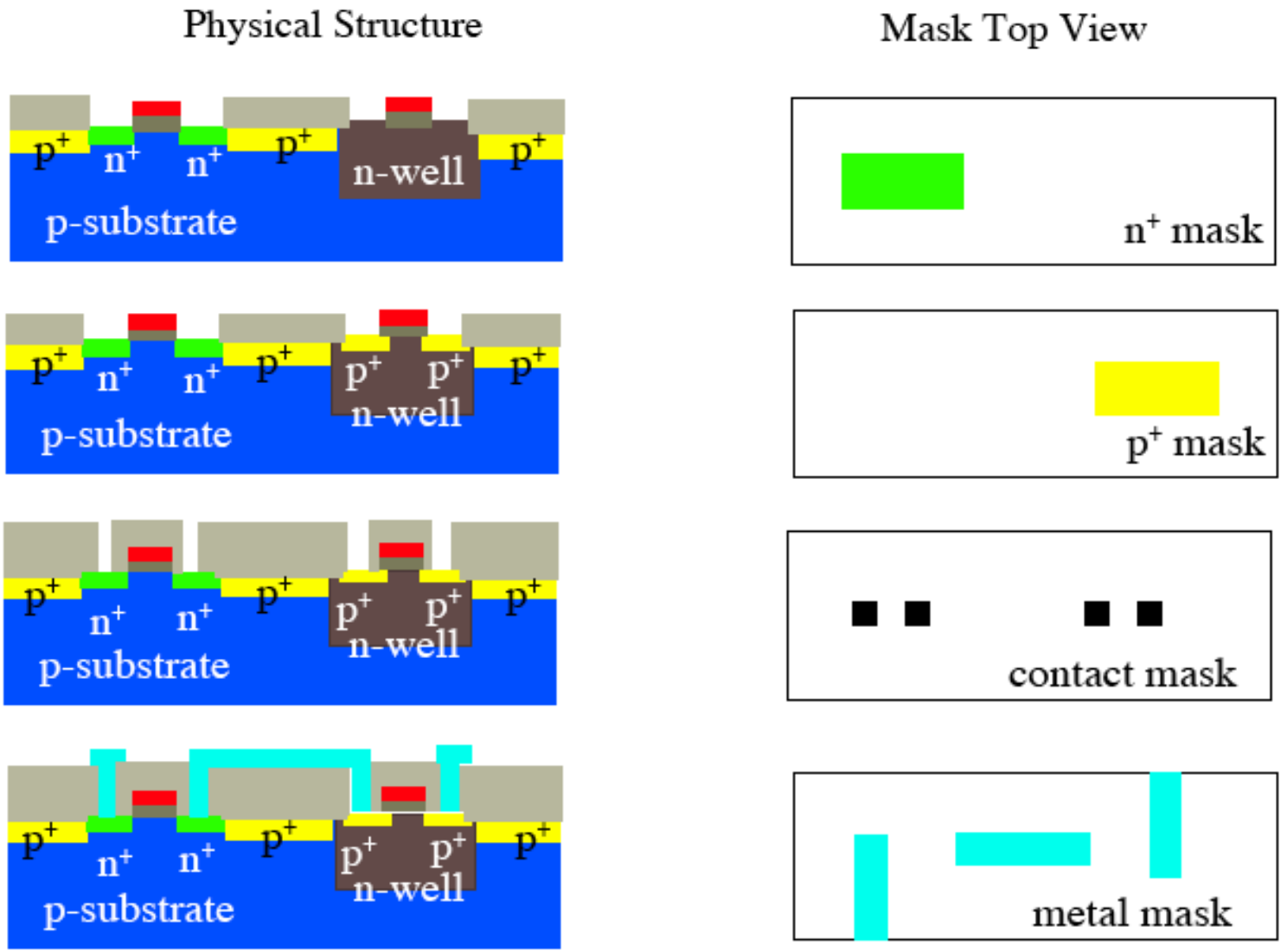
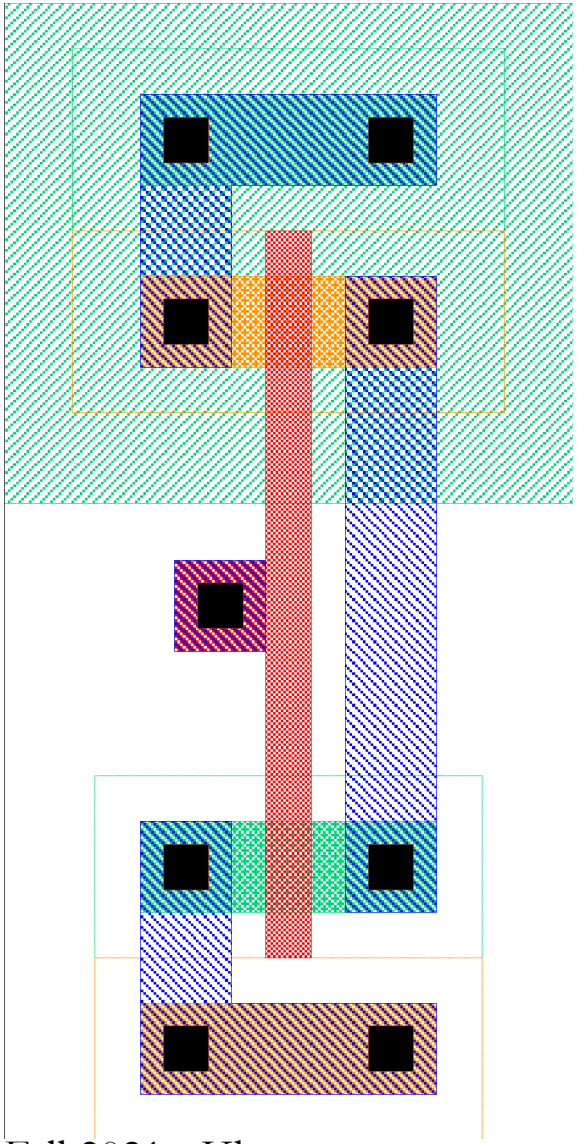
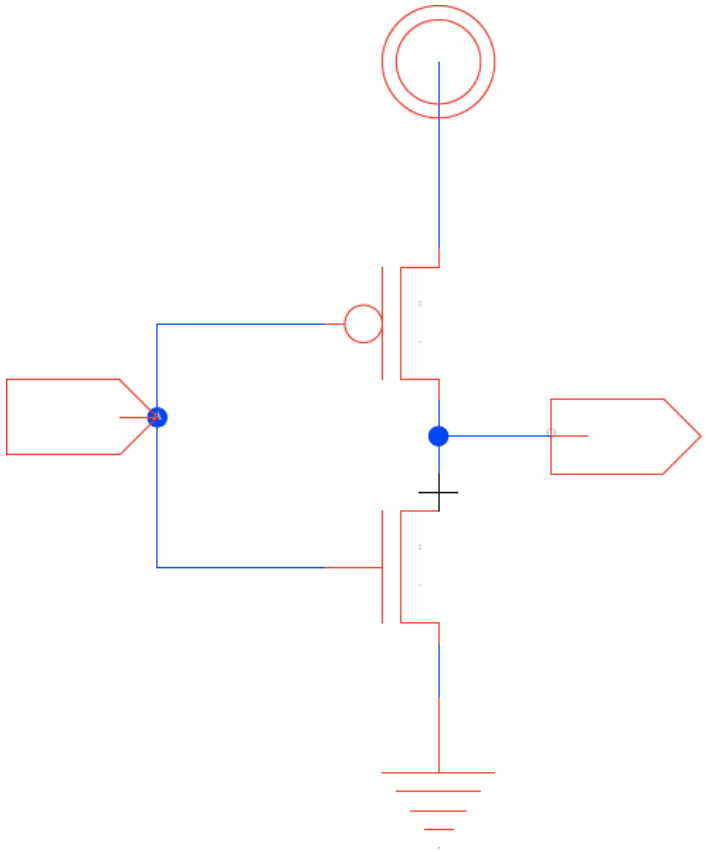
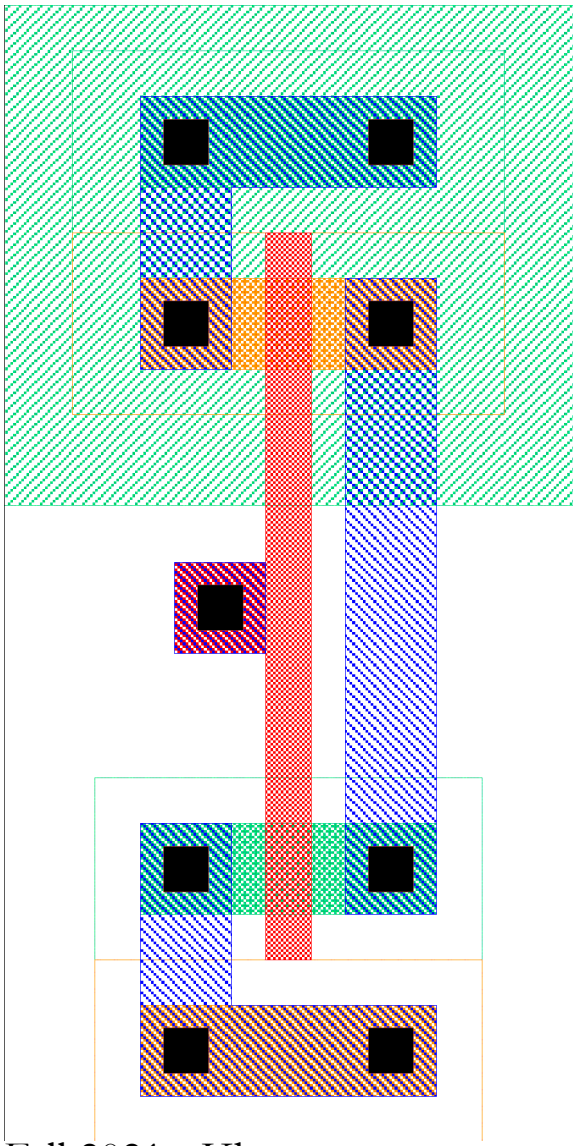


# Reverse Engineer Inverter Layout (Preclass 1)



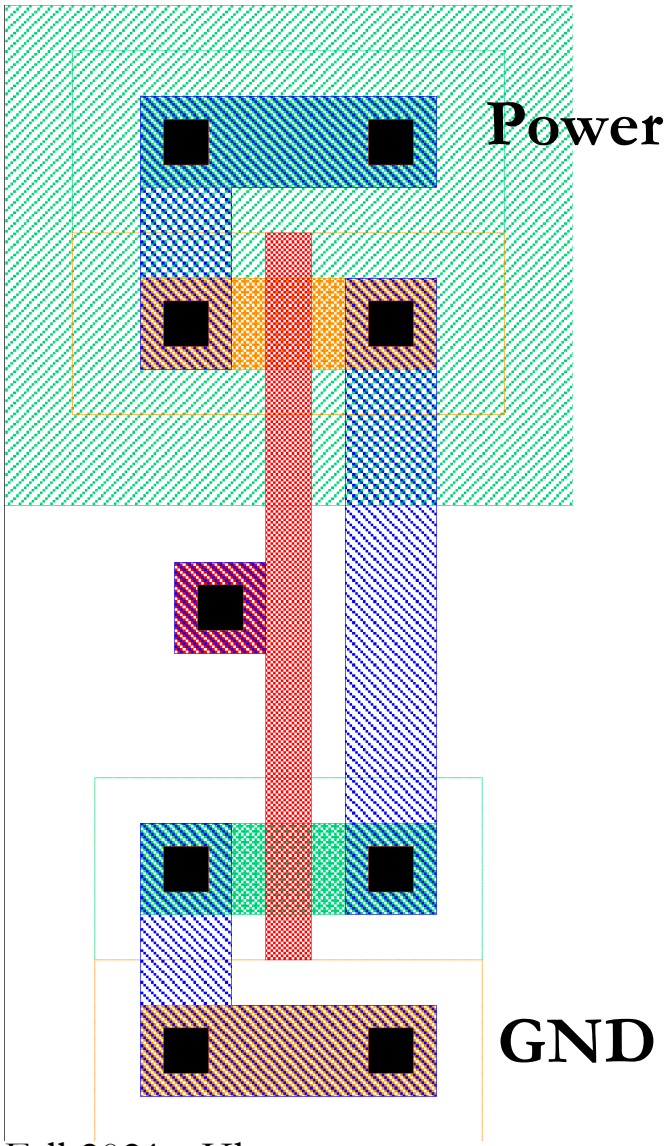


# Layout Revisited

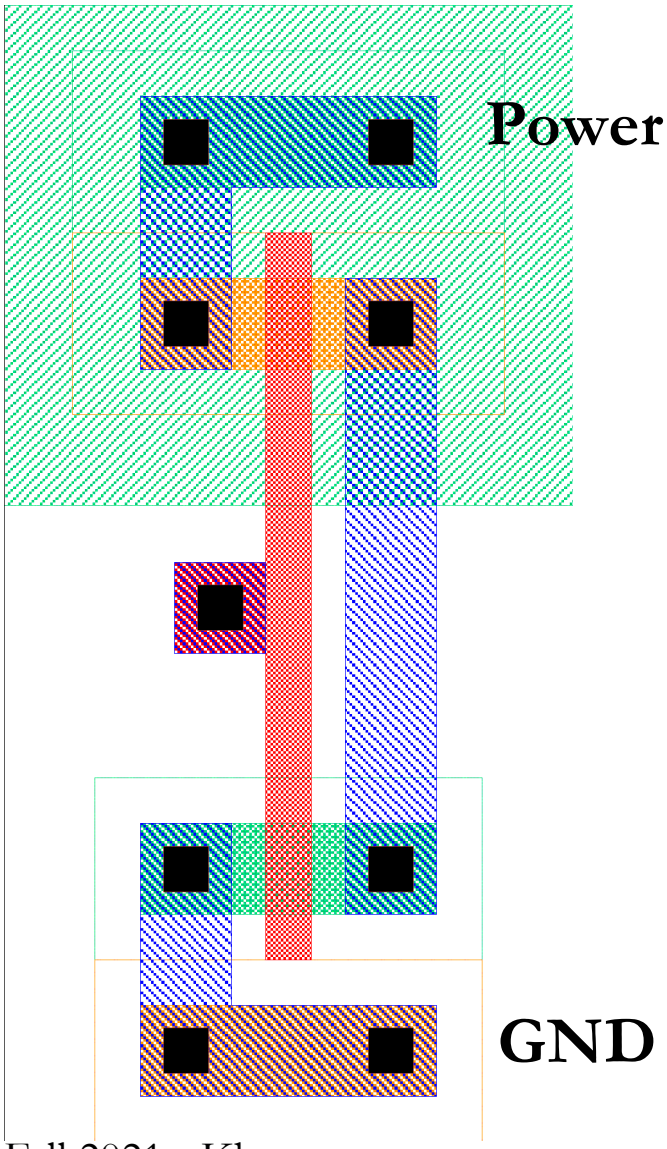


- How to "decode" circuit from layout?

# Reverse Engineer Inverter Layout

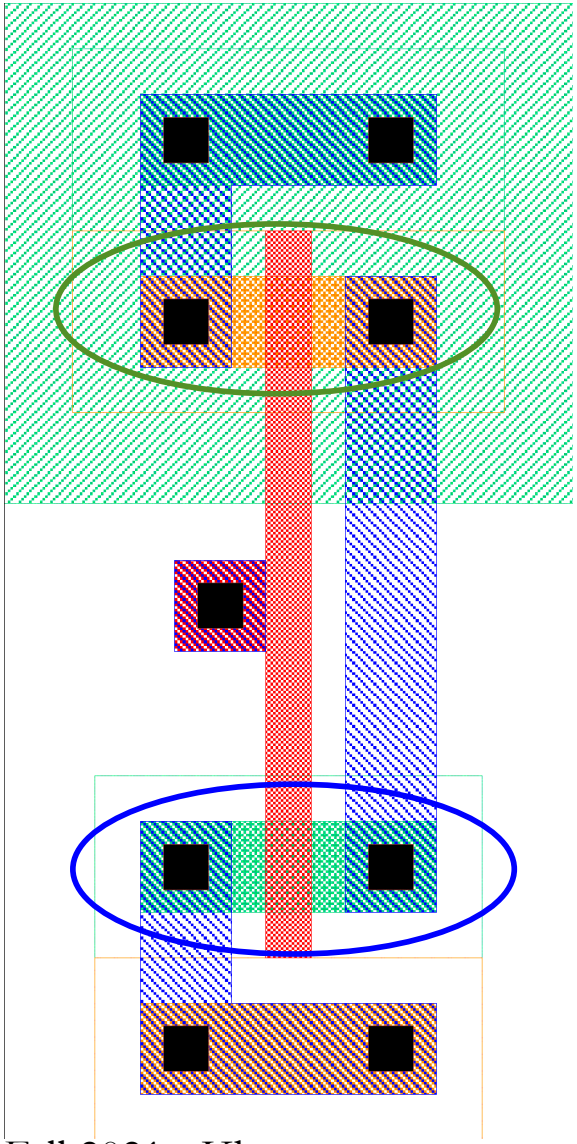


# Reverse Engineer Inverter Layout

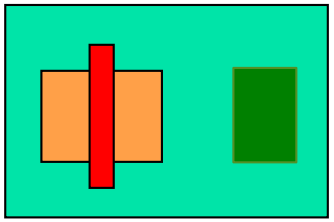


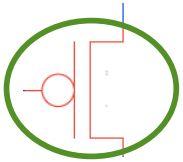

- Where is PMOS transistor?
- NMOS?

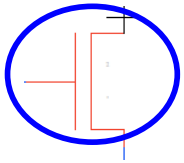
# Layout to Circuit

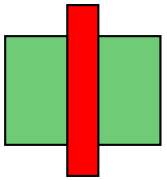


- 1. Identify transistors

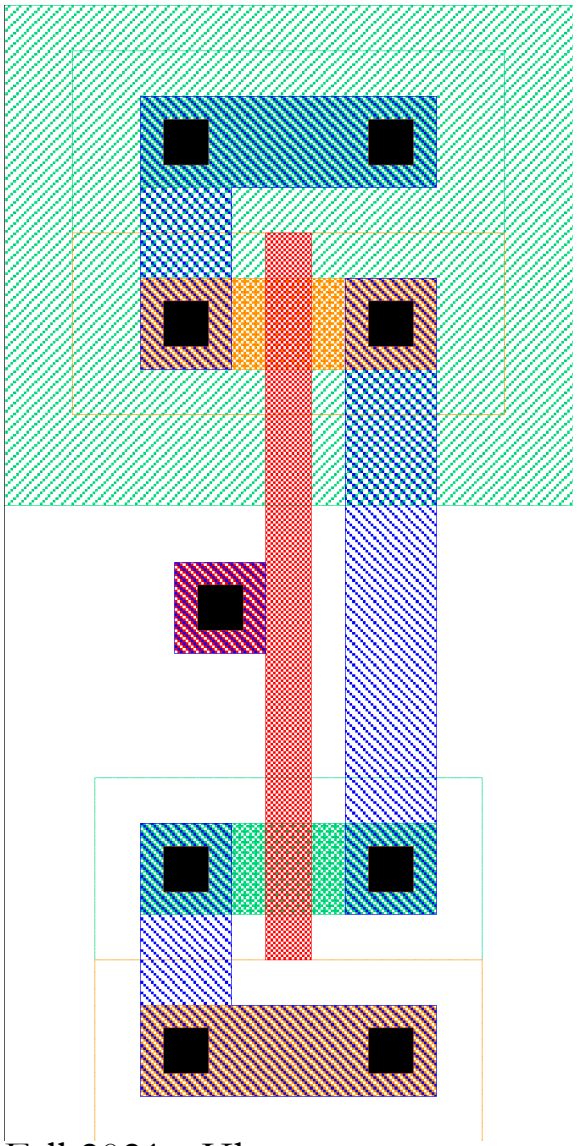






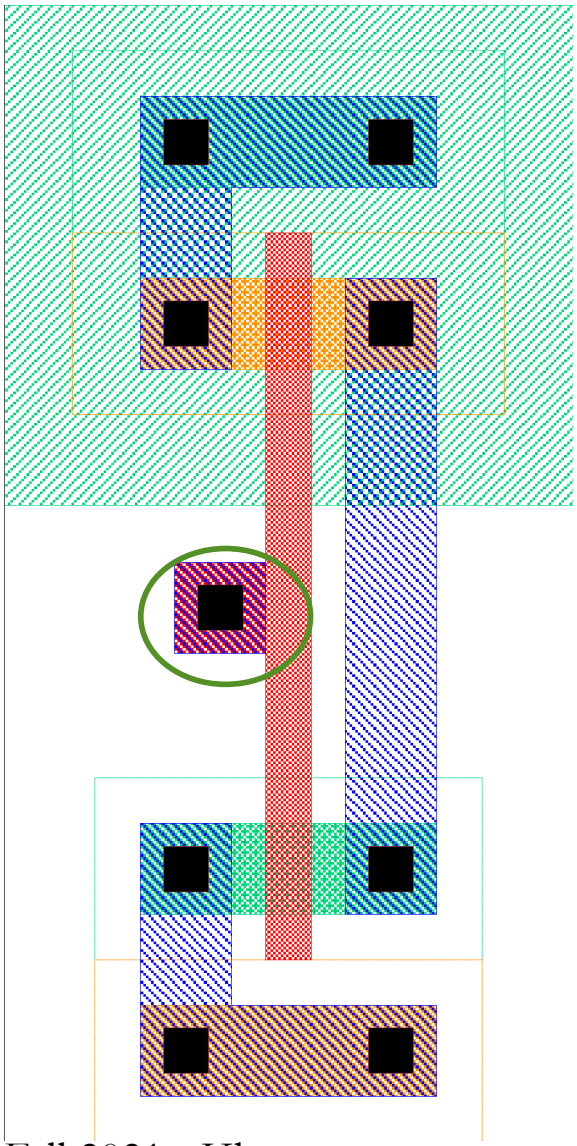


# Inverter Layout



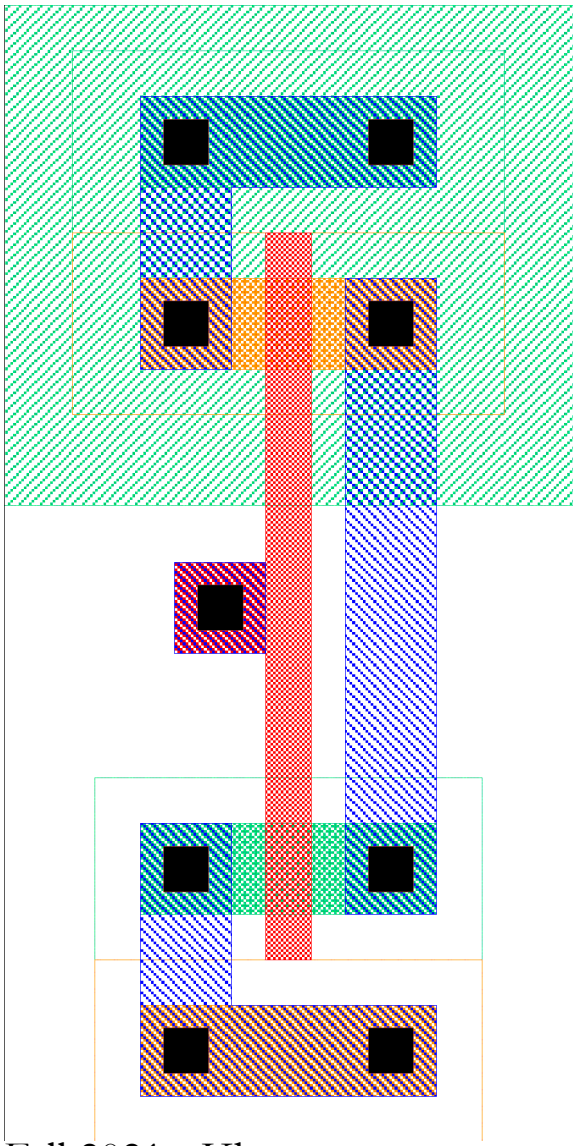
- Where is Input?

# Inverter Layout



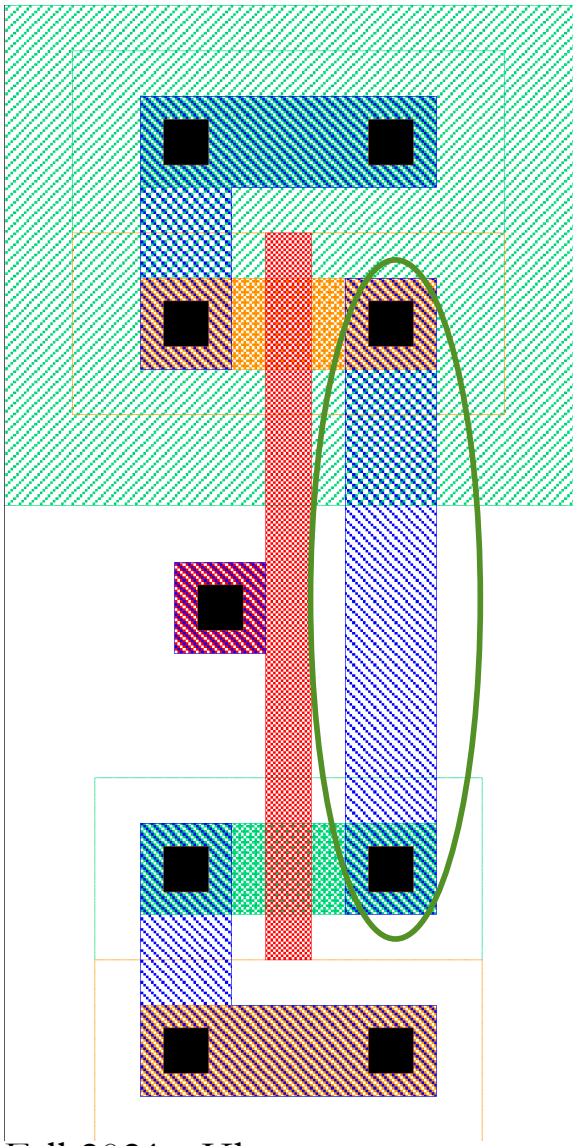
- Where is Input?

# Inverter Layout



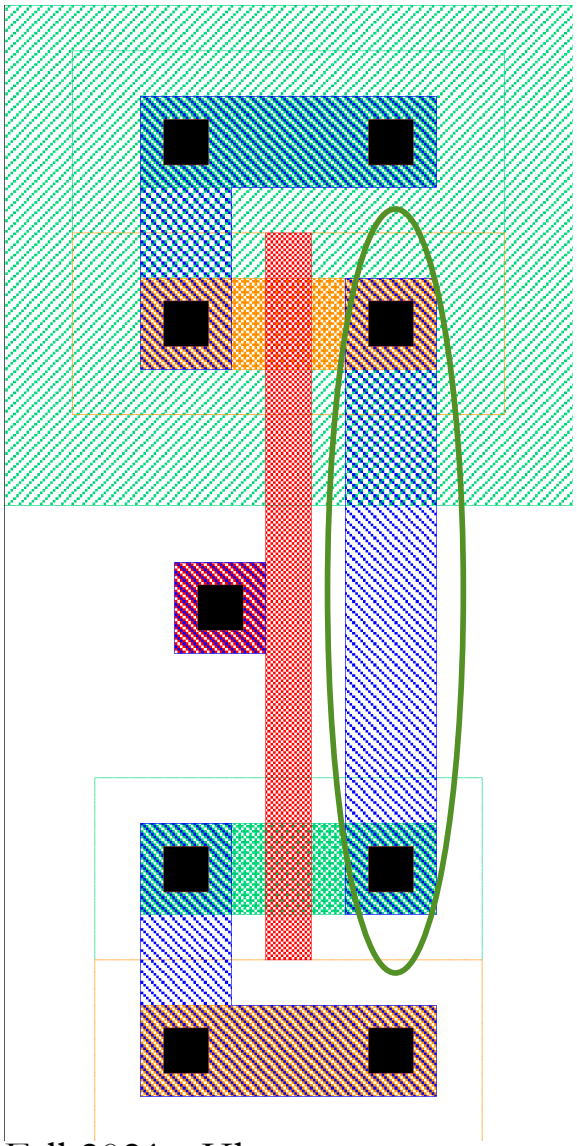
- Where is Output?

# Inverter Layout

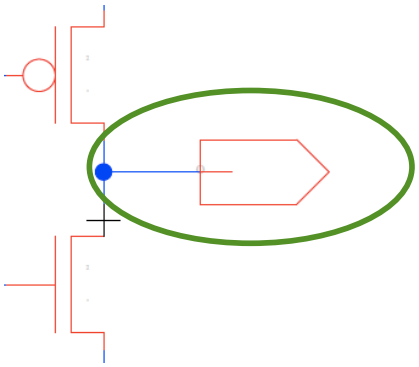


- Where is Output?

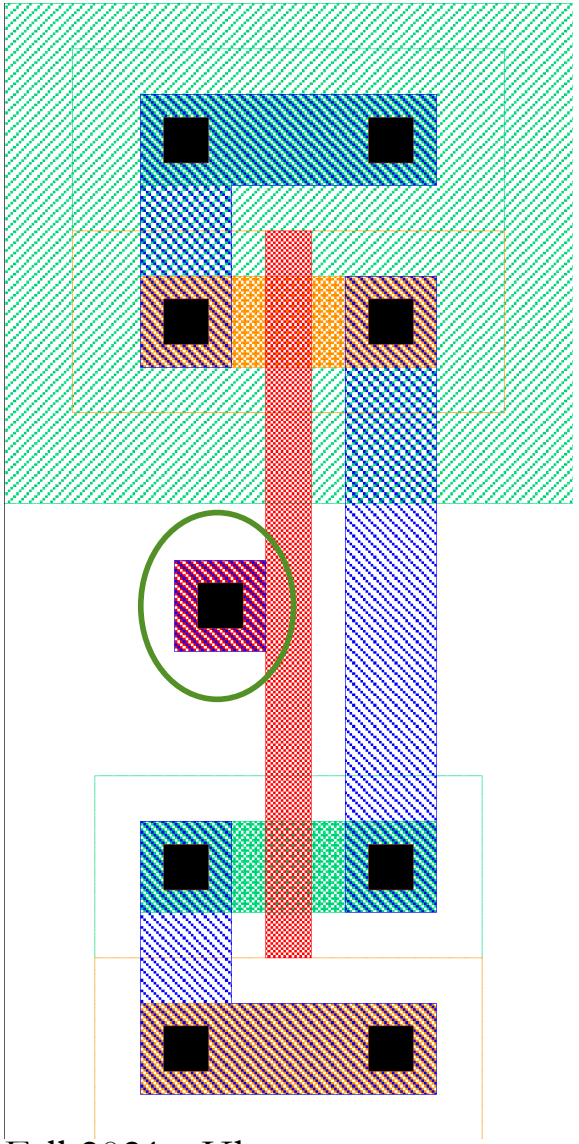
# Layout to Circuit



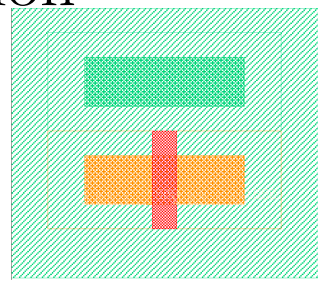
- 2. Add connections
  - Drain connection

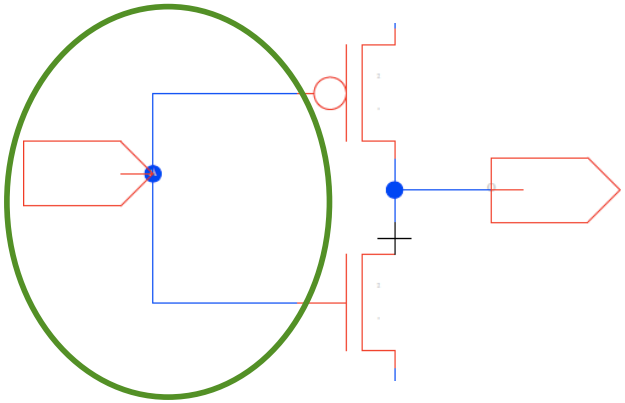


# Layout to Circuit

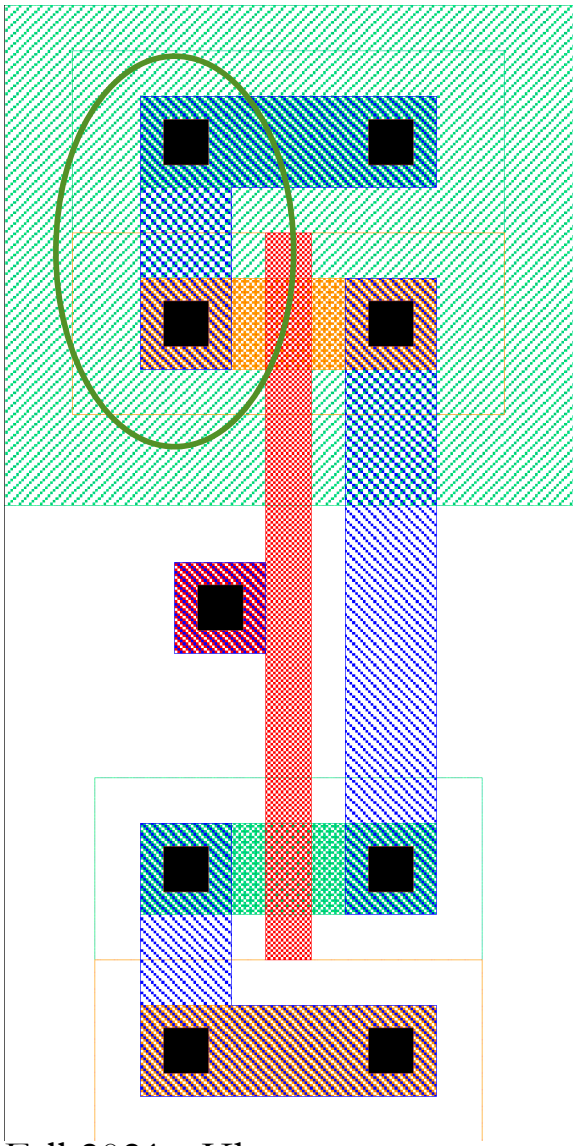


- 2. Add connections
  - Gate connection

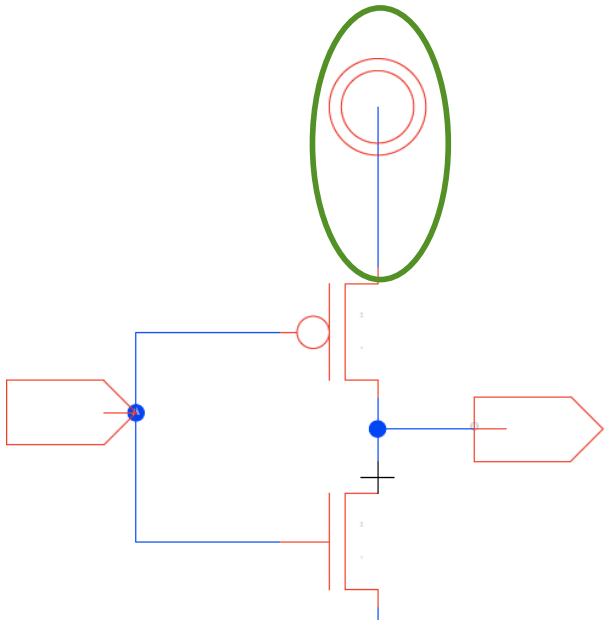




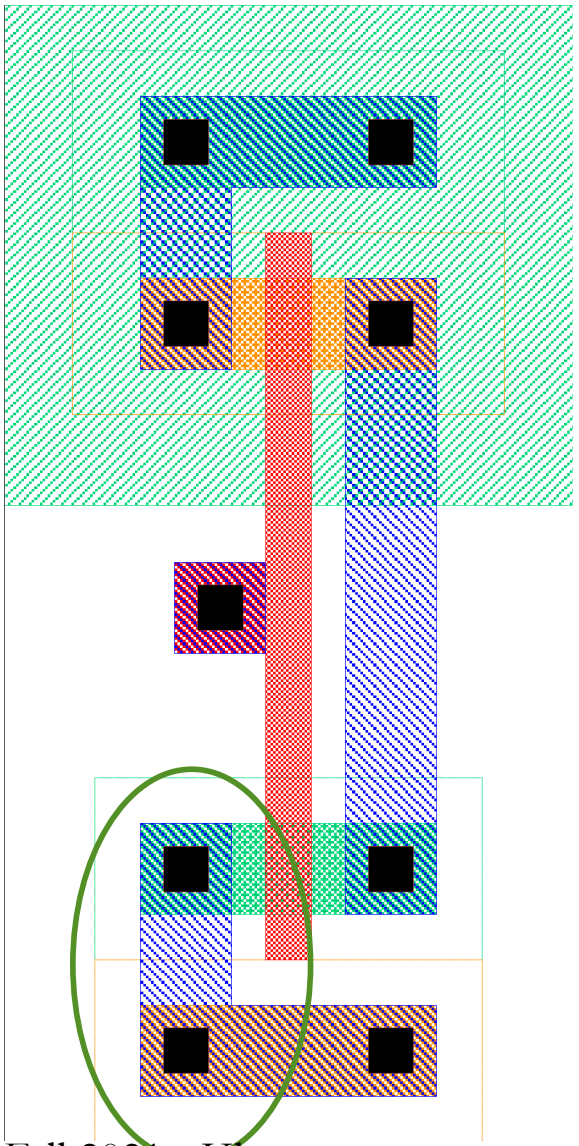
# Layout to Circuit



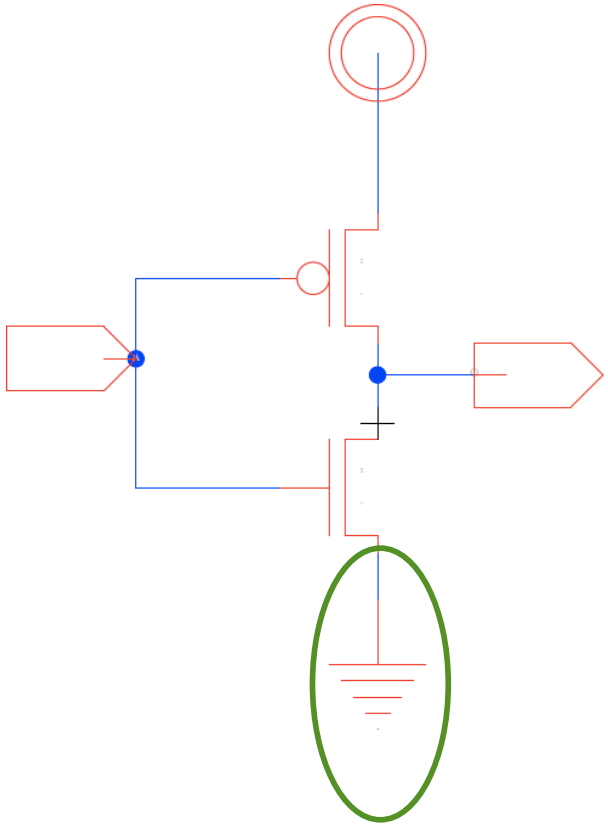
- 2. Add connections
  - pMOS-source to VDD



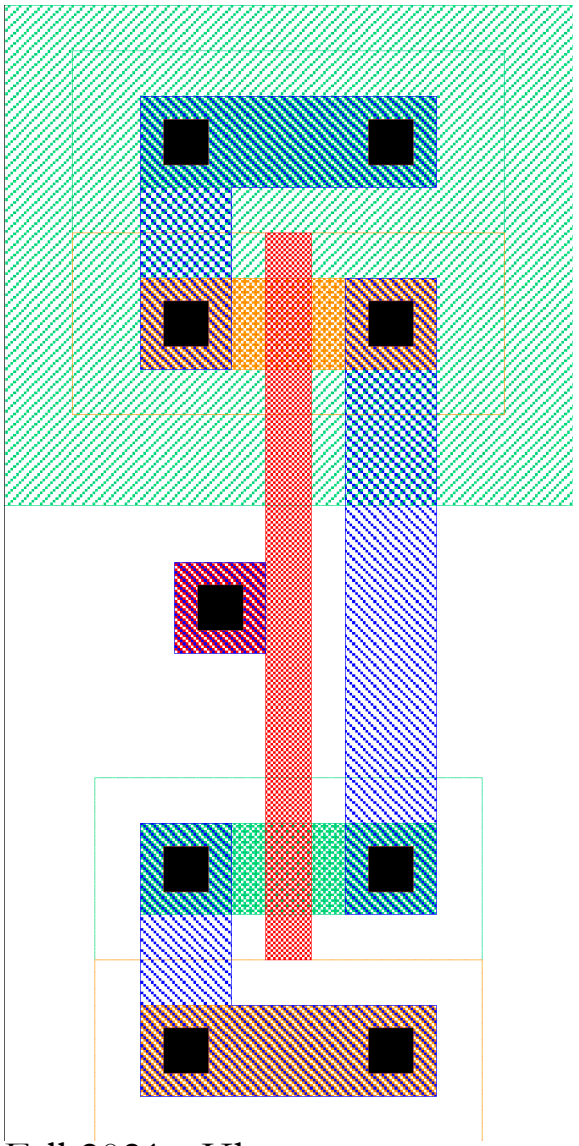
# Layout to Circuit



- 2. Add connections
  - nMOS source to GND



# Design Rules



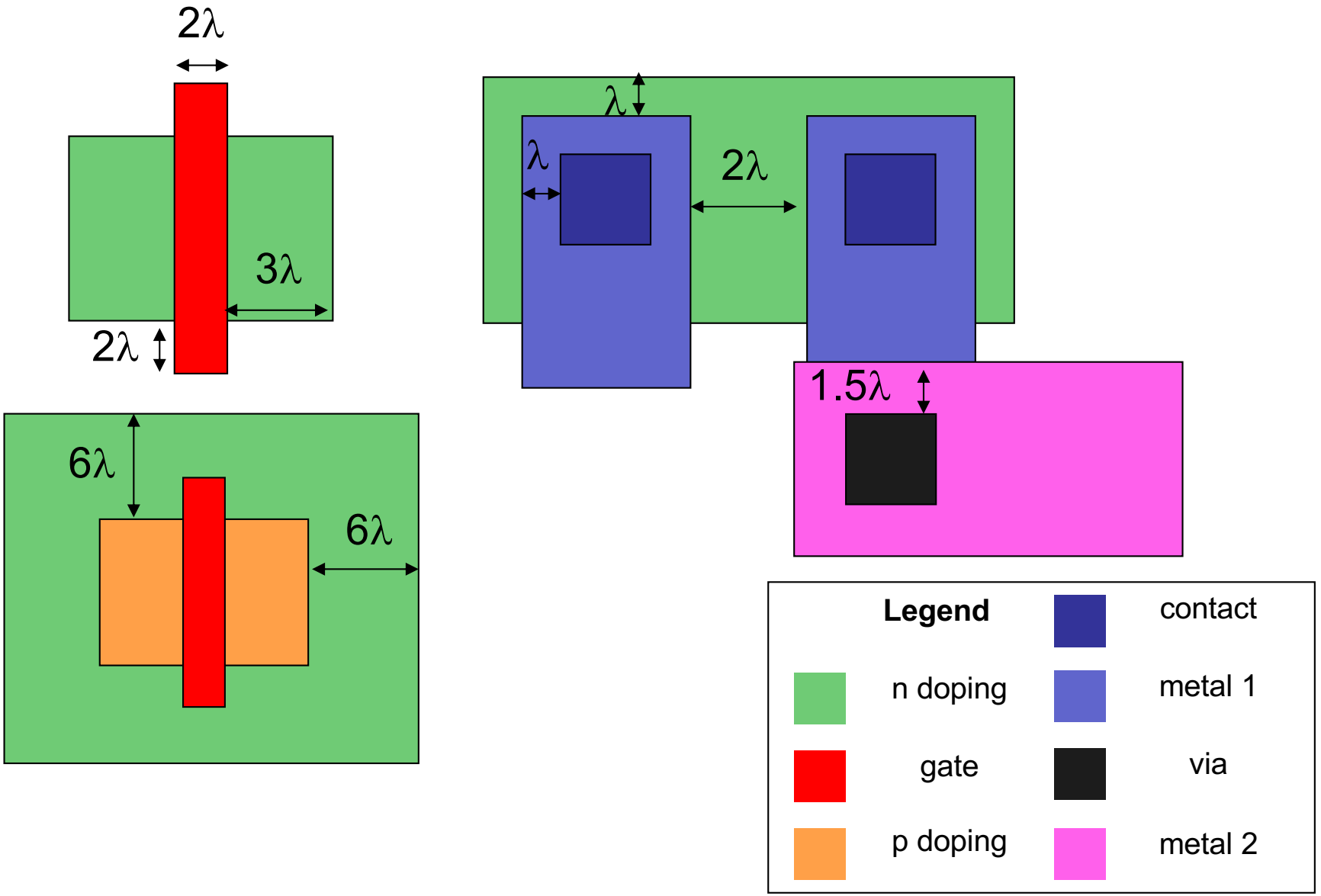
- Why not adjacent transistors?
  - Plenty of empty space
  - If area is money, pack in as much as possible
    - Shortens connections
- Recall: processing is imprecise
  - Margin of error for process variation

# Design Rules

- Contract between process engineer & designer
  - Minimum width/spacing
  - Can be (often are) process specific

- Lambda rules: scalable design rules
  - In terms of $\lambda = 0.5\ L_{min}$ ($L_{drawn}$)
  - Can migrate designs from similar process with lambda factor

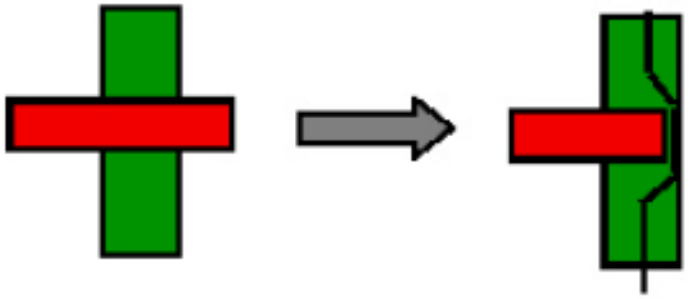
# Design Rules: Some Examples



# Potential Consequences of Design Rule Violations

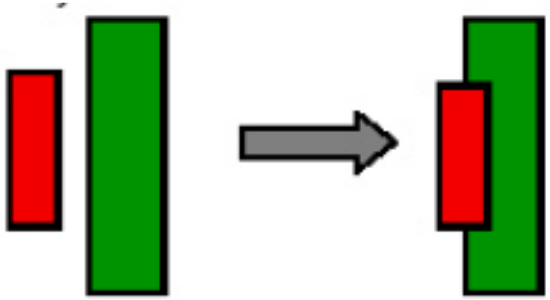
- Inter-Layer Design Rule Origins

Intended Transistor



Catastrophic Error – Unintended misalignment cause Source-Drain short circuit

Intended Unrelated Poly & Diffusion



Catastrophic Error – Unintended overlap cause fabrication of a parasitic Transistor

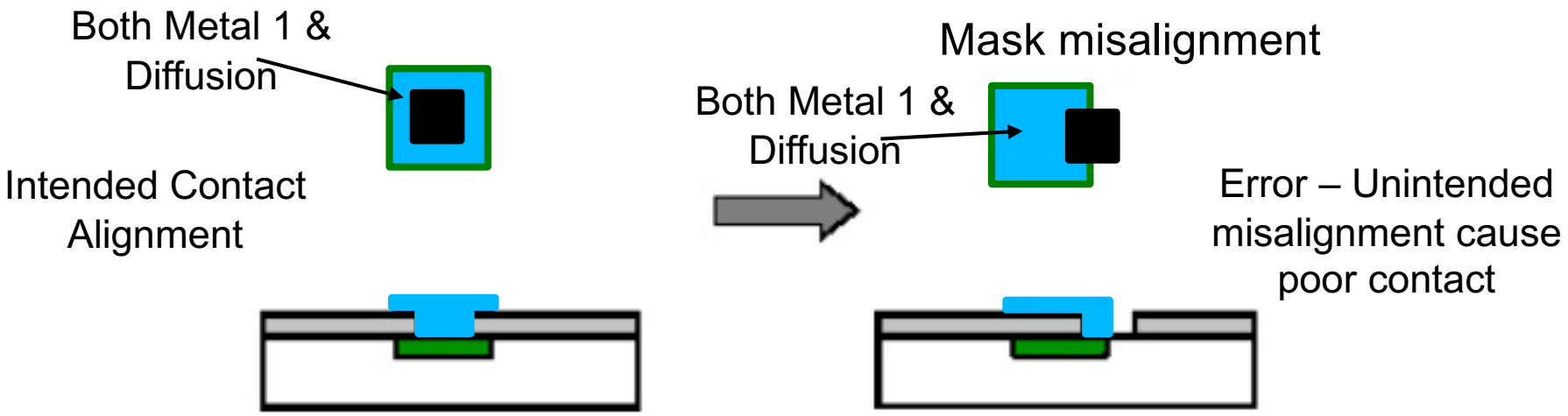
# Potential Consequences of Design Rule Violations

- Inter-Layer Design Rule Origins

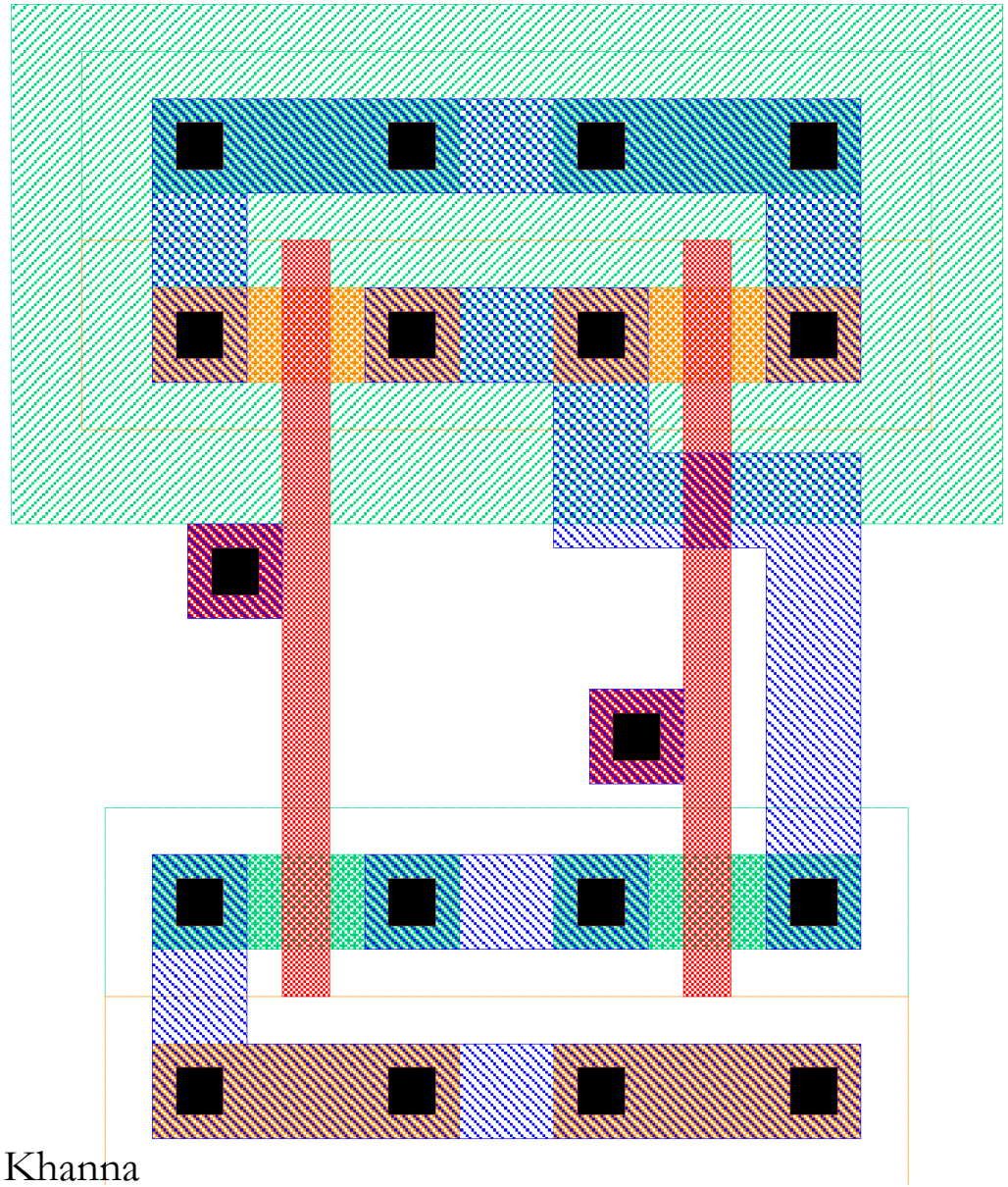
Contact and Via Masks

M1 contact to n-diffusion
M1 contact to p-diffusion
M1 contact to poly
-> Contact Mask

Mn contact to Mn-1 for n = 2, 3,.. -> Via Mask

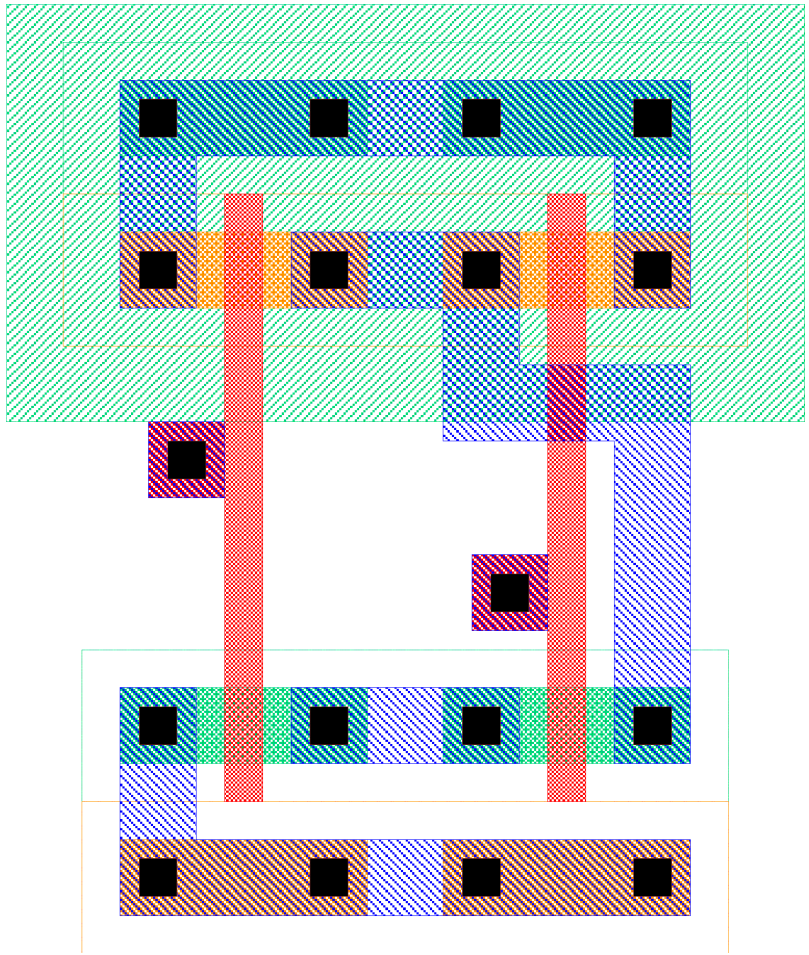


# Layout #2 (preclass 2)



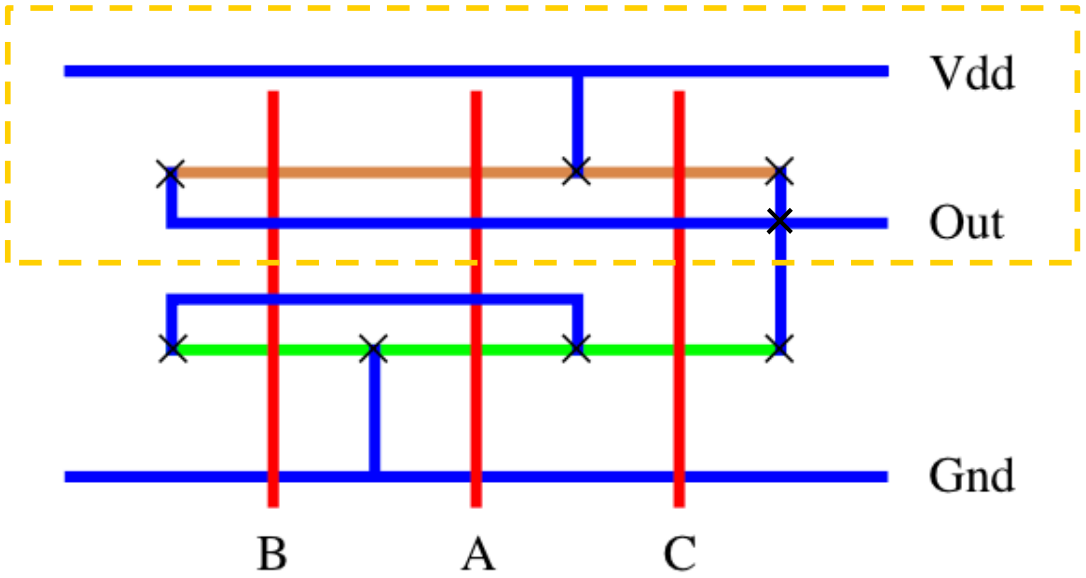
# Layout #2 (preclass 2)

- How many transistors?
  - PMOS?
  - NMOS?
- How connected?
  - PMOS, NMOS?
- Inputs connected how?
- Outputs?
- What is it?



# Symbolic Layout

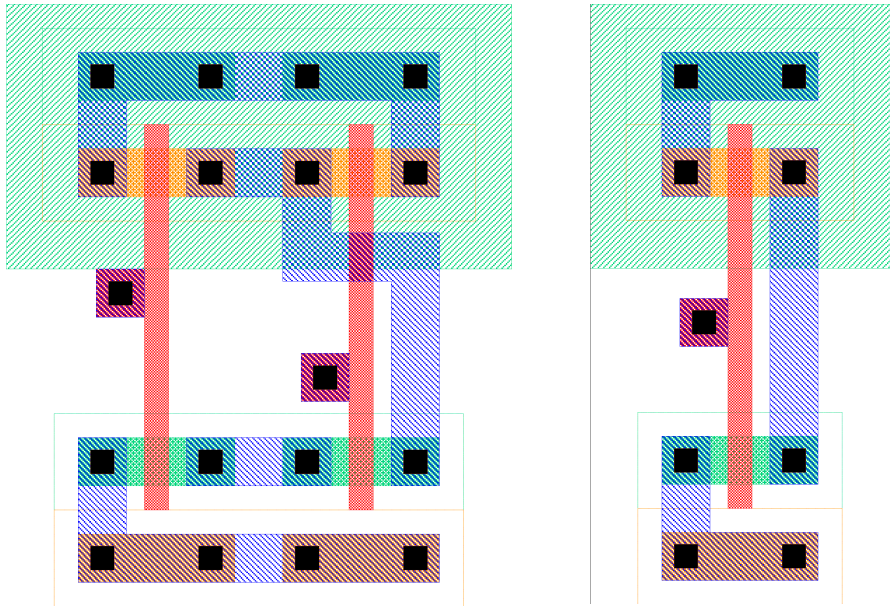
- Stick diagrams capture spatial relationships, but abstract away design rules



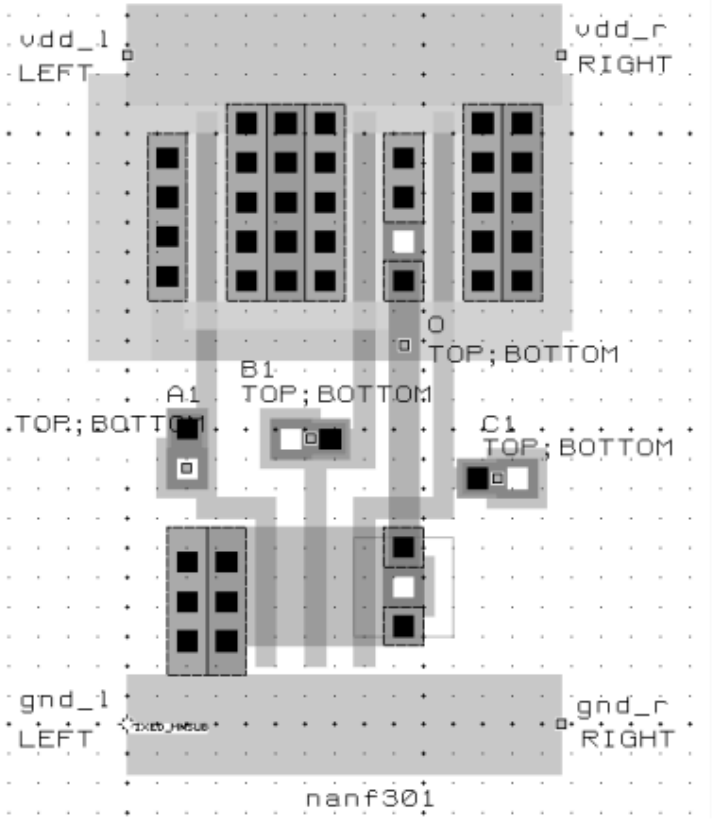

- What is the gate function?
  - How many NMOS? PMOS? D/S connections?
  - Draw schematic

# Standard Cells

- Lay out gates so that heights match
  - Rows of adjacent cells
  - Standardized sizing of gate heights
- Motivation: automated place and route
  - EDA tools convert HDL to layout



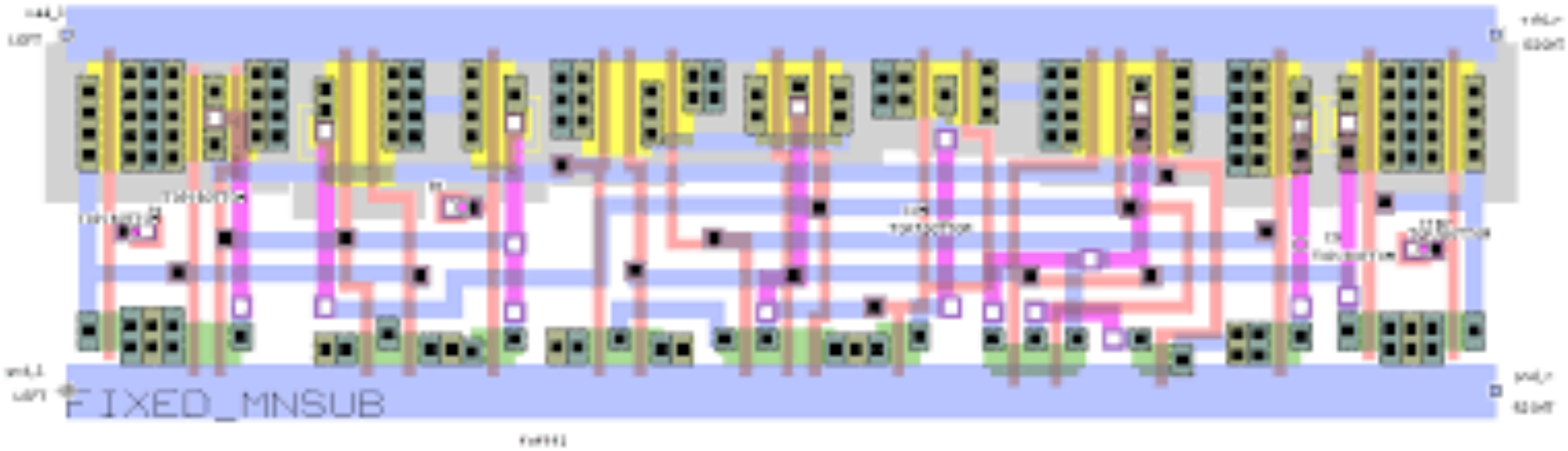
# Standard Cells



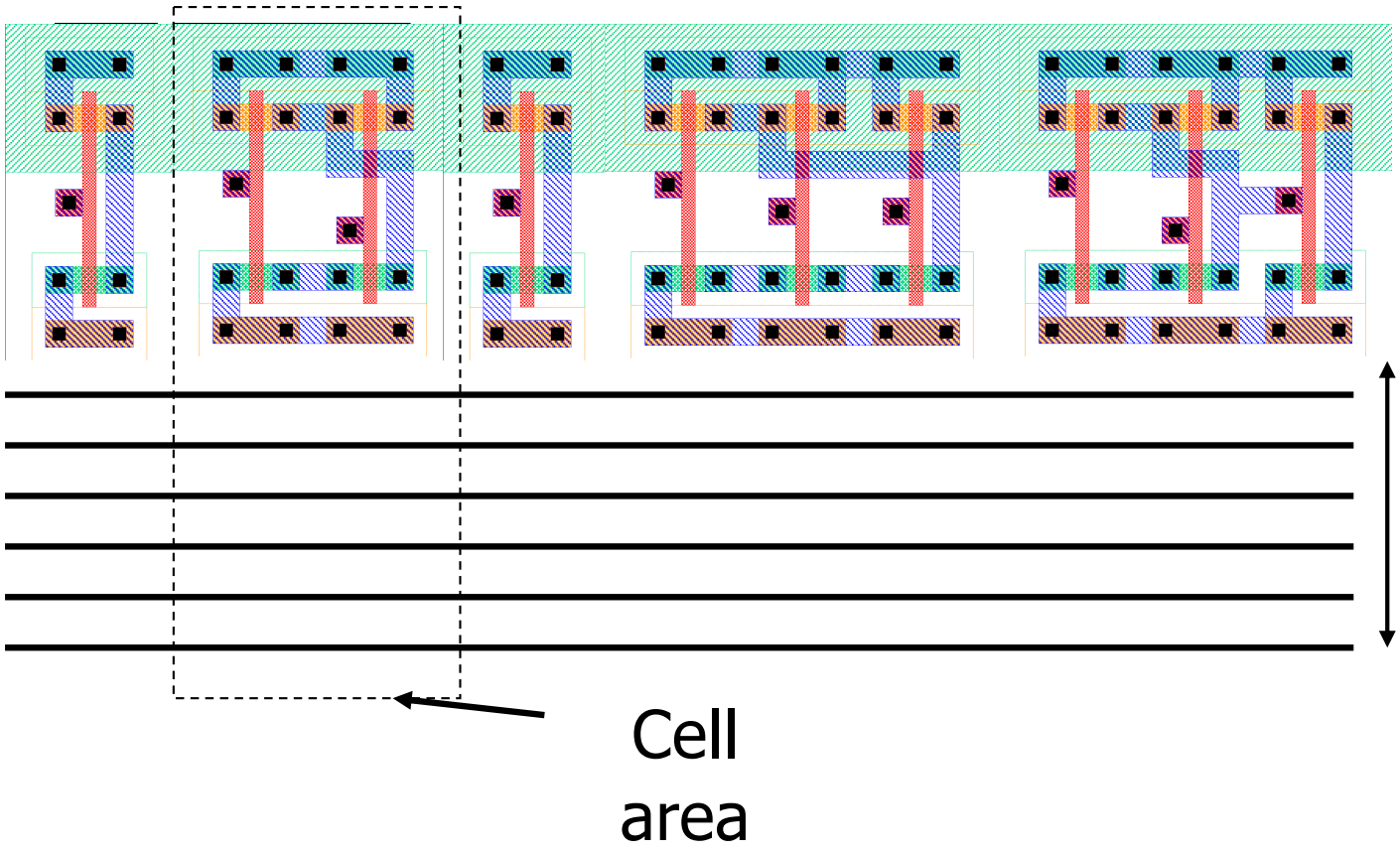

| Fanout 4x | 0.5 μm | 1.0 μm | 2.0 μm |
|---|---|---|---|
| *A1_tphl* | 0.595 | 0.711 | 0.919 |
| *A1_tplh* | 0.692 | 0.933 | 1.360 |
| *B1_tphl* | 0.591 | 0.739 | 1.006 |
| *B1_tplh* | 0.620 | 0.825 | 1.1.81 |
| *C1_tphl* | 0.574 | 0.740 | 1.029 |
| *C1_tplh* | 0.554 | 0.728 | 1.026 |

3-input NAND cell
(from Mississippi State Library)
characterized for fanout of 4 and
for three different technologies

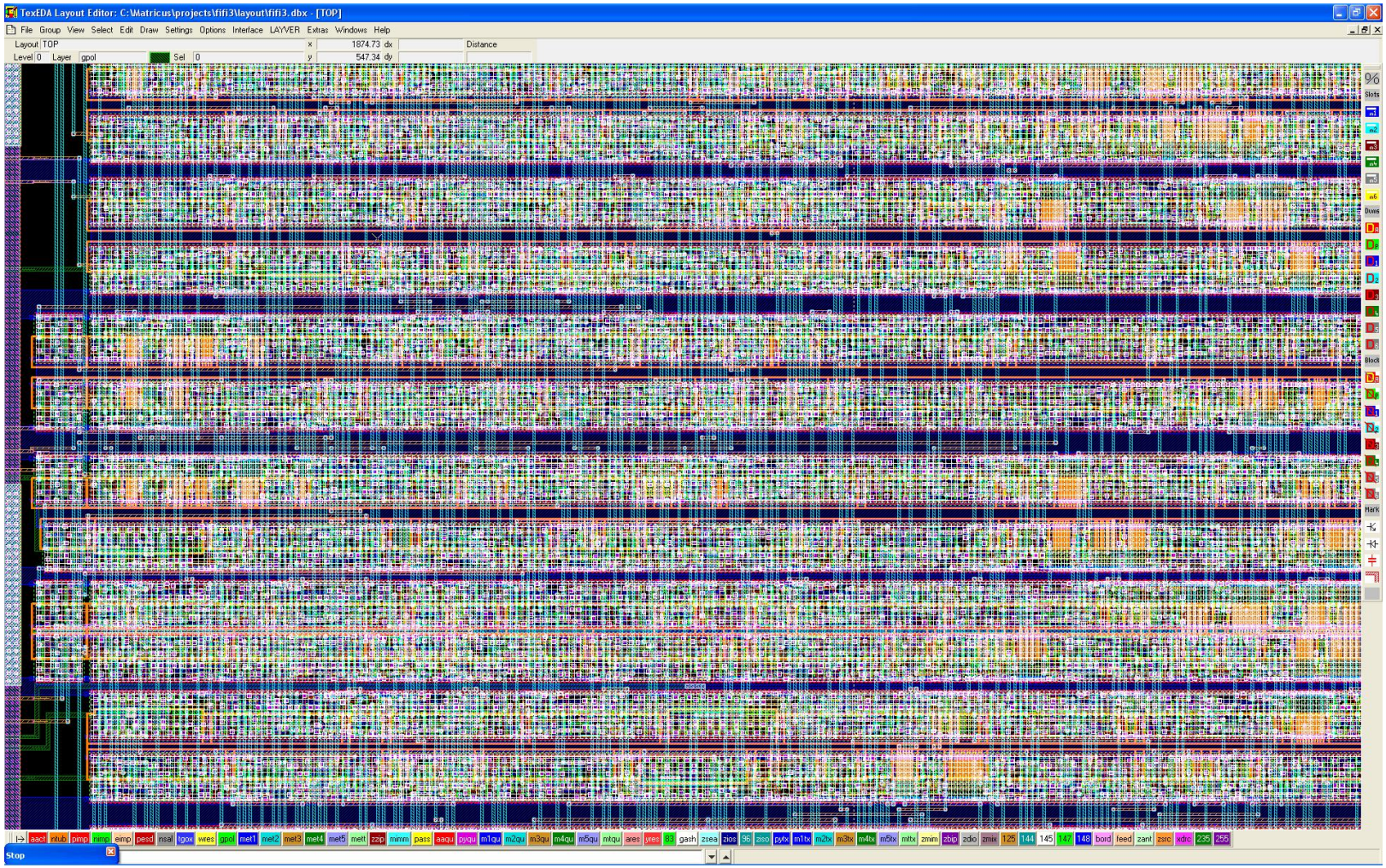
# Standard Cell Layout Example



# Standard Cell Area

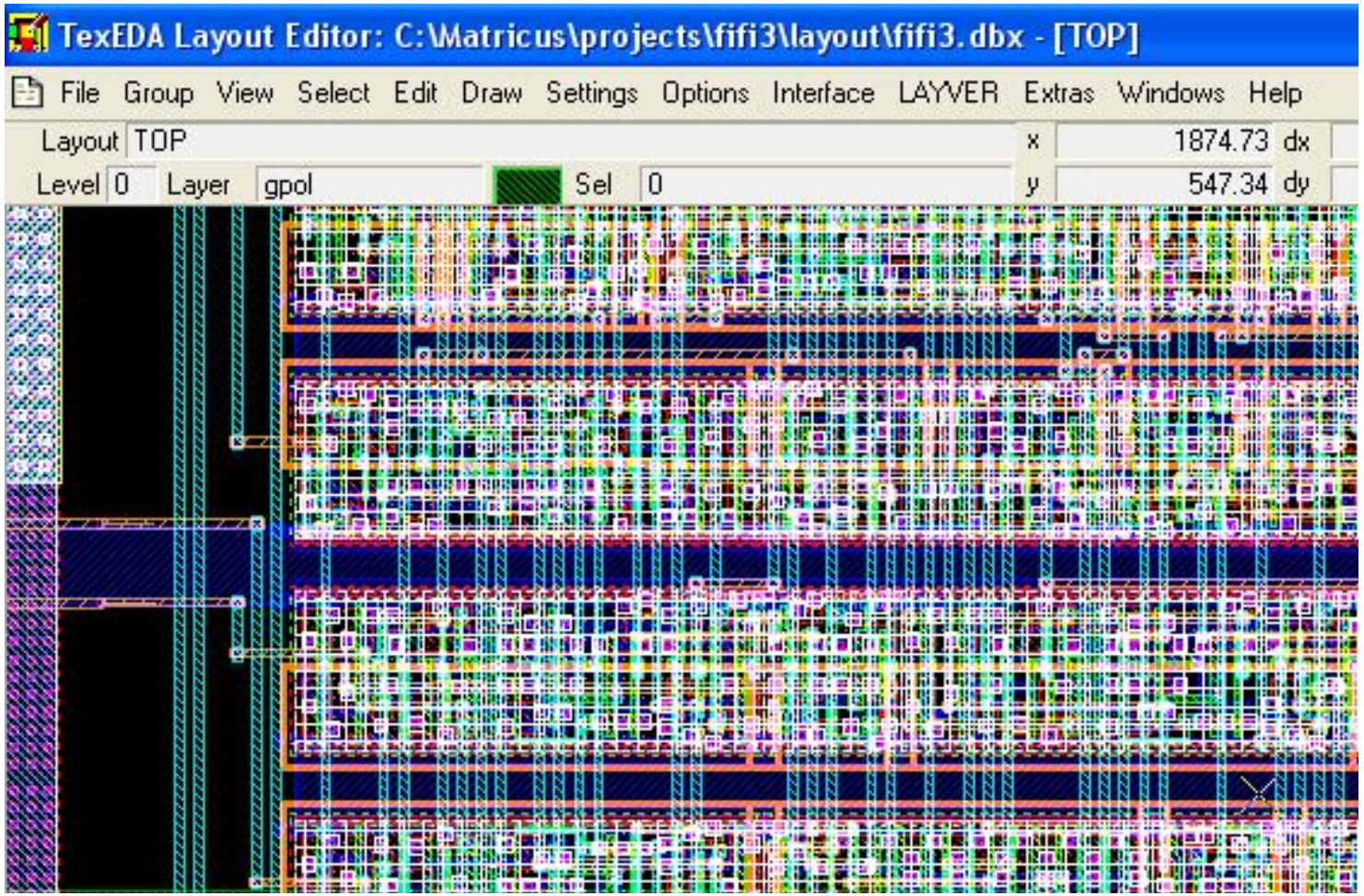


# Standard Cell Layout Example



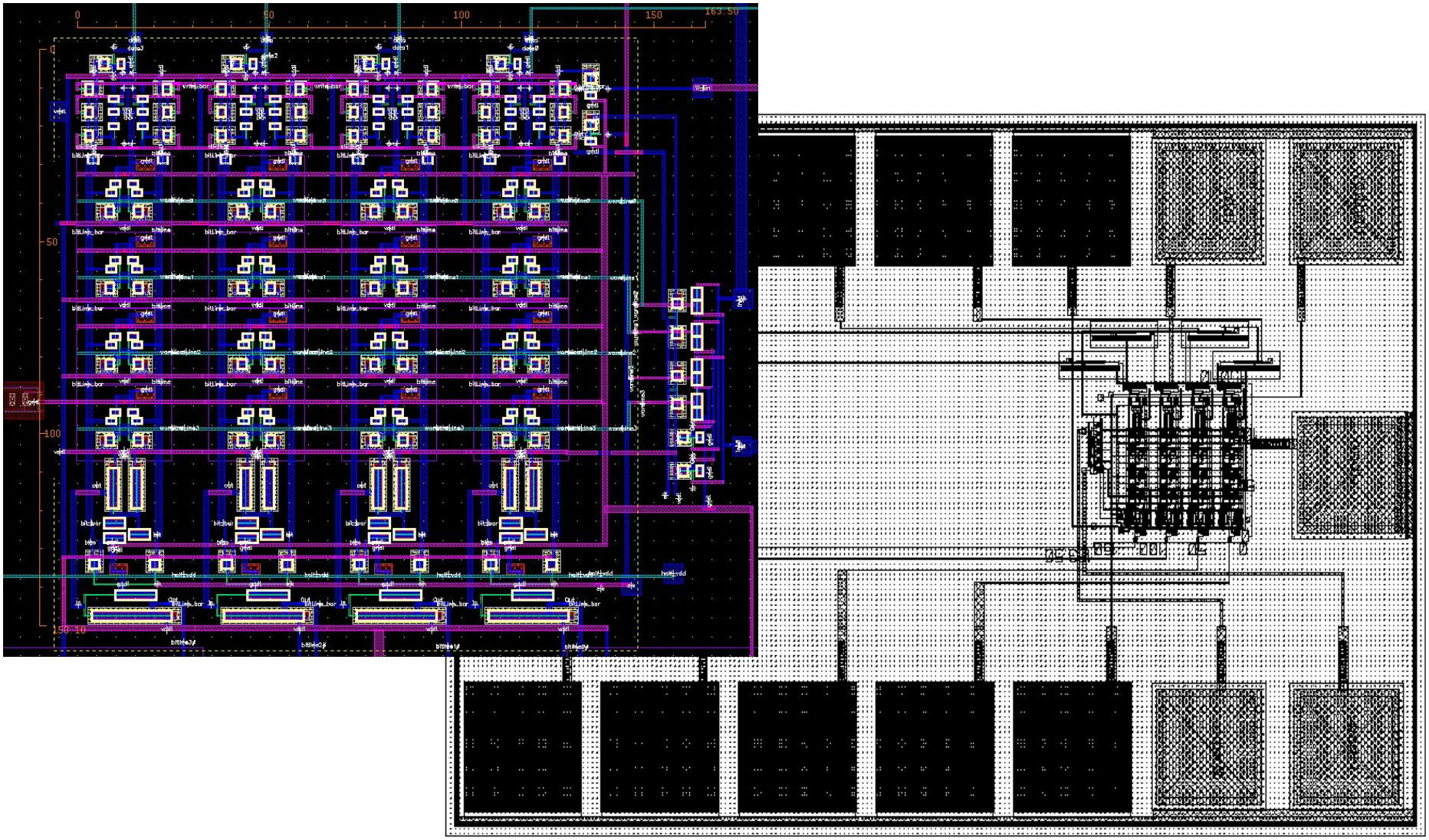

http://www.laytools.com/images/StandardCells.jpg

# Standard Cell Layout Example



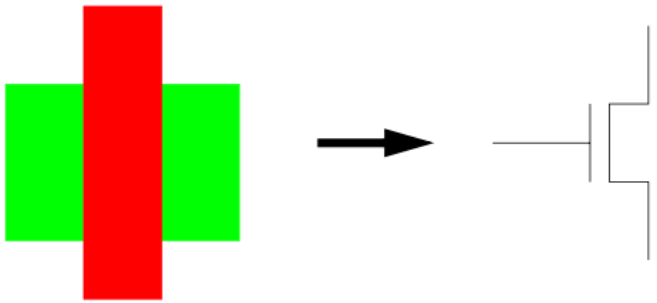

http://www.laytools.com/images/StandardCells.jpg

# 4x4 6T SRAM Memory



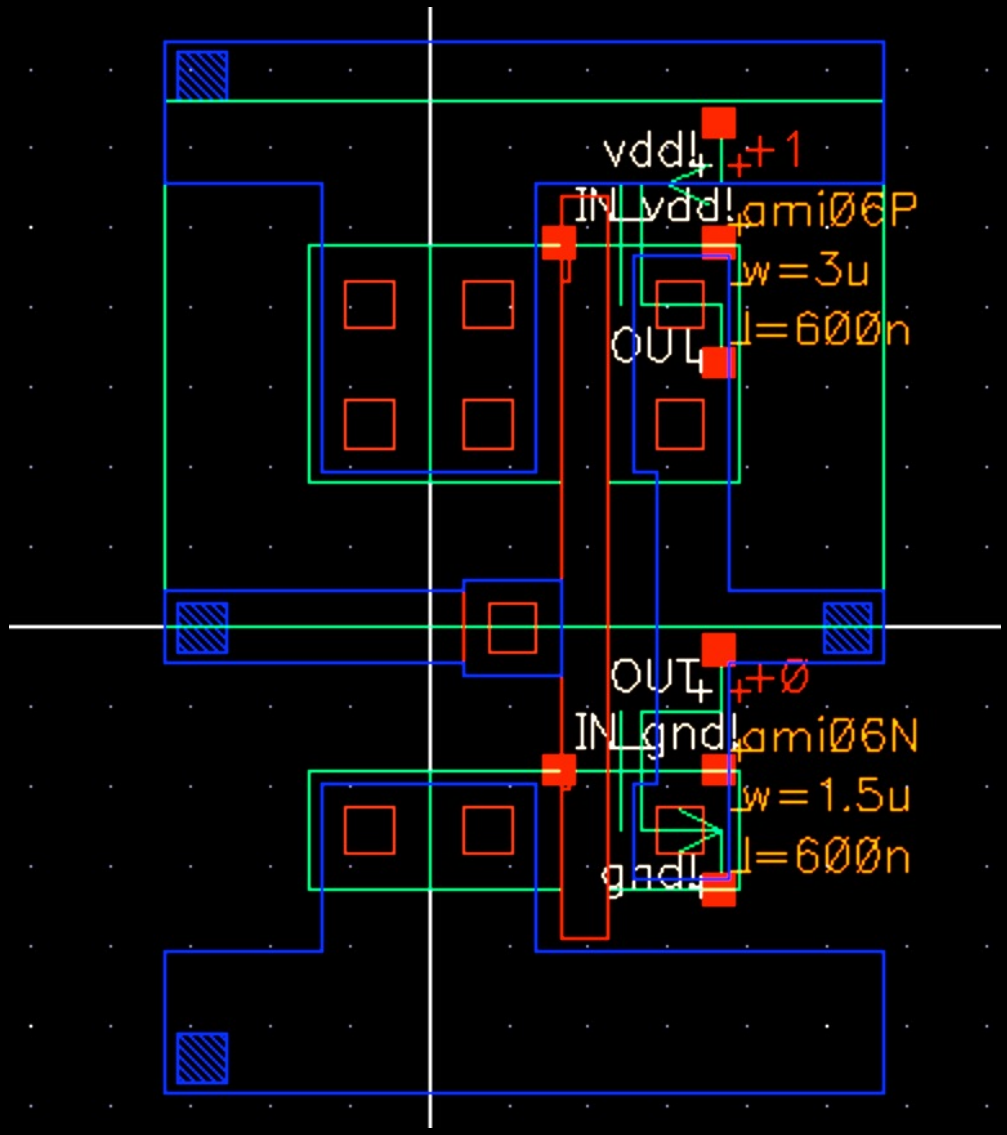
# Circuit Extraction

- Circuit extraction extracts a schematic representation of a layout, including transistors, wires, and possibly wire and device resistance and capacitance.

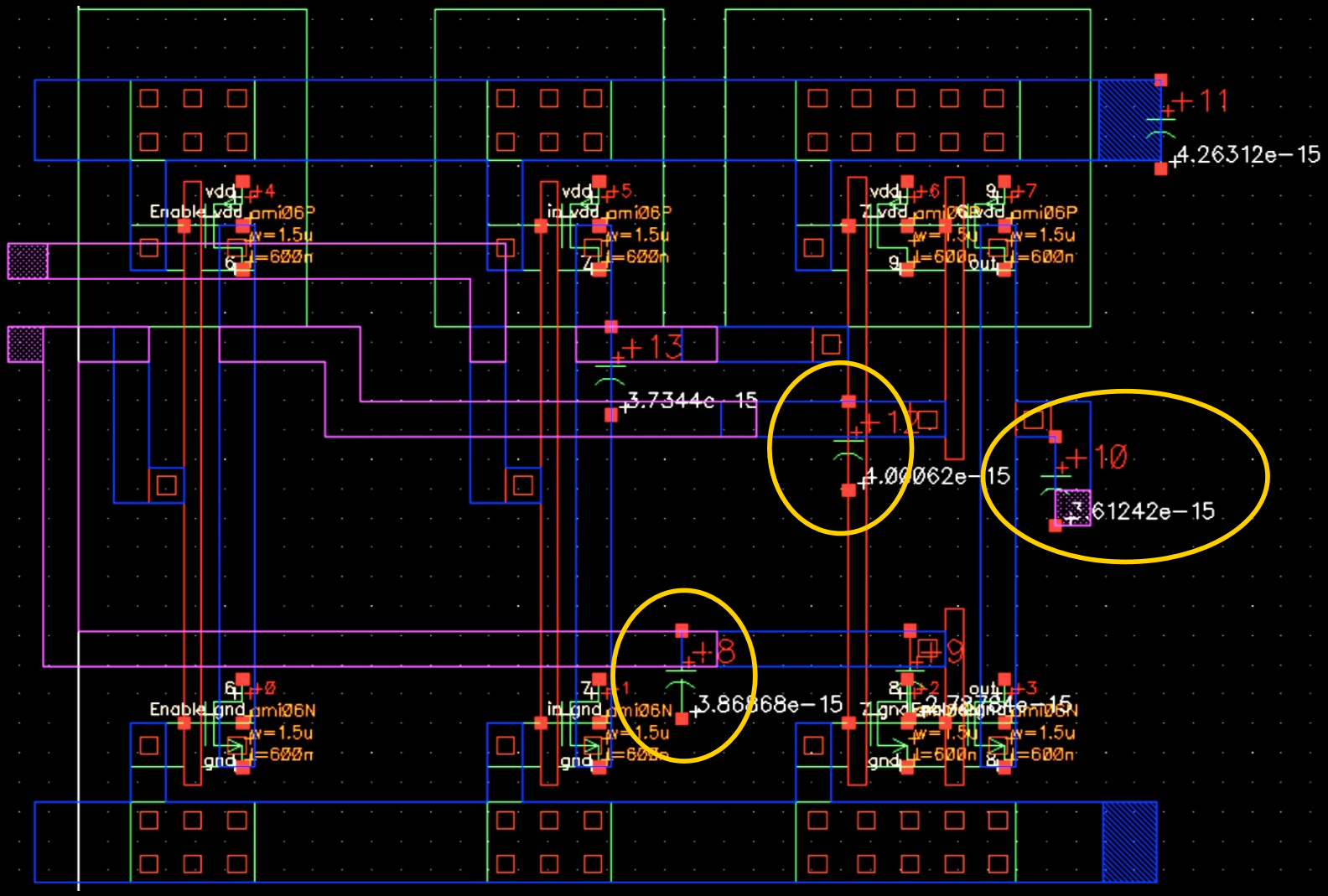


- Circuit extraction is used for LVS, and for spice simulation of layouts

# Circuit Extraction

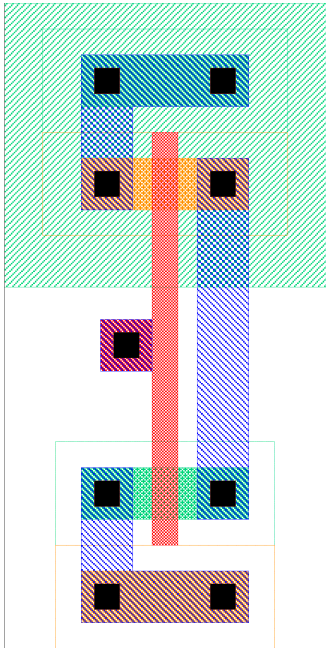


# Circuit Extraction



# Big Idea

- Layouts are physical realization of circuit
  - Geometry tradeoff
    - Can decrease spacing at the cost of yield
    - Design rules
- Can go from circuit to stick diagram/layout or stick diagram/layout to circuit by inspection



# Admin

- Midterm 1 Friday 10/1
  - 7-9pm in Towne 309
  - No Lecture, virtual office hours
    - Use Tania OH link on Piazza
  - Virtual review session on Wednesday, will be recorded
    - See Piazza for updates
- HW 4 posted Friday 10/1 after midterm
  - Due following Friday 10/8 @midnight