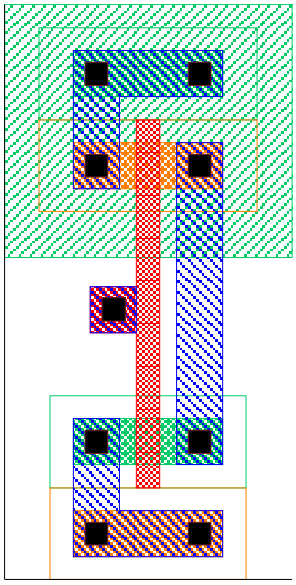
1. Consider the following layout for a CMOS inverter:



(a) The bar at the very top is V_{dd}, the one at the bottom is GND.

(b) Try to identify the PMOS and NMOS transistors. (Hint, the PMOS is on top and the NMOS is on bottom, like we draw schematics.)

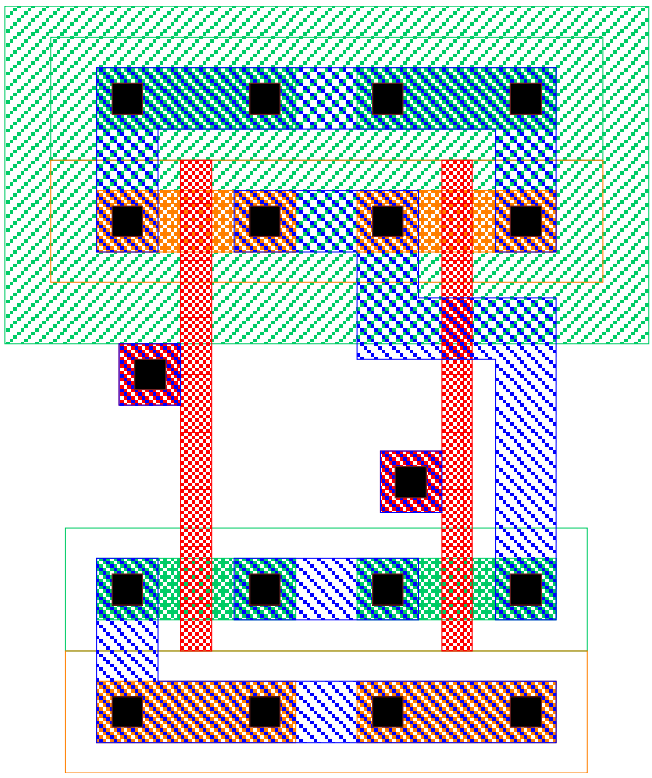
(c) Can you identify how the PMOS and NMOS transistors are connected?

(d) Where is the output?

(e) Where is the input?

This exercise is more "inclass" than "preclass". This is probably too foreign for you to do at the beginning of lecture (but maybe the questions about the structure on the previous page will help), but by the end of the lecture you should be able to do this.

2. Consider the following layout:



(a) How many PMOS transistors?

(b) How many NMOS transistors?

(c) How are the PMOS and NMOS transistors connected?

PMOS

NMOS

(d) How is the output connected to the transistors?

(e) How are the inputs connected?

(f) What function does this circuit perform?