Ideal scaling:

L	1/S
W	1/S
t_{OX}	1/S
N_A	S
V	1/S

1. What is the scale factor, $1/S$, between a 32nm process and a 22nm process?

2. Under ideal scaling, how do the following characteristics scale?
(get started on what you can; we will complete together during lecture)

Area	
Capacitance, C_{ox}	
Capacitance, C_g	
Resistance	
V_{th}	1/S (given)
Current (I_{ds})	
Gate Delay (τ_{gd})	
Wire Delay	
Power [same freq]	
Power [scale freq $1/\tau_{td}$]	
Power Density (P/A) [same freq (f)]	
Power Density (P/A) [scale freq $1/\tau_{td}$]	

Note: Dynamic power in CMOS is capacitive charging: $P \propto CV^2f$
(we will address on future lectures)

3. Assuming V_{dd}=10V in a 10μm process and V_{dd}=1V in a 100nm process: (assume everything else scales according to ideal scaling.)

- What is the voltage scaled by (U)?
- What is the feature size scaled by (S)?
- How much faster are the gates than ideal scaling?
- Assuming you can exploit this gate speedup to increase frequency of operation, how does power density scale?