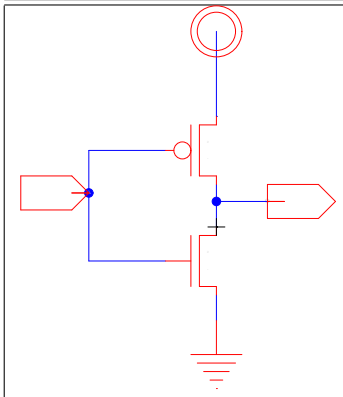
Let:

- R_0 – equivalent resistance of minimum size ($W = L = 1$) NMOS transistor
- I_0 – equivalent current of minimum size ($W = L = 1$) NMOS transistor
- C_0 – gate capacitance of minimum size transistor
- $\tau = R_0 C_0$ – technology-specific delay unit (maybe more accurate today $\tau = C_0/I_0$)

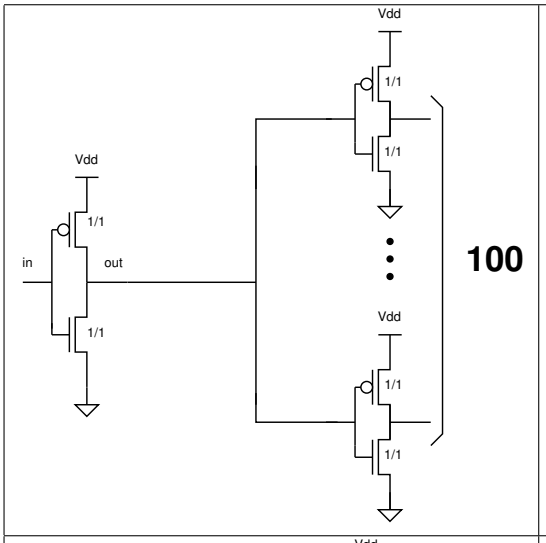
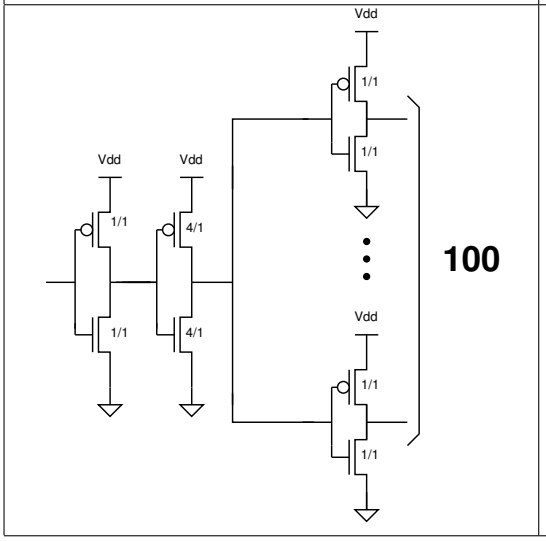
1. What are I_{ds}, R, and C in terms of I_0, R_0, and C_0 for a transistor with width W:

R_{drive}	
I_{drive}	
C_{gate}	

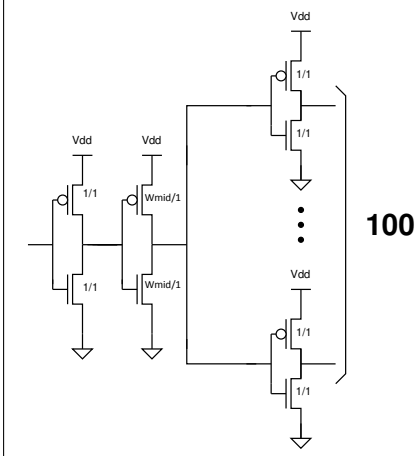
2. How size for equal rise/fall times assuming μ_n=500 cm$^2/(V \cdot s)$ and μ_p=200 cm$^2/(V \cdot s)$, velocity saturated, and $|V_{T_p}| = |V_{T_n}|$ and targeting $R_{drive} = \frac{R_0}{2}$.

	W_p	W_n	C_{in} in multiples of C_0
			

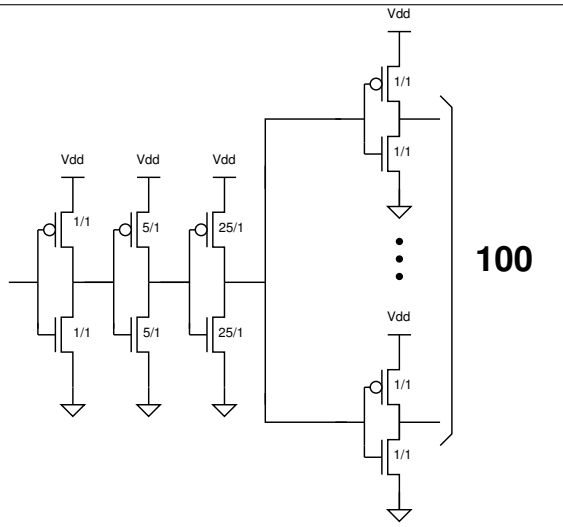
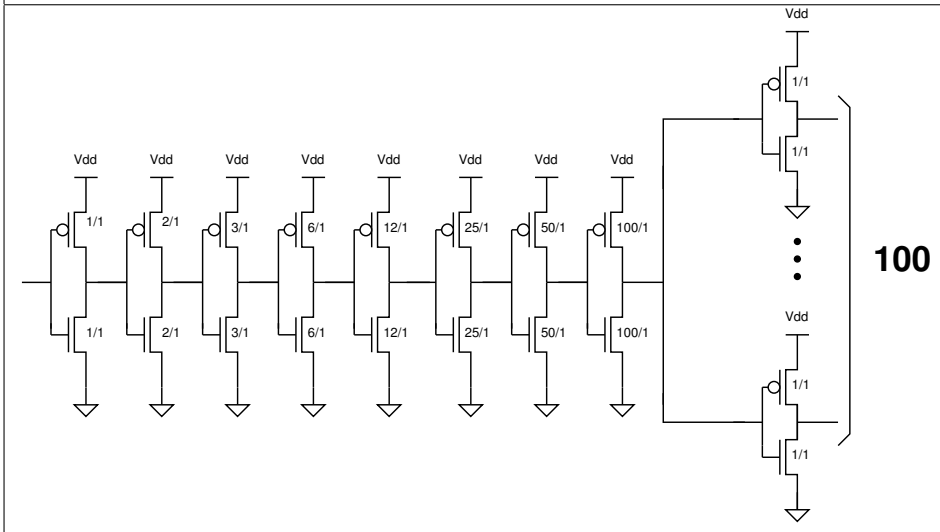
3. What is the delay in τ units?

	Delay
	
	

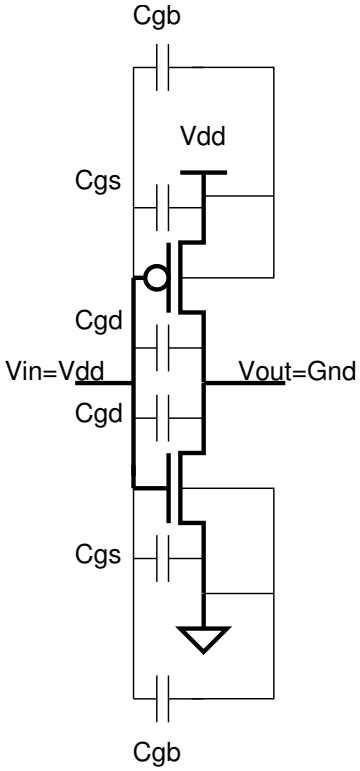
4. How should we size the transistors in middle stage?

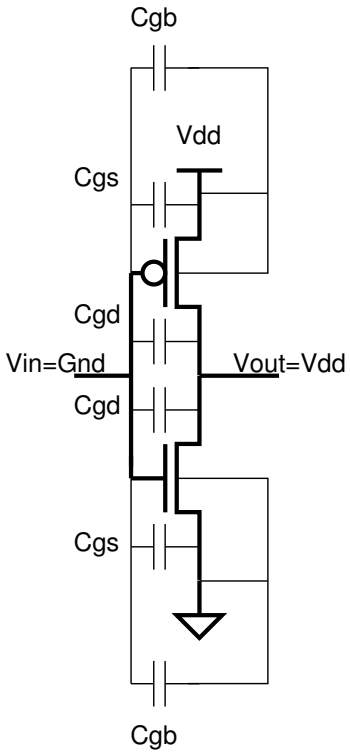
	W_p	W_n	Delay in τ
			

5. What is the delay in τ units?

	Delay
	
	

6. Identify charges and capacitances:





(a) What is charge, Q, on each of the capacitors when Vin=Vdd and Vin=Gnd? Pay carefull attention to polarities. (Qab = - Qba)

	PMOS			NMOS		
Vin	Cgd	Cgb	Cgs	Cgd	Cgb	Cgs
Vdd						
Gnd						

(b) What is the total Δ Q on each C_{gd} when Vin switches from Vdd to Gnd? (and vice versa)

(c) Assuming ΔV=V_{dd}, what is the equivalent capacitance switched?