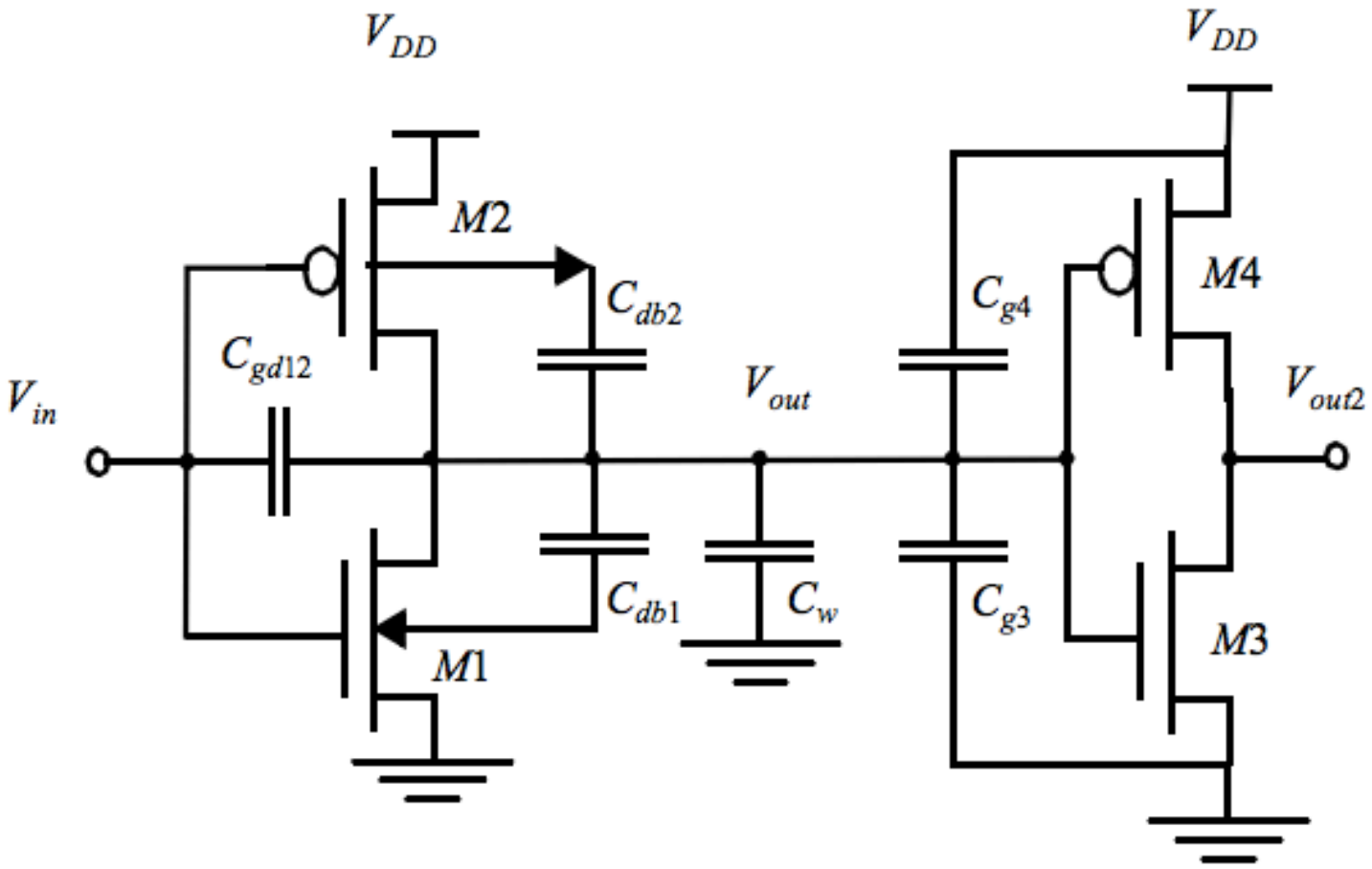
ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

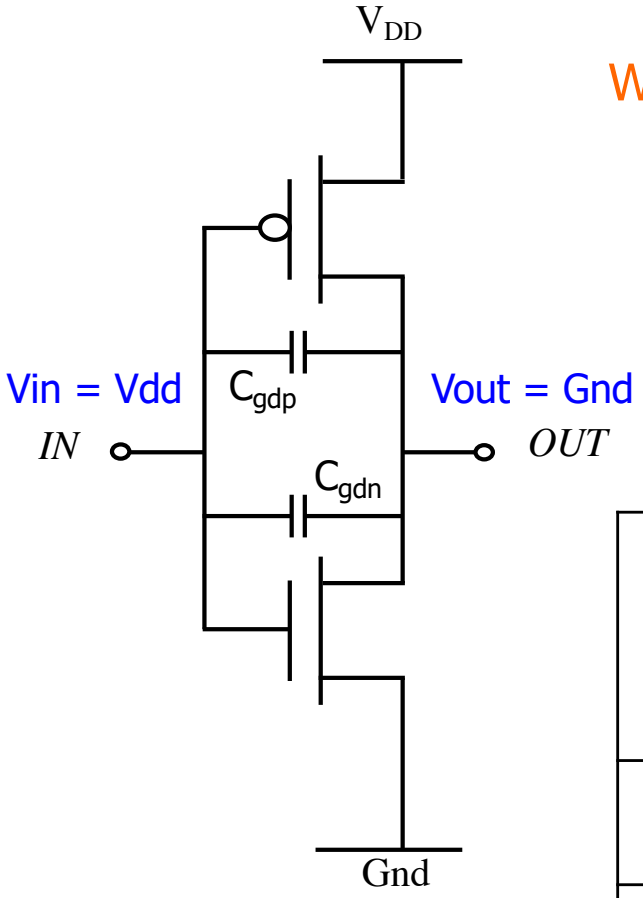
Lec 14: October 8, 2021

Performance: Gates

Capacitance Reminder



Charge on Capacitors (preclass 6)

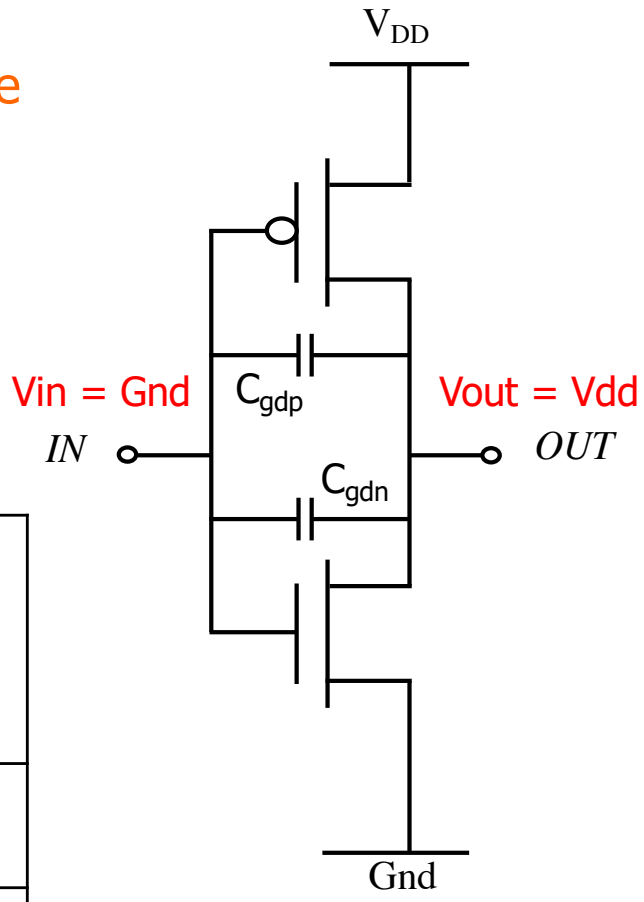


What is charge, Q, on each of the capacitors when Vin=Vdd and Vin=Gnd?

Vin	**PMOS** C_{gdp}	**NMOS** C_{gdn}
Vdd		
Gnd		

Charge on Capacitors (preclass 6)

What is charge, Q, on each of the capacitors when Vin=Vdd and Vin=Gnd?



Vin	PMOS C_{gdp}	NMOS C_{gdn}
Vdd		
Gnd		

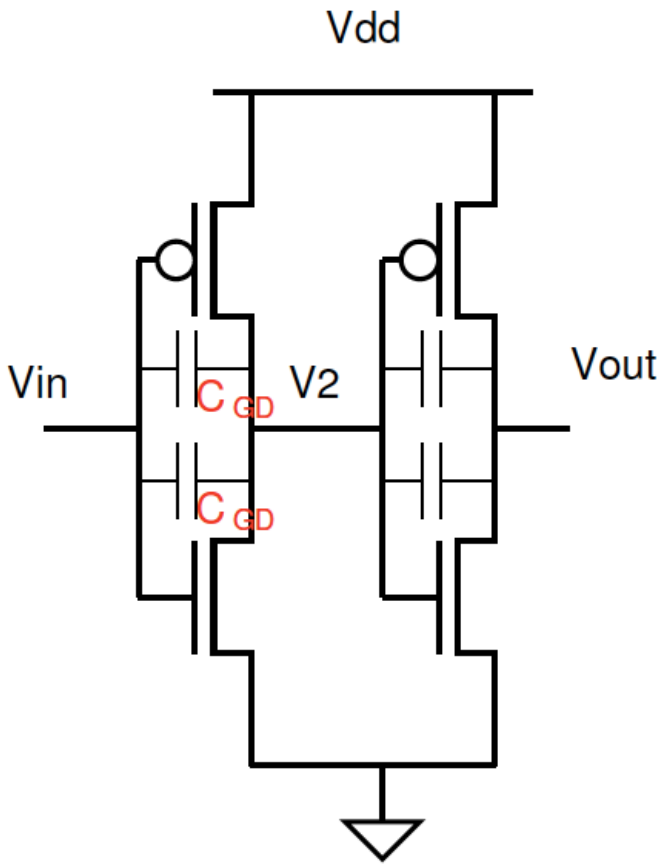
Questions

- What is ΔQ on each C_{gd} when input switched?
- Assuming $\Delta V = Vdd$, what is equivalent capacitance?

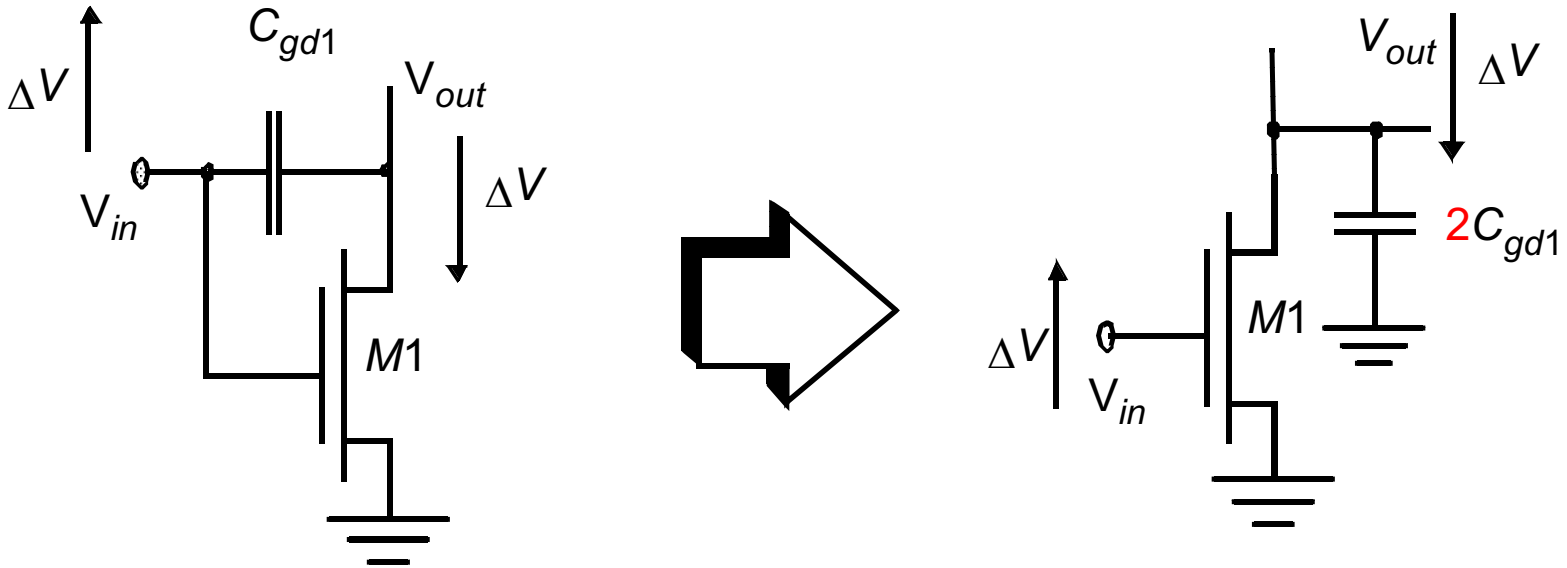
Vin	**PMOS** C_{gdp}	**NMOS** C_{gdn}
Vdd		
Gnd		

Miller Effect For an Inverter

- Feedback capacitance (C_{gd}) between input and output must swing 2 V_{dd}
- Or…behaves same as a double-sized capacitor on the output



Miller Effect For an Inverter



"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

Previously: First Order Delay

- R_0 = Resistance of minimum size NMOS device
- $I_0 = I_{ds}$ of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- $R_{drive} = R_0/W_n$ $I_{drive} = W_n I_0$ $C_g = W_n C_0$
- Technology independent relative delay

$$\tau = R_0 C_0 = C_0/I_0$$

- Large fanout results in large delays
  - Drive in stages to reduce delay

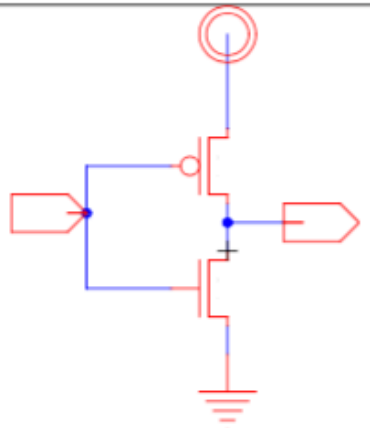
Today

- Delay in Gates
- Data Dependent Delay
- Large Fanin

- Analyze everything for two cases:
  - Ratio to minimize average delay: $R_{p0} = 2R_{n0} = 2R_0$
  - Extreme velocity saturation: $R_{p0} = R_{n0} = R_0$
    - Simplified case from Monday in analyzing fanout delays

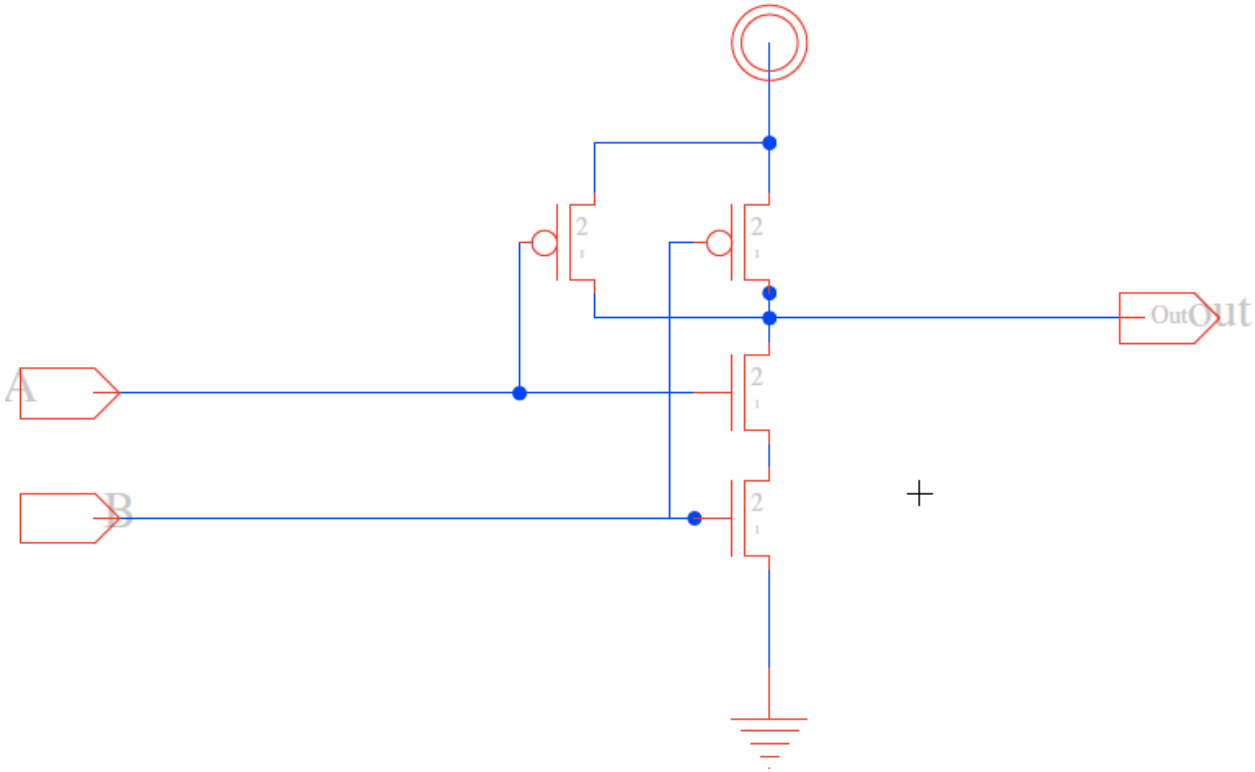
Inverter Performance (preclass 1, row 1)

- Sized for $R_0/2$ drive resistance, (R_0=R_{n0})

	$R_{p0} = R_{n0}$			$R_{p0} = 2R_{n0}$		
	W_p	W_n	C_a	W_p	W_n	C_a
	2	2	$4C_0$	4	2	$6C_0$

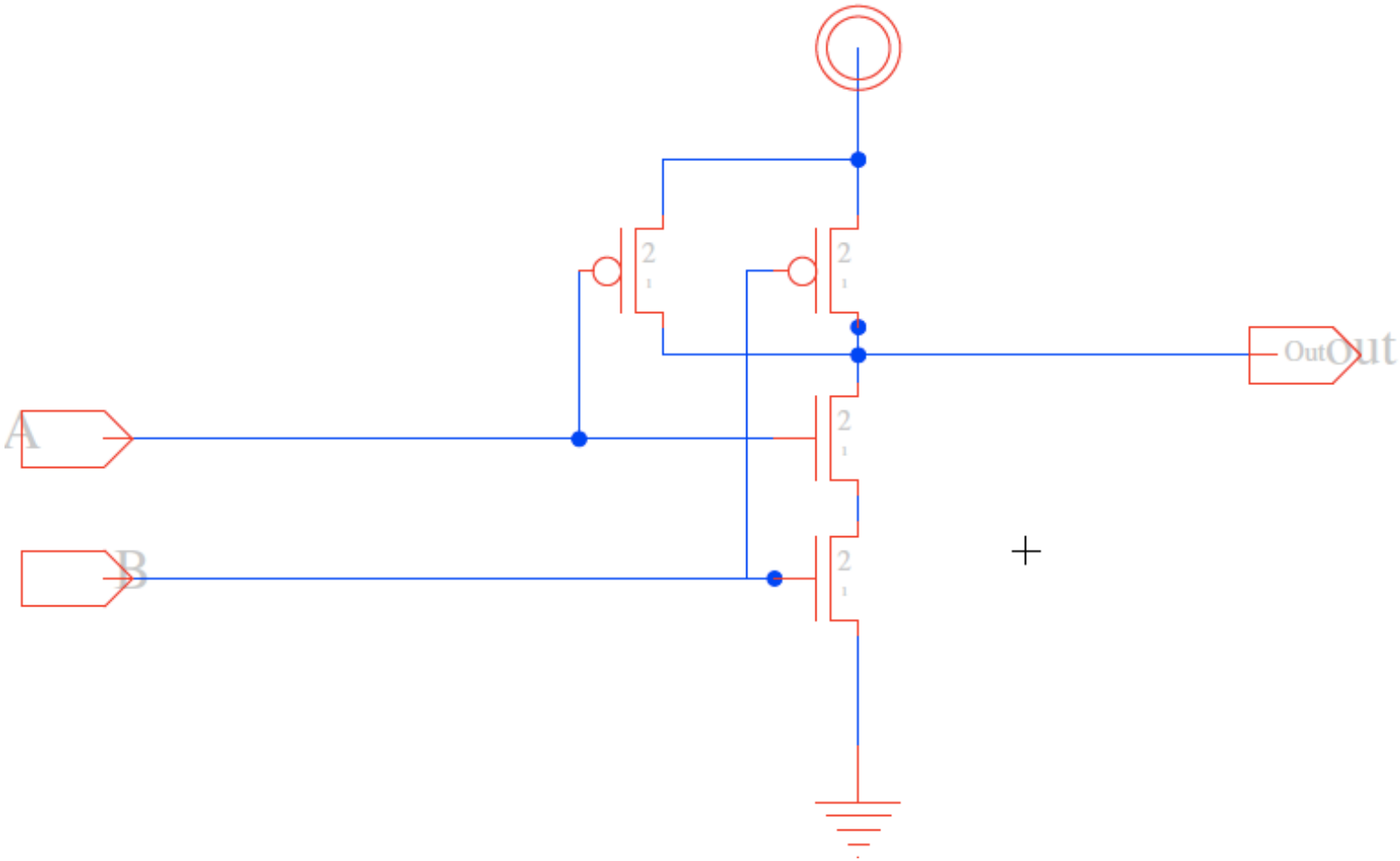
Data Dependent Delay

- Drive resistance depends on input values
  - Delay depends on input data
  - Analyze using worst case delay



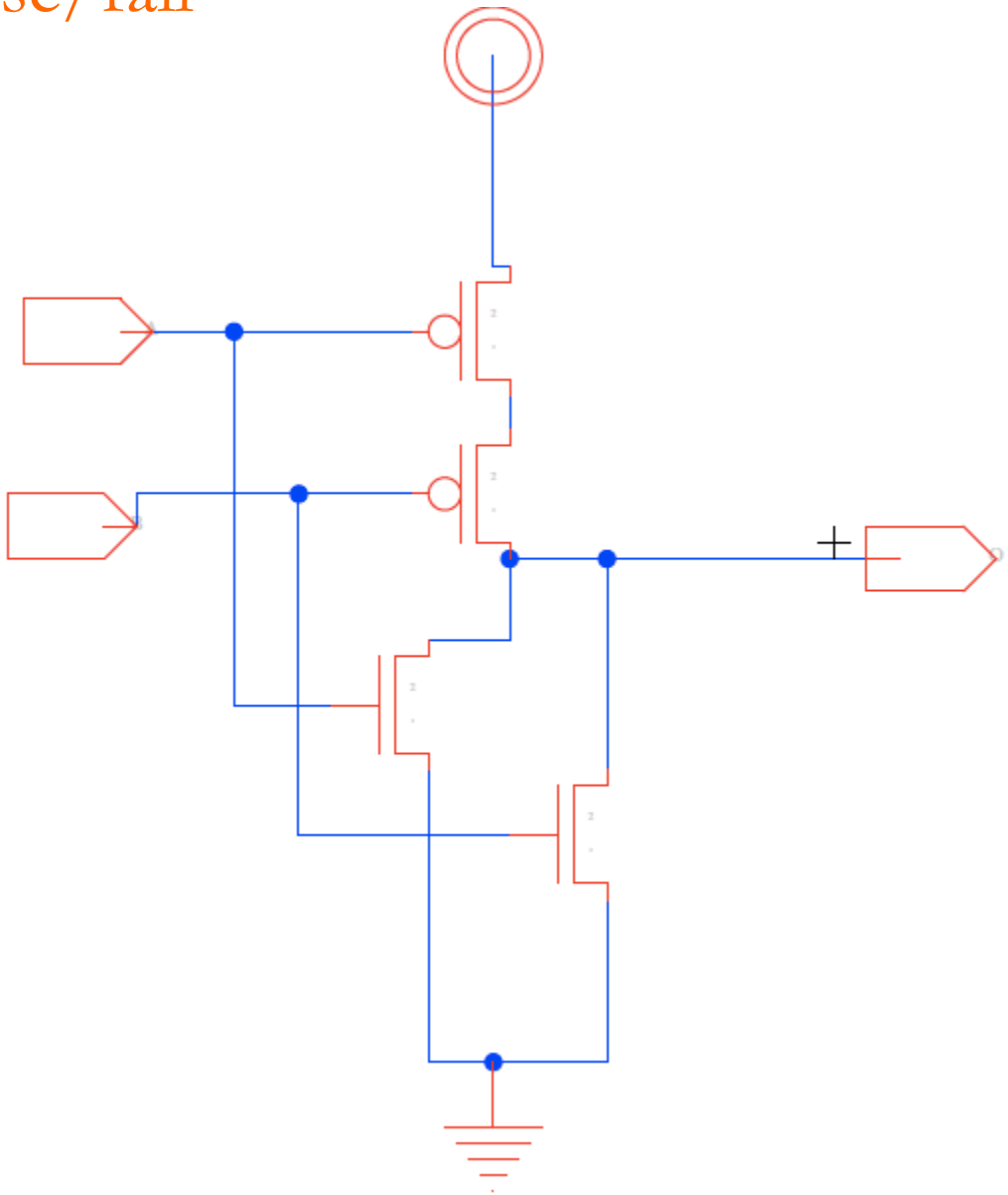
Transistor Sizing (preclass 1, row 2)

- How should we size to equalize worst-case rise/fall times for $R_{drive}=R_0/2$?



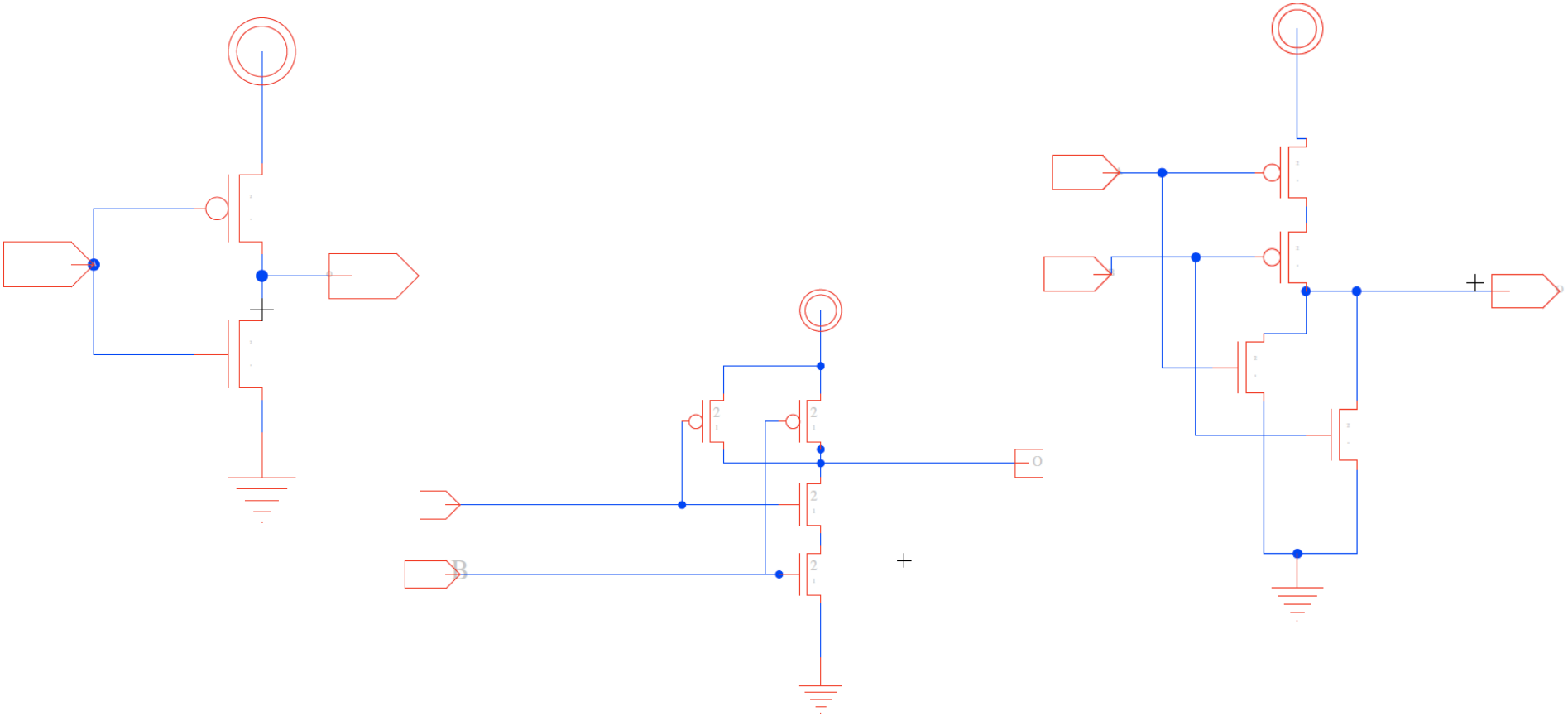
Transistor Sizing (preclass 1, row 3)

- How size for equal rise/fall for $R_{drive}=R_0/2$?



Input Load

- Input capacitance per input in each case?

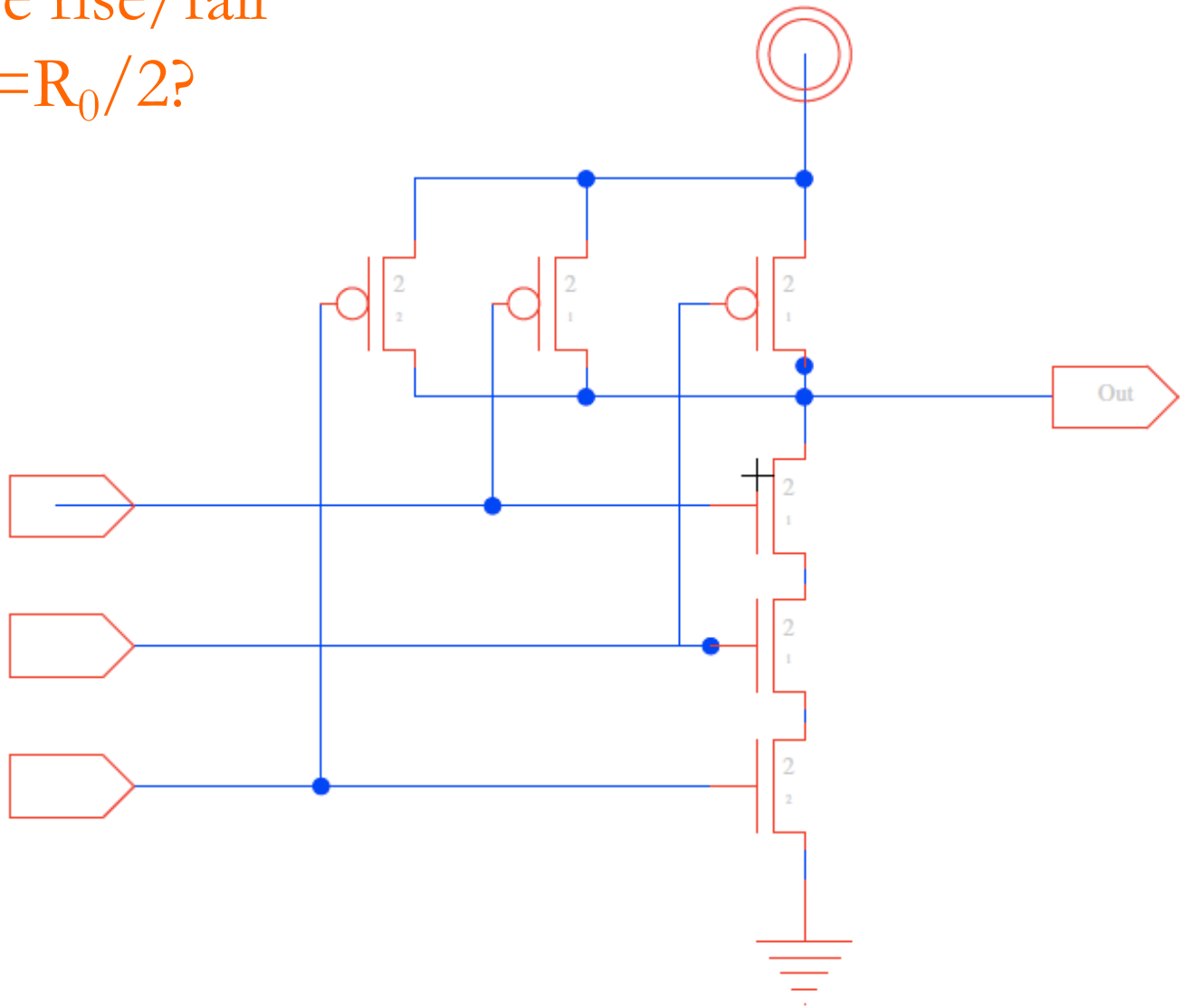


Observe

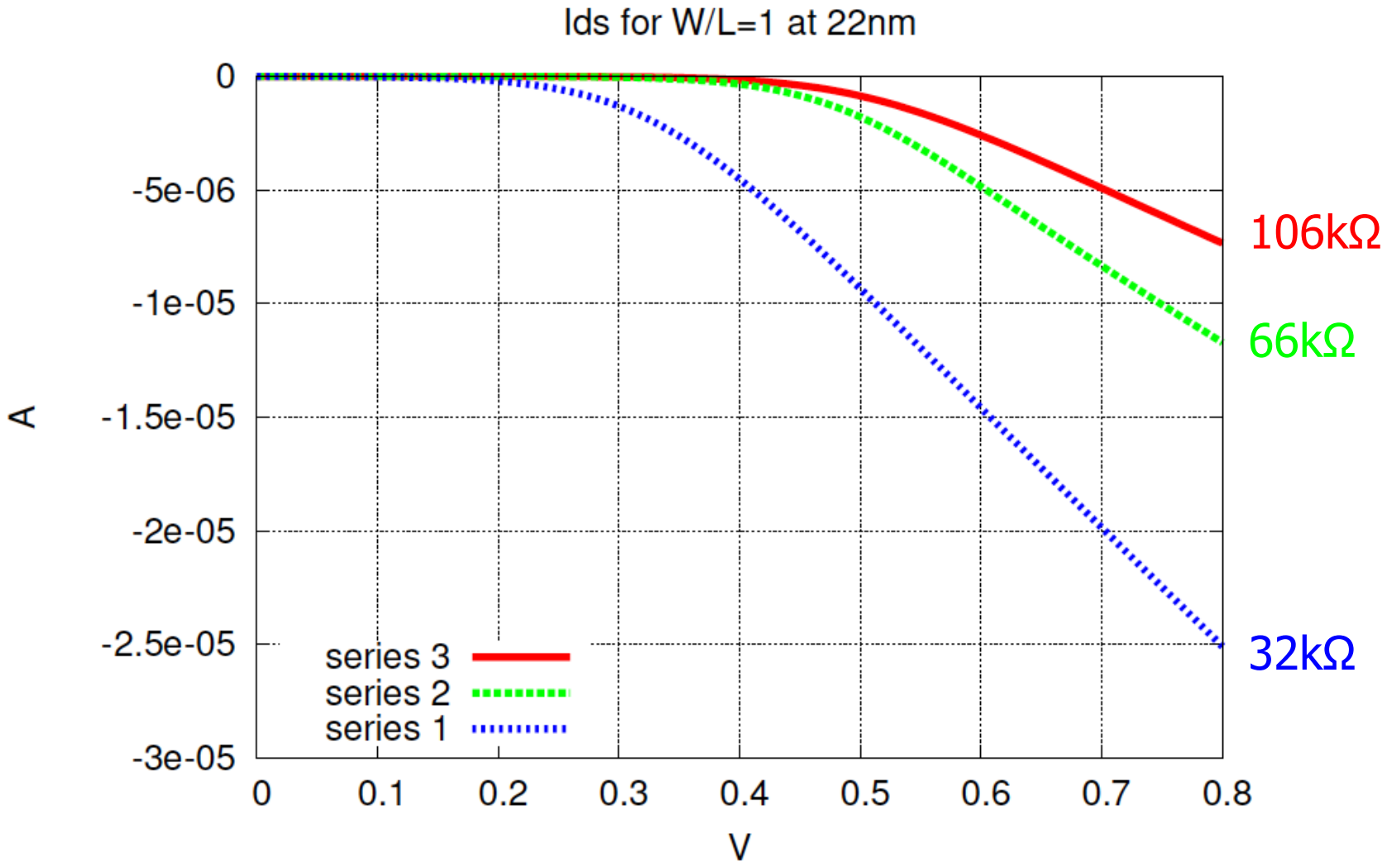
- Ratio of Input Load Capacitance to Output Drive Strength: C_{InLoad}/I_{ds}
  - Differs with gate function
  - Gate efficiency

Transistor Sizing (preclass 1, row 4)

- Size equalize rise/fall times $R_{drive}=R_0/2$?



Series Transistors



Increasing Fanin (preclass 2)

- What happens to input capacitance as fanin (k) increases
  - Keeping output drive the same
    - E.g. $R_{drive}=R_0/2$
- k-input nand gate has what input capacitance?

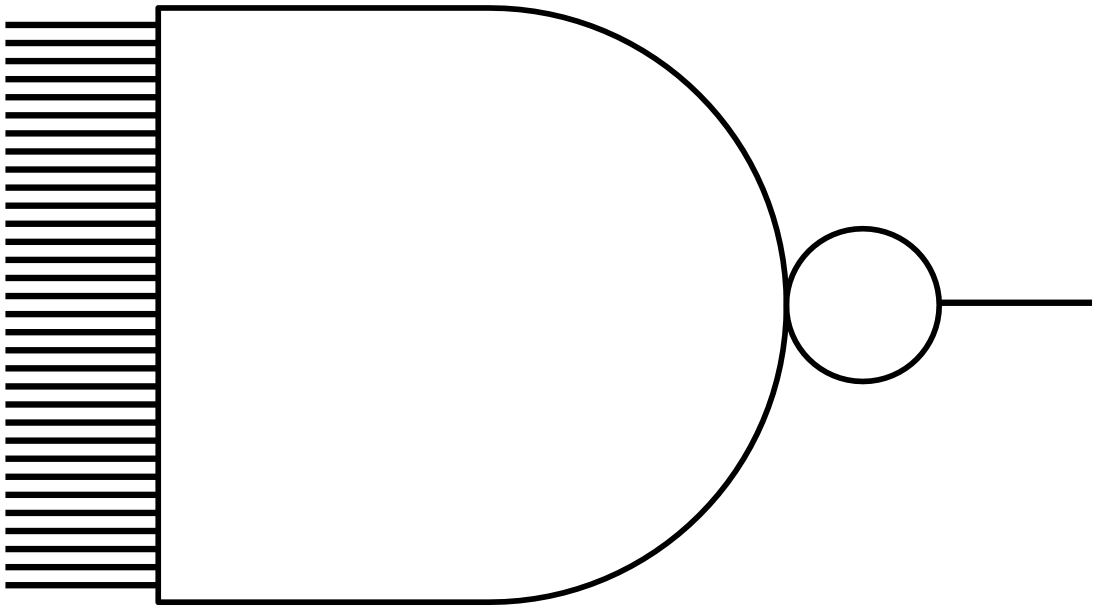
Fanin

- **Conclude:** gates slow down with fanin
  - Less drive per input capacitance
  - C_{InLoad}/I_{ds} increases

nand32 (preclass 3, row 1)

- single-stage nand32
  - Delay with $R_0/2$ input drive and $4C_0$ load?

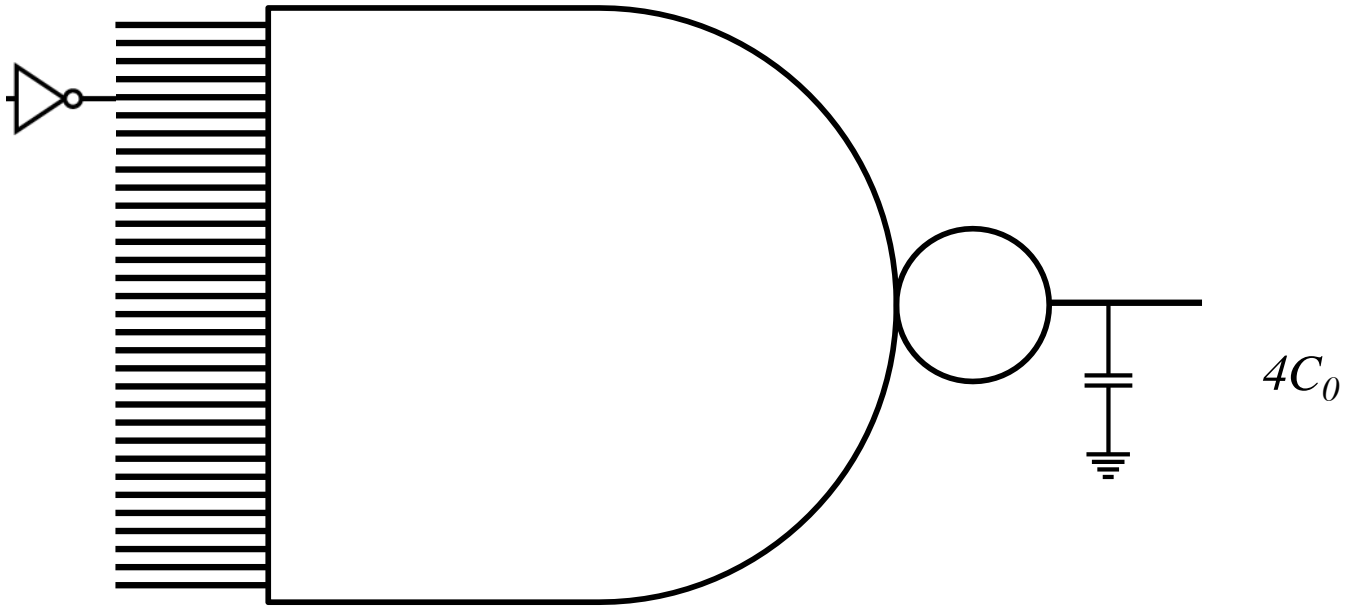
$R_{n0}=R_{p0}$ case only



nand32 (preclass 3, row 1)

- nand32
  - Delay with $R_0/2$ input drive and $4C_0$ load?

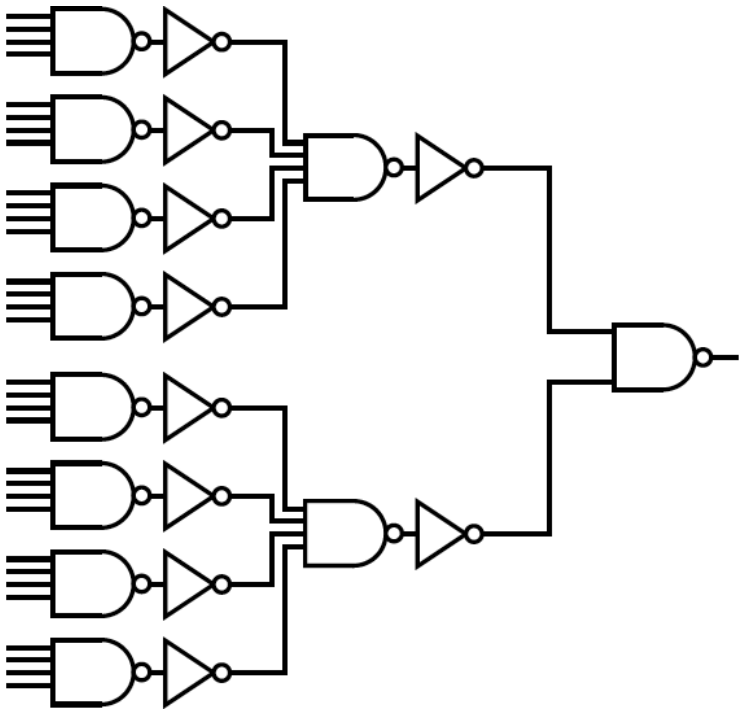
$R_{n0}=R_{p0}$ case only



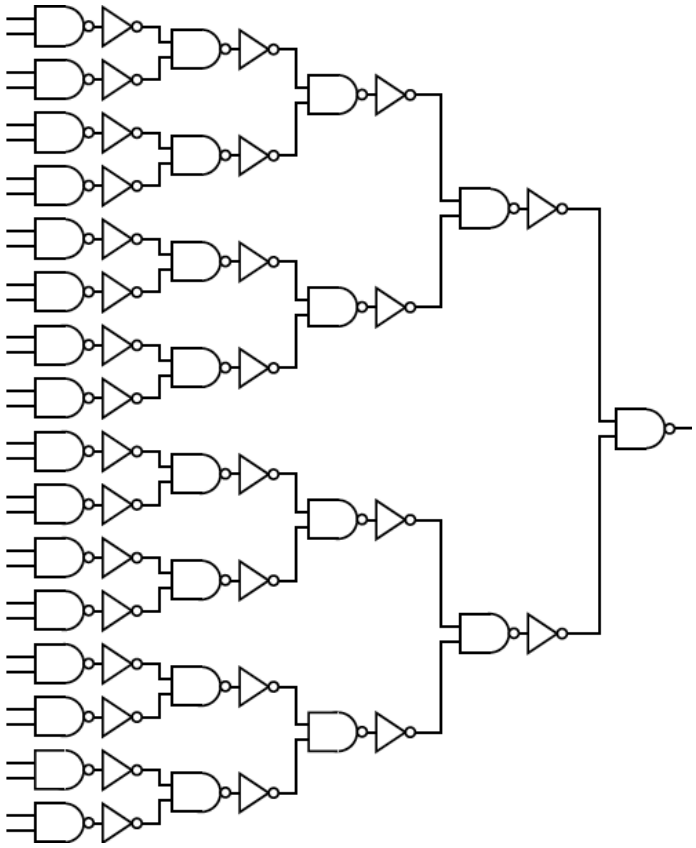
Which is Faster? (preclass 3, rows 2&3)

- nand32

$R_{n0}=R_{p0}$ case only



nand4-inv-nand4-inv-nand2

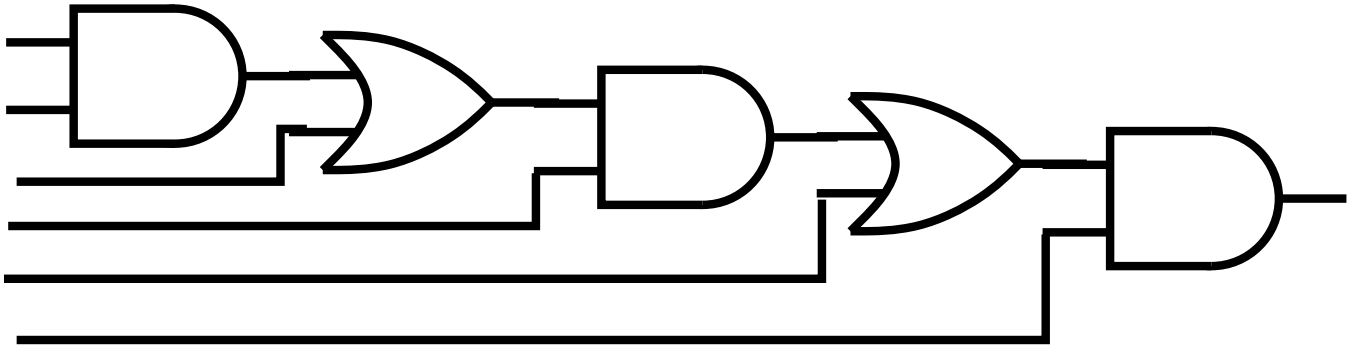


$(\text{nand2-inv})^4\text{-nand2}$

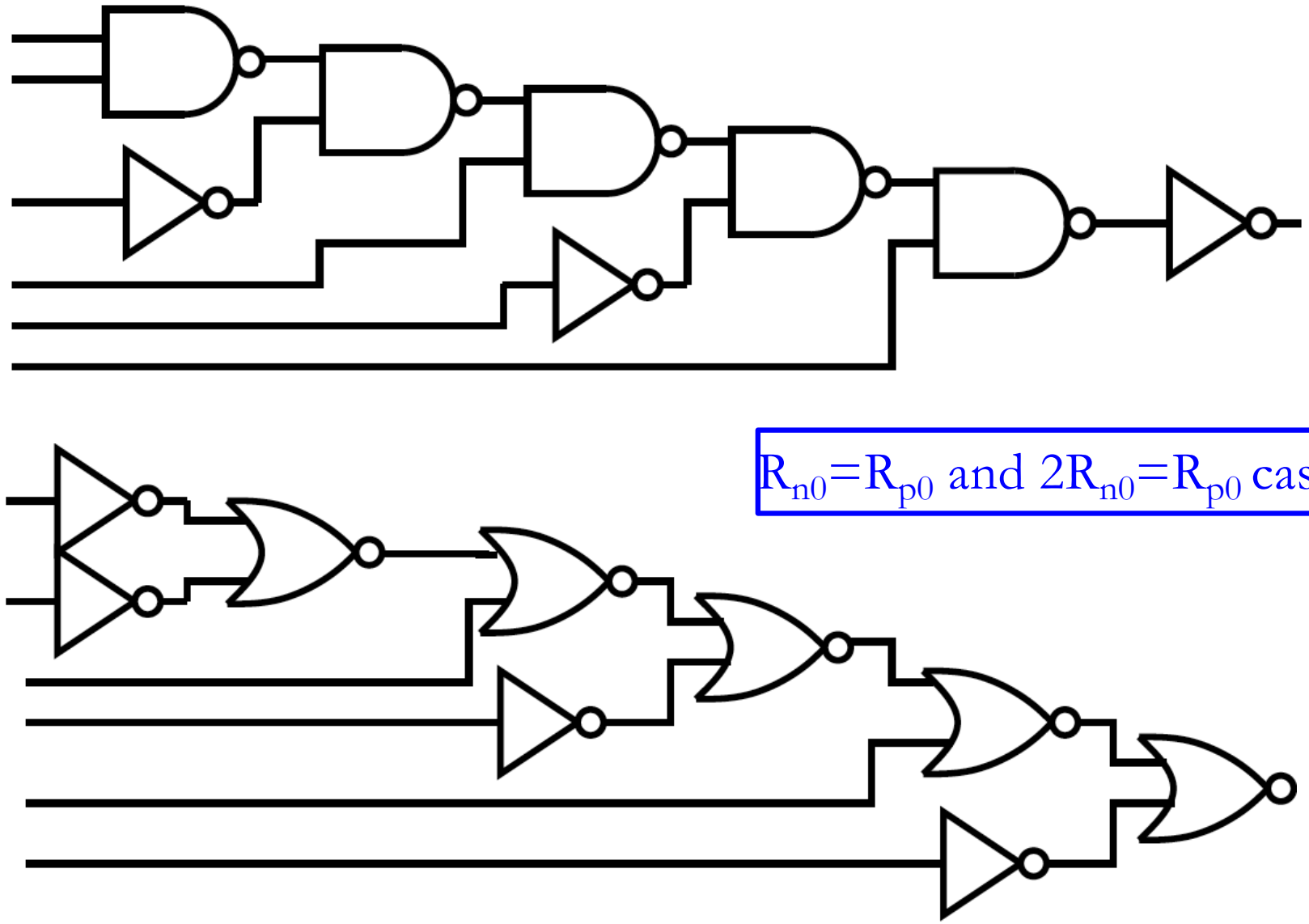
Lesson

- Large gates are slow / inefficient
  - High capacitive load / drive current
- Small gates can be inefficient
  - Need many stages
- Staging over moderate size gates minimizes delay
- Exact size will be technology dependent

And-Or Chain



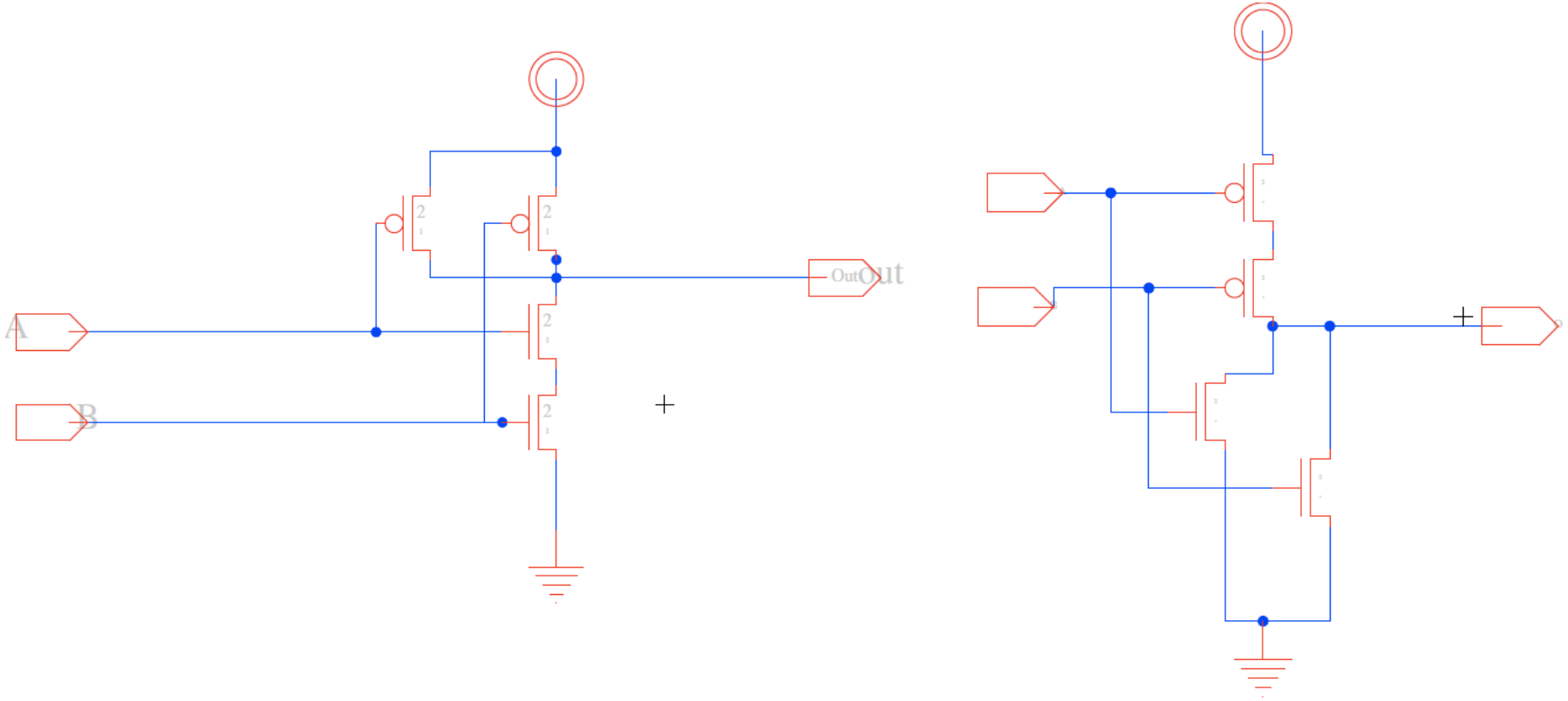
Delay of each implementation? (preclass 4)



$R_{n0}=R_{p0}$ and $2R_{n0}=R_{p0}$ cases

Take Away?

- nor vs. nand



Ideas

- First order reason in $\tau = R_0C_0$ units
- Gates have different efficiencies
  - Drive strength per unit input capacitance
- Without velocity saturation
  - Reason to prefer nand over nor
- With velocity saturation
  - nands and nors are similar efficiency
- Large fanin and fanout slow gates
  - Decompose into stages
  - …but not too many

Admin

- HW 4
  - Due tonight at midnight
- HW 5 out now
  - Is long and will take time, start today
  - Due during fall break 10/15