

ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 16: October 13, 2021
Energy and Power Tradeoffs



Previously

- Three components of power
 - Static
 - Dynamic
 - Short circuit
- $P_{\text{tot}} = P_{\text{static}} + P_{\text{dyn}} + P_{\text{sc}}$

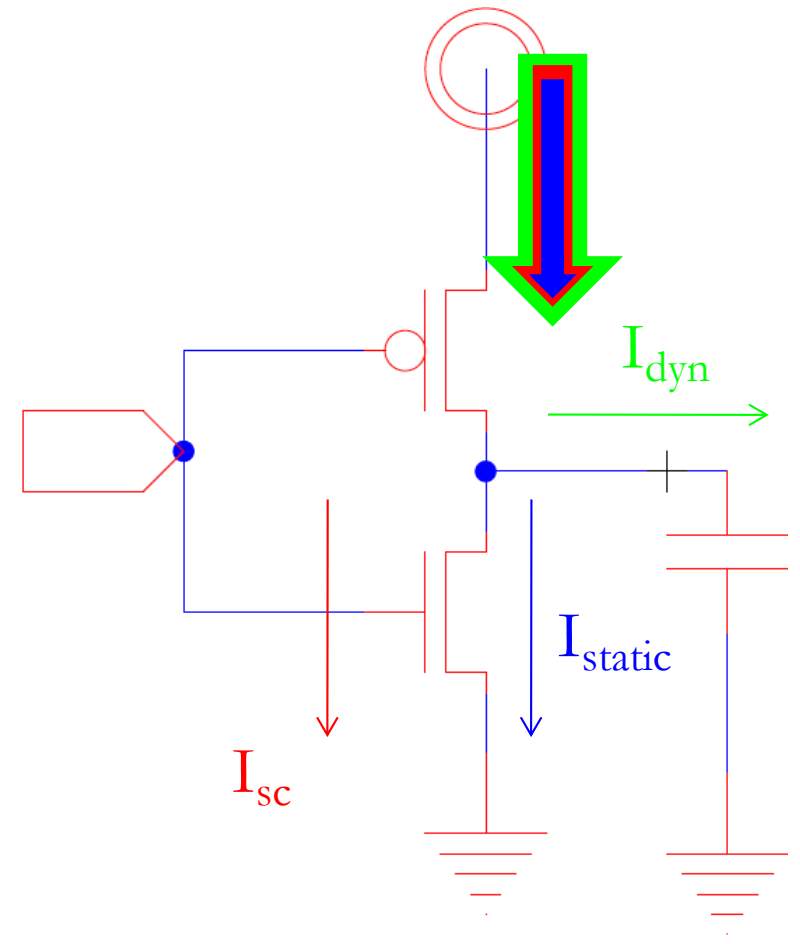
Switching

Dynamic Power

Switching Currents

□ $I_{total}(t) = I_{static}(t) + I_{switch}(t)$

□ $I_{switch}(t) = I_{sc}(t) + I_{dyn}(t)$

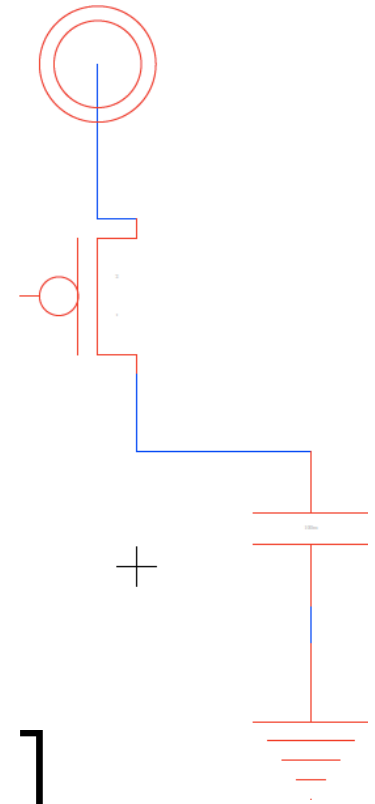


Charging

□ $I_{dyn}(t)$ – why is it changing?

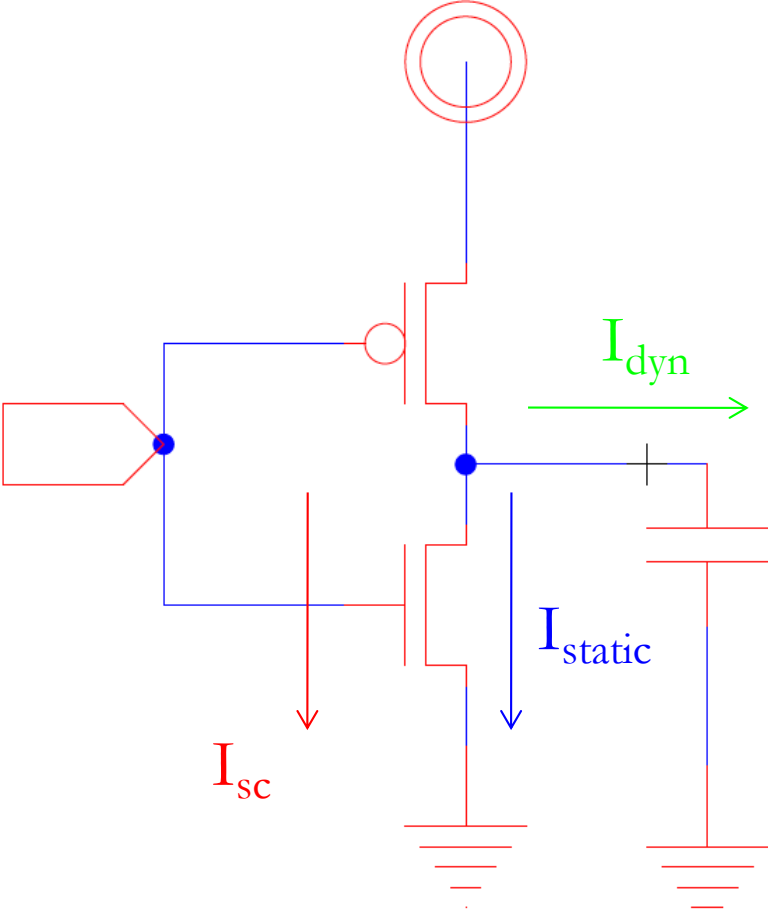
- $I_{ds} = f(V_{ds}, V_{gs})$
- and V_{gs}, V_{ds} changing

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$
$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L} \right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$





Switching Energy – focus on $I_{dyn}(t)$



Switching (Dynamic)

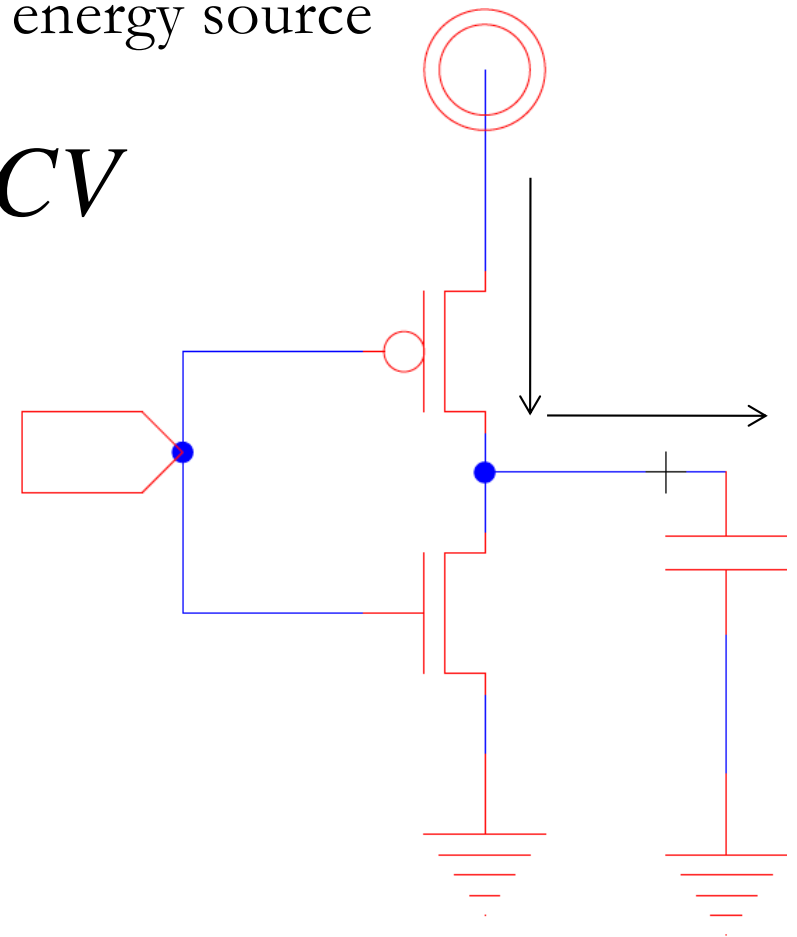
- ❑ CMOS circuit switching output from 0→1
 - Spends energy CV_{dd}^2 charging load
 - CV_{dd}^2 energy is pulled from the energy source

$$Q = \int I(t) dt = CV$$

$$E = \int P(t) dt$$

$$E = V_{dd} \int I(t) dt$$

$$E = CV_{dd}^2$$





Switching Power

- Every time output switches $0 \rightarrow 1$ pay:
 - $E = CV^2$

- $P_{\text{dyn}} = (\# 0 \rightarrow 1 \text{ trans}) \times CV^2 / \text{time}$



Charging Power

- $P_{\text{dyn}} = (\#0 \rightarrow 1 \text{ trans}) \times CV^2 / \text{time}$

- Often like to think about switching frequency
- Useful to consider per clock cycle
 - Frequency $f = 1/\text{clock-period} = \text{clock-cycles}/\text{time}$

- $P_{\text{dyn}} = (\#0 \rightarrow 1 \text{ trans}/\text{clock-cycle}) CV^2 f$

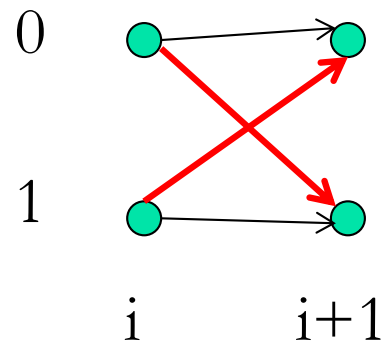


Data Dependent Activity

- Consider an 8b counter
 - How often do each of the following switch?
 - Low bit?
 - High bit?
- Assuming random inputs
 - Activity at output of nand2?
 - Activity at output of xor2?

Gate Output Switching (random inputs)

Output states



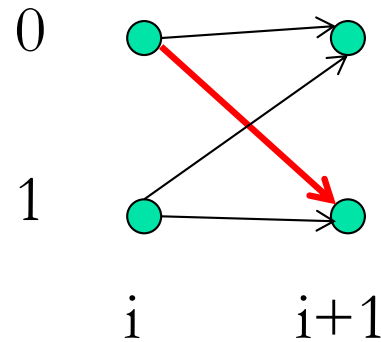
$$P(\text{out}_i \neq \text{out}_{i+1}) = P(\text{out}_i = 0) * P(\text{out}_{i+1} = 1) + P(\text{out}_i = 1) * P(\text{out}_{i+1} = 0)$$

Probability of output switch of nand2?

Probability of output switch of xor2?

Gate Output Switching (random inputs)

Output states



$$P(\text{out}_i \rightarrow \text{out}_{i+1} = 0 \rightarrow 1) = P(\text{out}_i = 0) * P(\text{out}_{i+1} = 1)$$



Dynamic Power

- $P_{\text{dyn}} = (\#0 \rightarrow 1 \text{ trans/clock-cycle}) CV^2 f$
- Let $a = \text{activity factor}$
 - $a = \text{average } \# \text{tran}_{0 \rightarrow 1} / \text{clock}$
 - $a = \text{probability of } \# \text{tran}_{0 \rightarrow 1}$

- $P_{\text{dyn}} = aCV^2 f$



Activity Factor

- Let a = activity factor
 - a = average #tran_{0→1}/clock
 - a = probability of #tran_{0→1}

$$a = p(out_i = 0)p(out_{i+1} = 1)$$

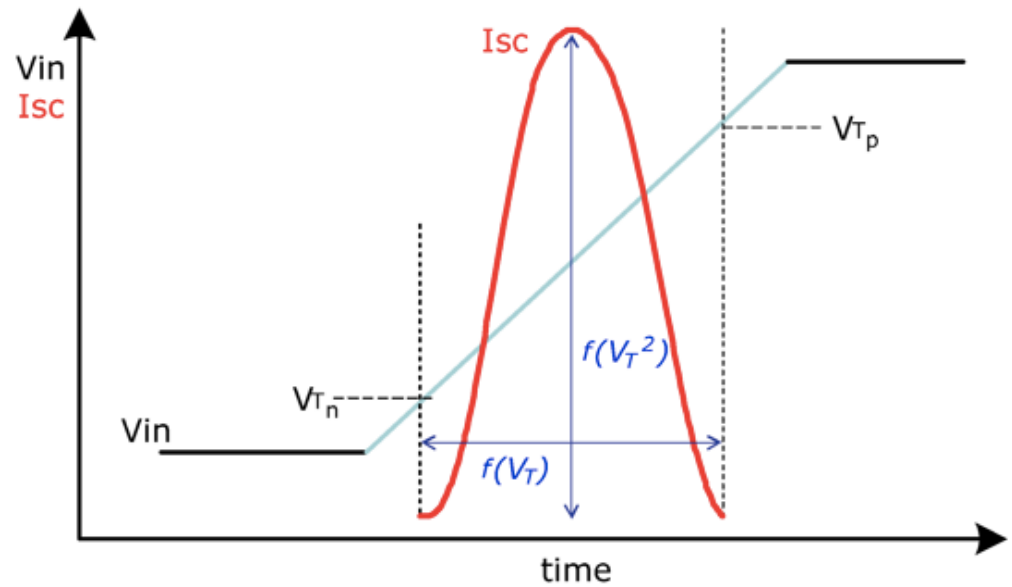
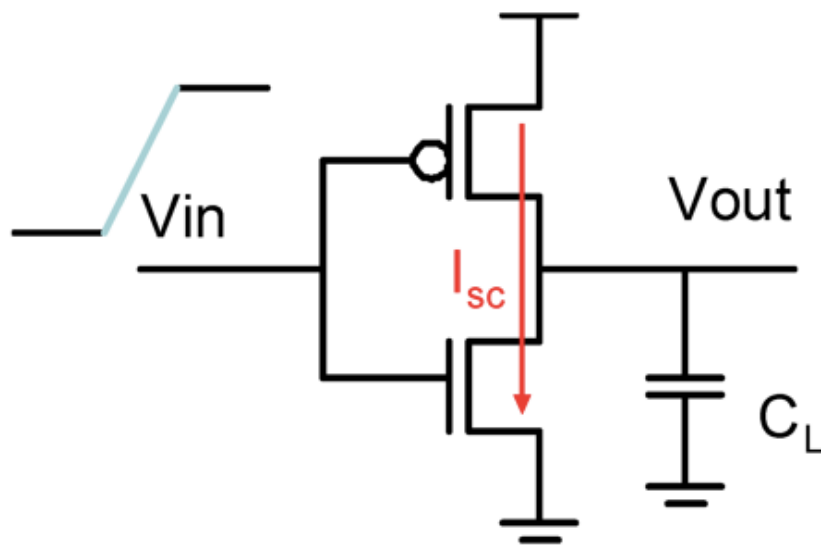
$$a = \frac{N_0}{2^N} \frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Switching

Short Circuit Power

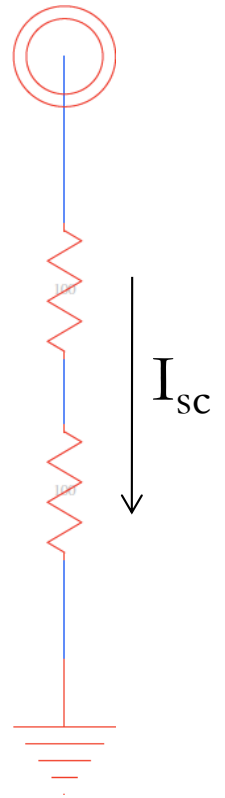
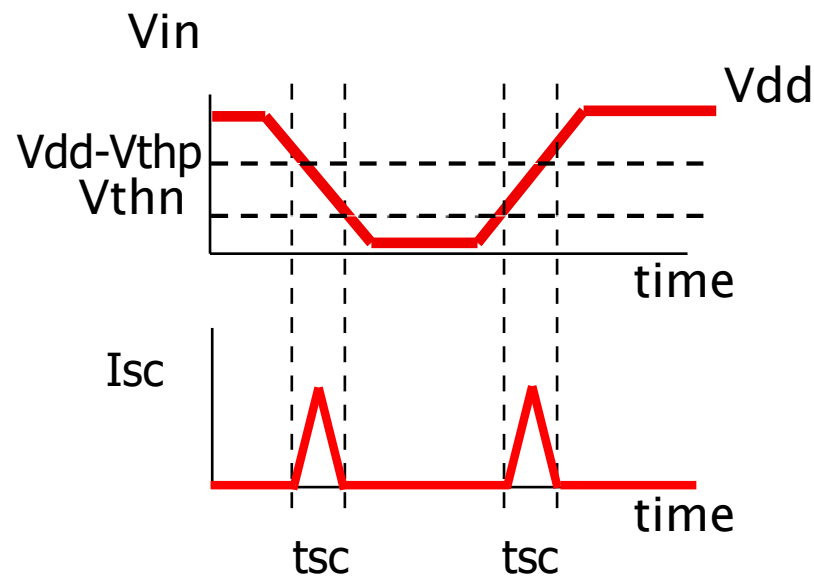
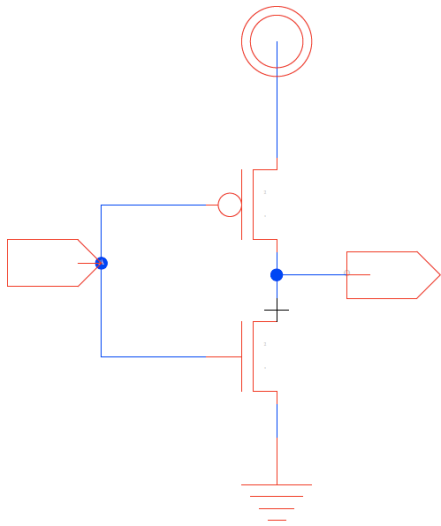
Short Circuit Power

- Between V_{TN} and $V_{dd} - V_{TP}$
 - Both N and P devices conducting



Short Circuit Power

- Between V_{TN} and $V_{dd} - V_{TP}$
 - Both N and P devices conducting
- Roughly:

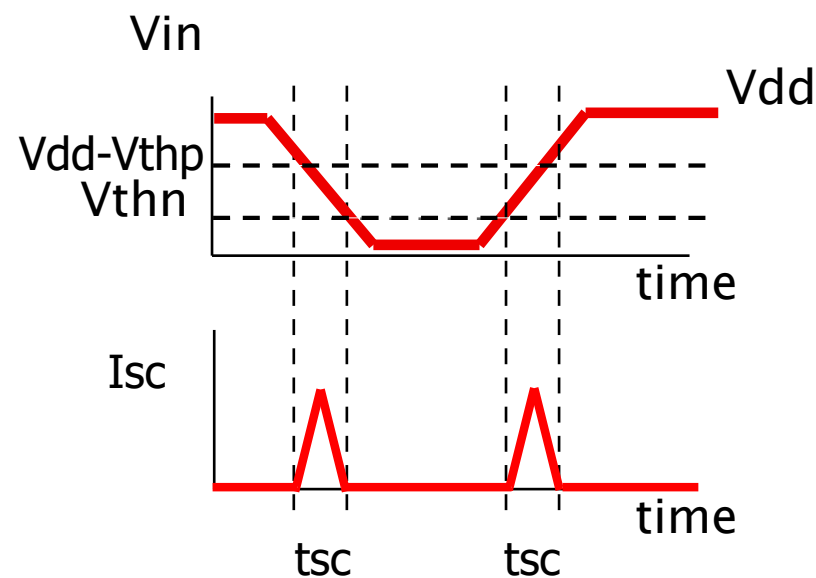
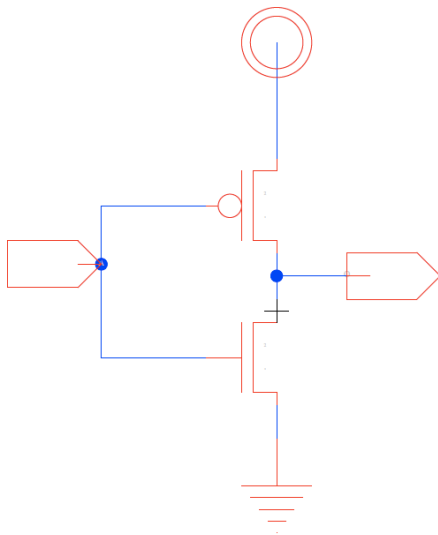




Peak Current

- I_{peak} around $V_{dd}/2$
 - If $|V_{TN}| = |V_{TP}|$ and sized equal rise/fall

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$



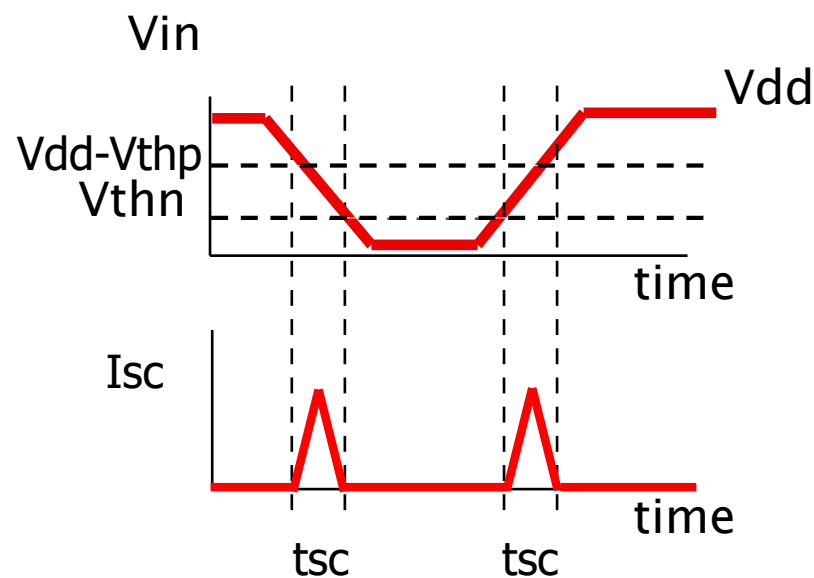
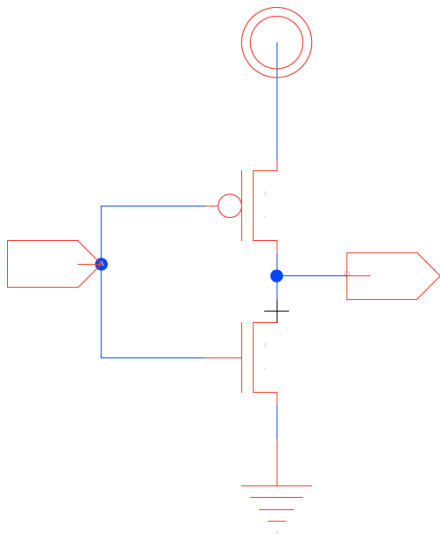
Peak Current

□ I_{peak} around $V_{dd}/2$

■ If $|V_{TN}| = |V_{TP}|$ and sized equal rise/fall

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$\int I(t) dt \approx I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right)$$



Peak Current

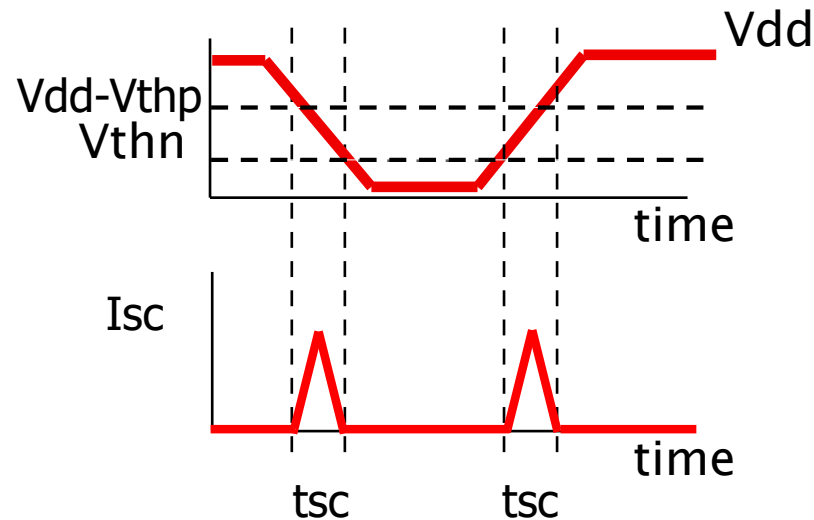
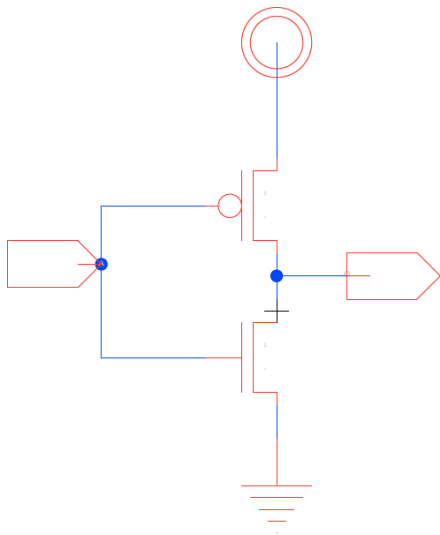
□ I_{peak} around $V_{dd}/2$

■ If $|V_{TN}| = |V_{TP}|$ and sized equal rise/fall

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$\int I(t) dt \approx I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right)$$

$$E_{Vin} = V_{dd} \times I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right)$$





Short Circuit Energy

- Make it look like switching an equivalent capacitance, C_{SC}

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \frac{1}{2} \right)$$

$$E = C_{SC} V_{dd}^2$$

Short Circuit Energy

- Make it look like switching an equivalent capacitance, C_{SC}

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \frac{1}{2} \right)$$

$$E = C_{SC} V_{dd}^2$$

$$C_{SC} = \frac{I_{peak} t_{sc}}{2V_{dd}}$$



Short Circuit Energy

- Every time switch ($0 \rightarrow 1$ and $1 \rightarrow 0$)
 - Also dissipate short-circuit energy: $E = C_{sc}V^2$
 - C_{cs} “fake” capacitance (for accounting)



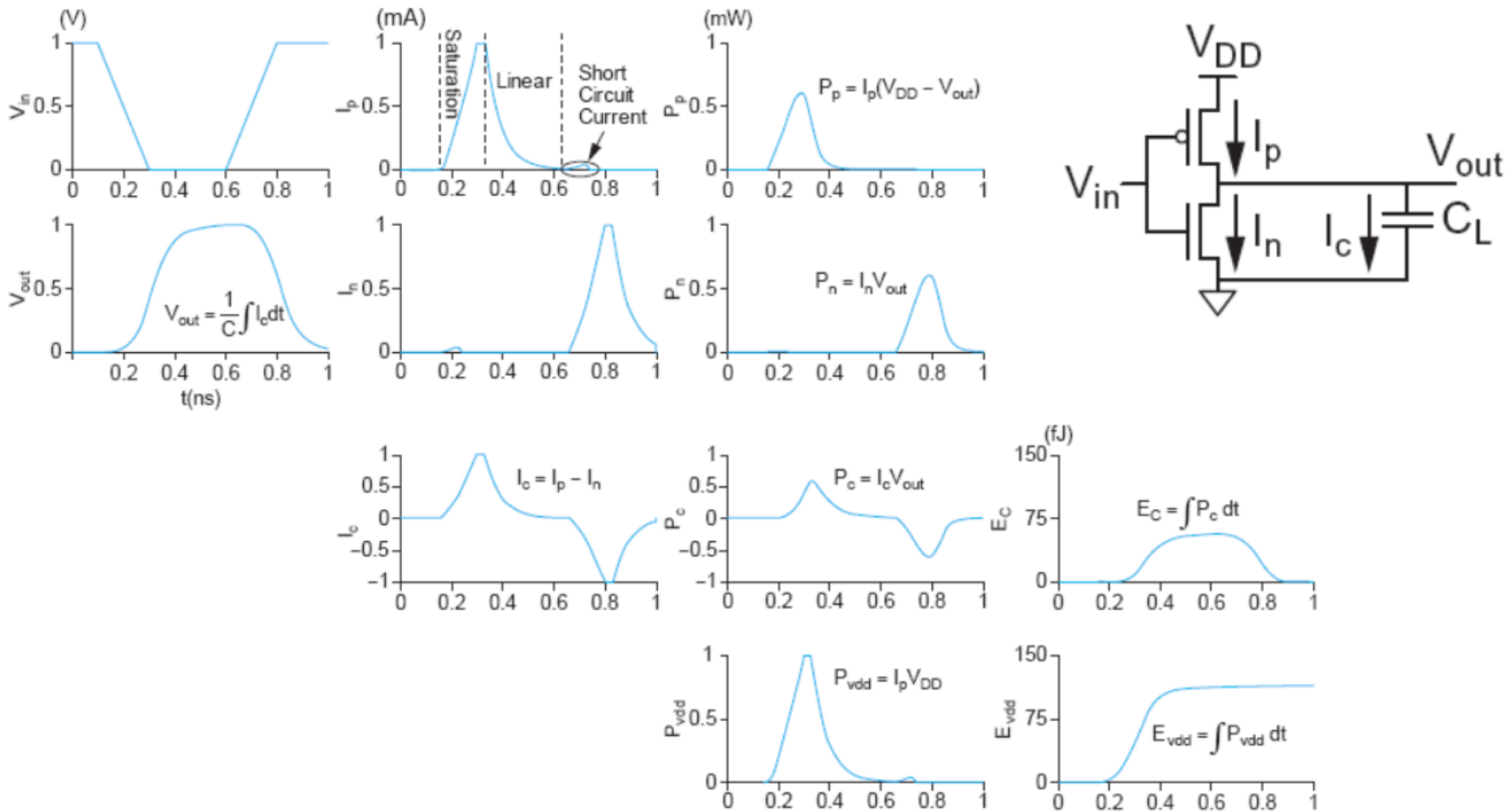
Total Power

$$\square P_{\text{tot}} = P_{\text{static}} + P_{\text{sc}} + P_{\text{dyn}}$$

$$\square P_{\text{dyn}} + P_{\text{sc}} = aC_{\text{load}}V^2f + 2aC_{\text{sc}}V^2f$$

$$\square P_{\text{tot}} \approx a(C_{\text{load}} + 2C_{\text{sc}})V^2f + VI'_s(W/L)e^{-Vt/(nkT/q)}$$

Switching Waveforms

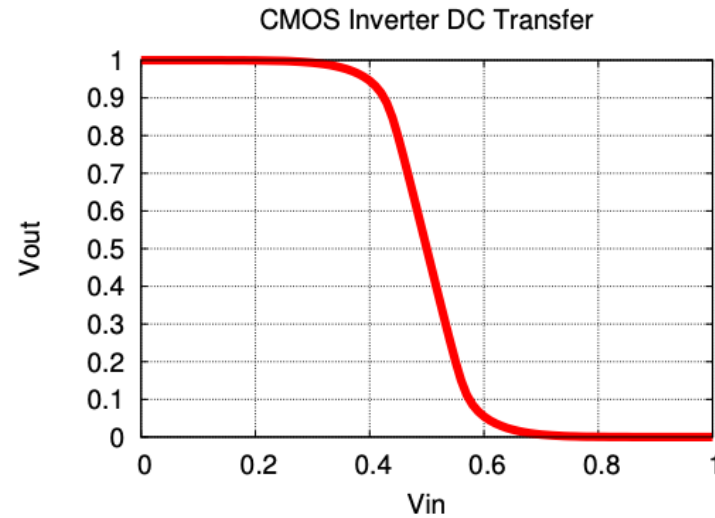
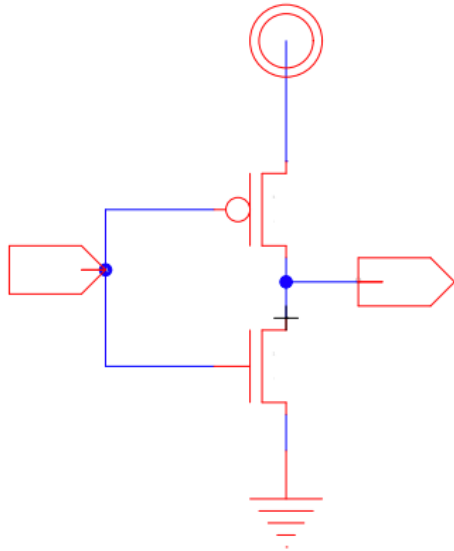




Preclass 1

Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7}) e^{\frac{V_{gs} - V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4} (V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7}) e^{-\left(\frac{V_{gs} - V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4} (V_{gs} - V_{thp})$

Consider an inverter using the pmos and nmos devices described above:





Preclass 1

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V			
140mV			
400mV			
500mV			
600mV			
860mV			
1V			

Design Tradeoffs



Reduce Dynamic Power?

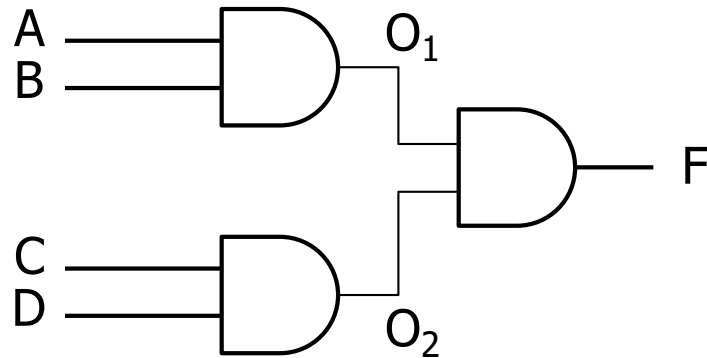
- $P_{\text{dyn}} = aCV^2 f$

- How do we reduce dynamic power?

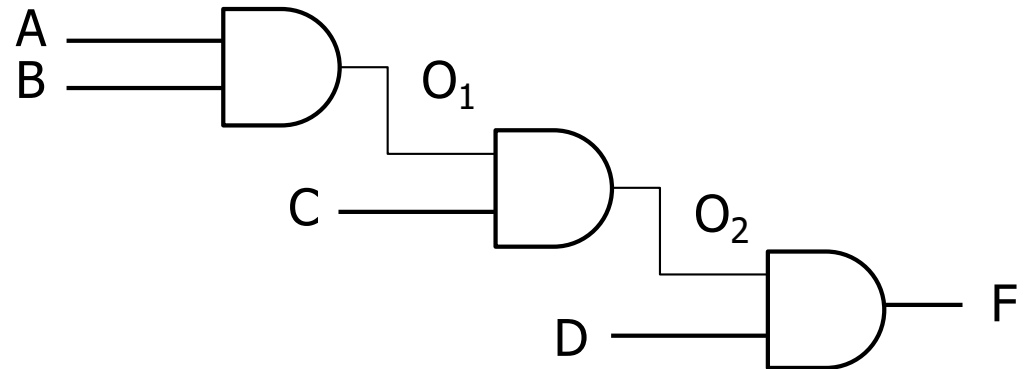


Reduce Activity Factor

Tree



Chain



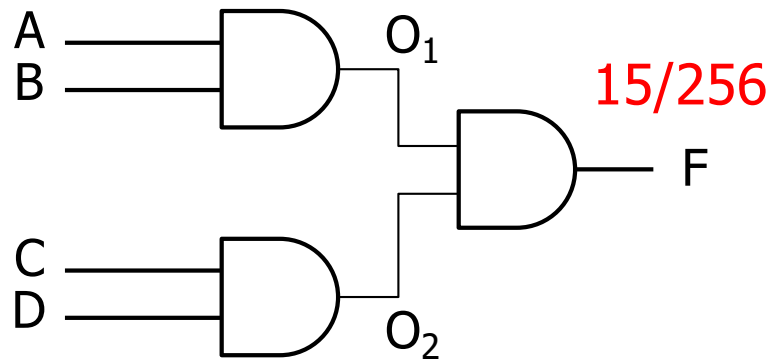
$$a = p(out_i = 0)p(out_{i+1} = 1)$$

$$a = \frac{N_0}{2^N} \frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

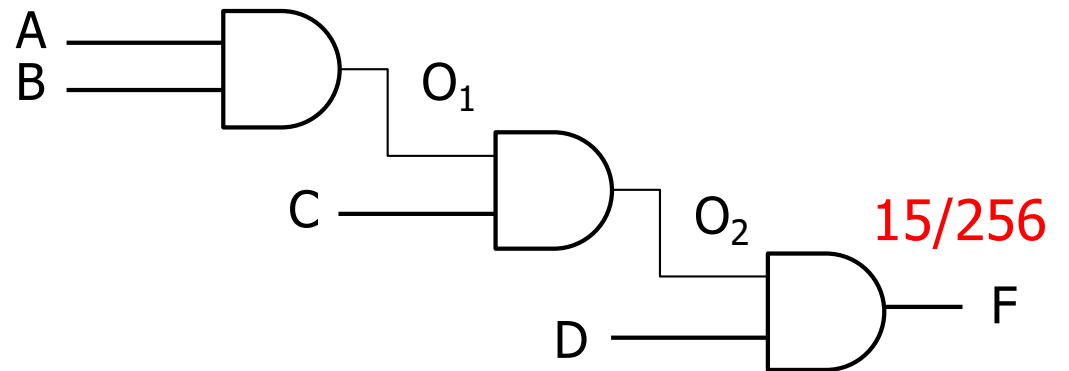


Reduce Activity Factor

Tree



Chain

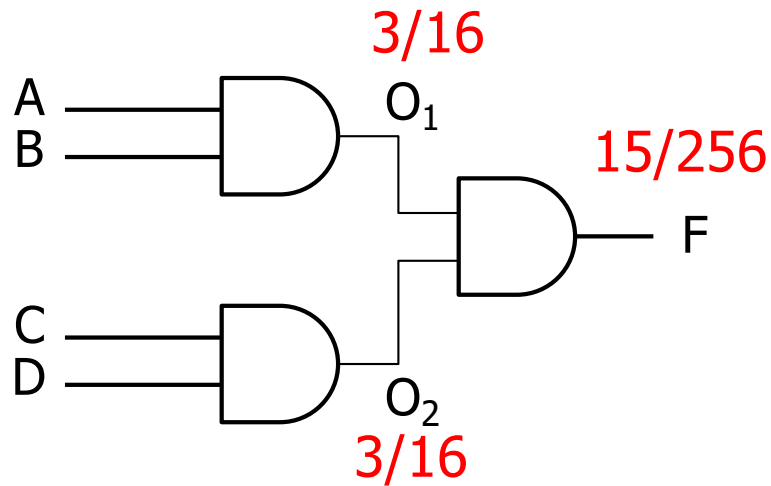


$$a = p(out_i = 0)p(out_{i+1} = 1)$$

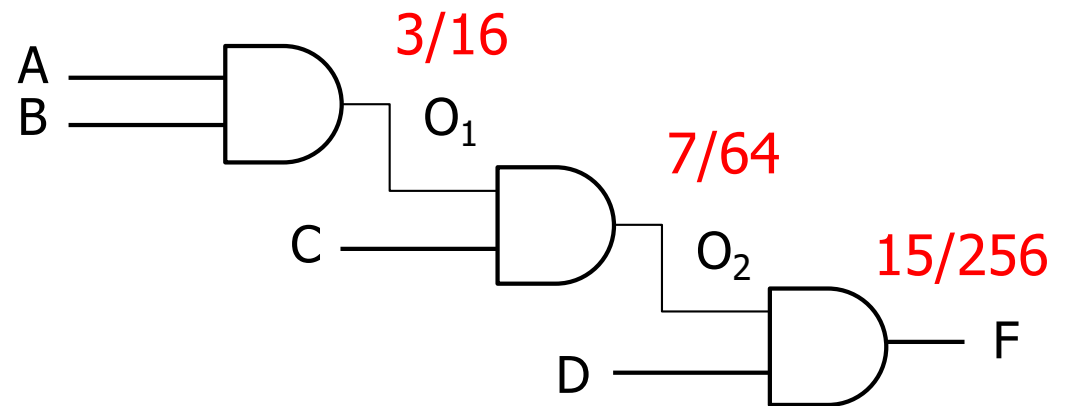
$$a = \frac{N_0}{2^N} \frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Reduce Activity Factor

Tree



Chain



$$a = p(out_i = 0)p(out_{i+1} = 1)$$

$$a = \frac{N_0}{2^N} \frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$



Reduce V_{dd} (Preclass 2)

□ $V_{dd}=520\text{mV}$, $V_{thn} = |V_{thp}| = 300\text{mV}$

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V			
140mV			
260mV			
380mV			
520mV			

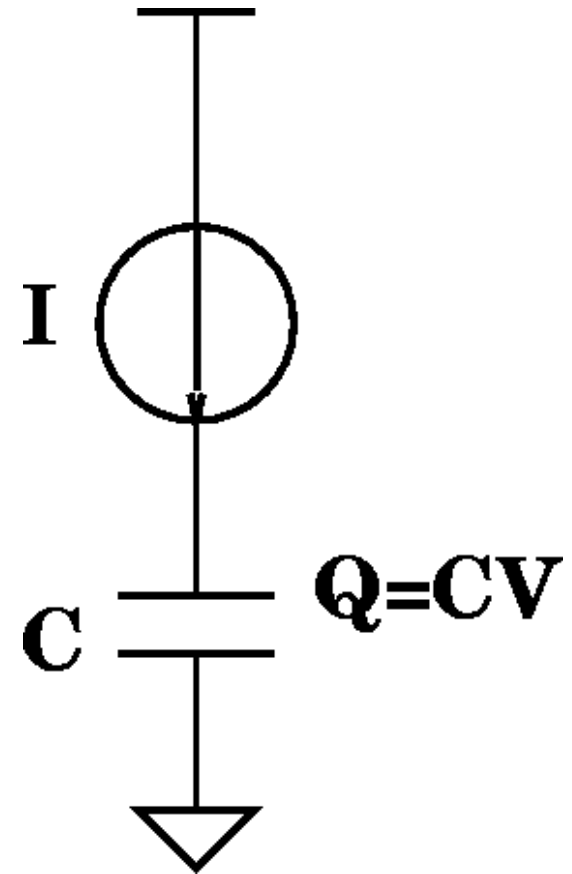


Reduce V_{dd}

- What happens as reduce V ?
 - Energy?
 - Static
 - Switching
 - Delay?

Reduce V_{dd} :

- ❑ $\tau_{gd} = Q/I = (CV)/I$
- ❑ $I_d = (\mu C_{OX}/2)(W/L)(V_{gs} - V_{TH})^2$
- ❑ τ_{gd} impact?
- ❑ $\tau_{gd} \propto \frac{1}{V}$



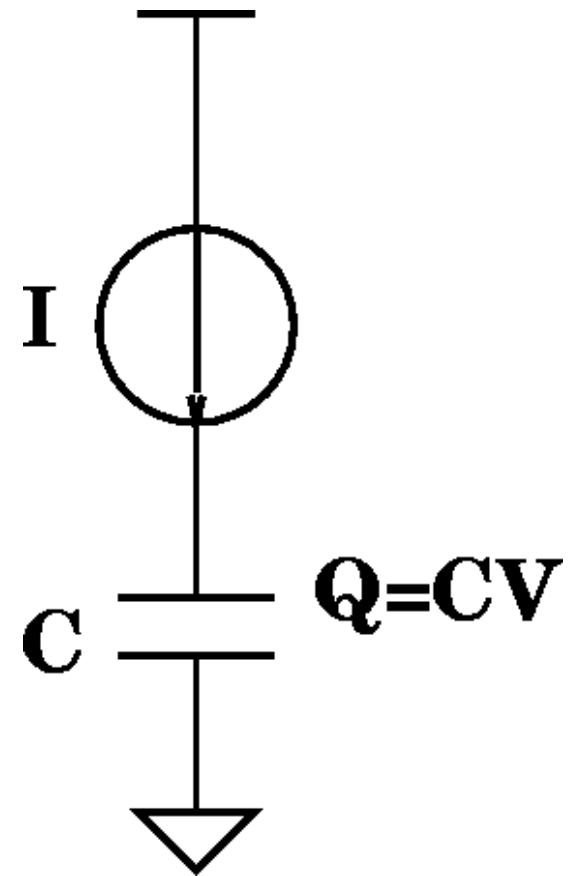
Reduce V_{dd} :

- ❑ $\tau_{gd} = Q/I = (CV)/I$
- ❑ $I_d = (\mu C_{OX}/2)(W/L)(V_{gs} - V_{TH})^2$
- ❑ τ_{gd} impact?

- ❑ $\tau_{gd} \propto \frac{1}{V}$

- ❑ Ignoring leakage:

$$E \propto V^2$$



Reduce V_{dd} :

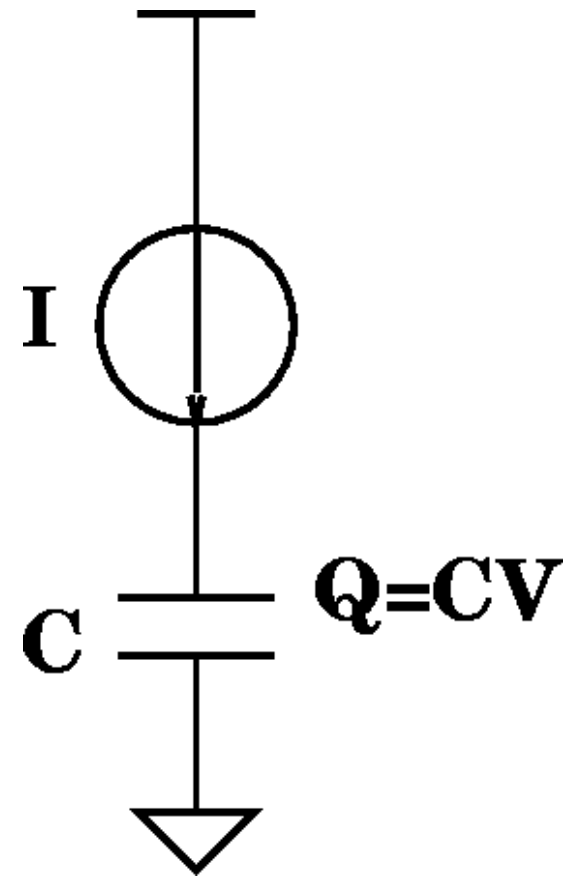
- ❑ $\tau_{gd} = Q/I = (CV)/I$
- ❑ $I_d = (\mu C_{OX}/2)(W/L)(V_{gs} - V_{TH})^2$
- ❑ τ_{gd} impact?

- ❑ $\tau_{gd} \propto \frac{1}{V}$

- ❑ Ignoring leakage:

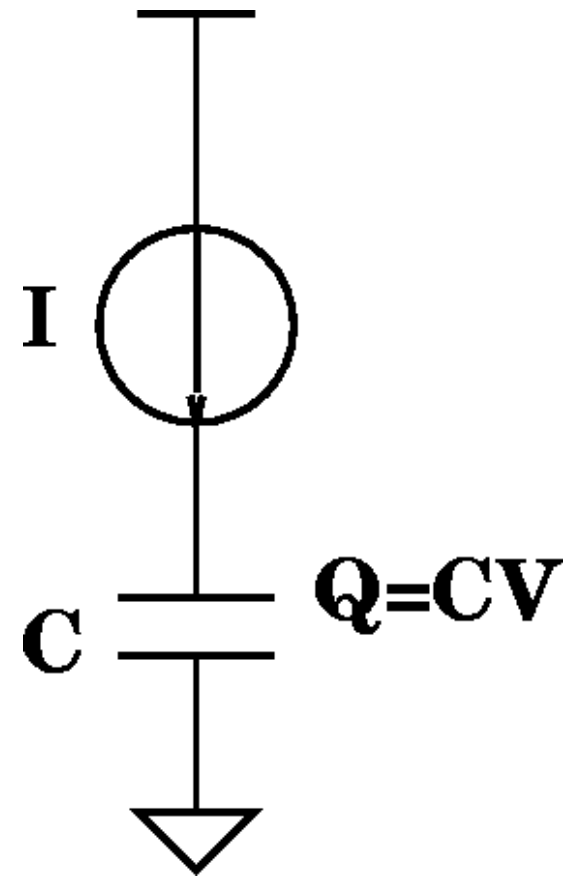
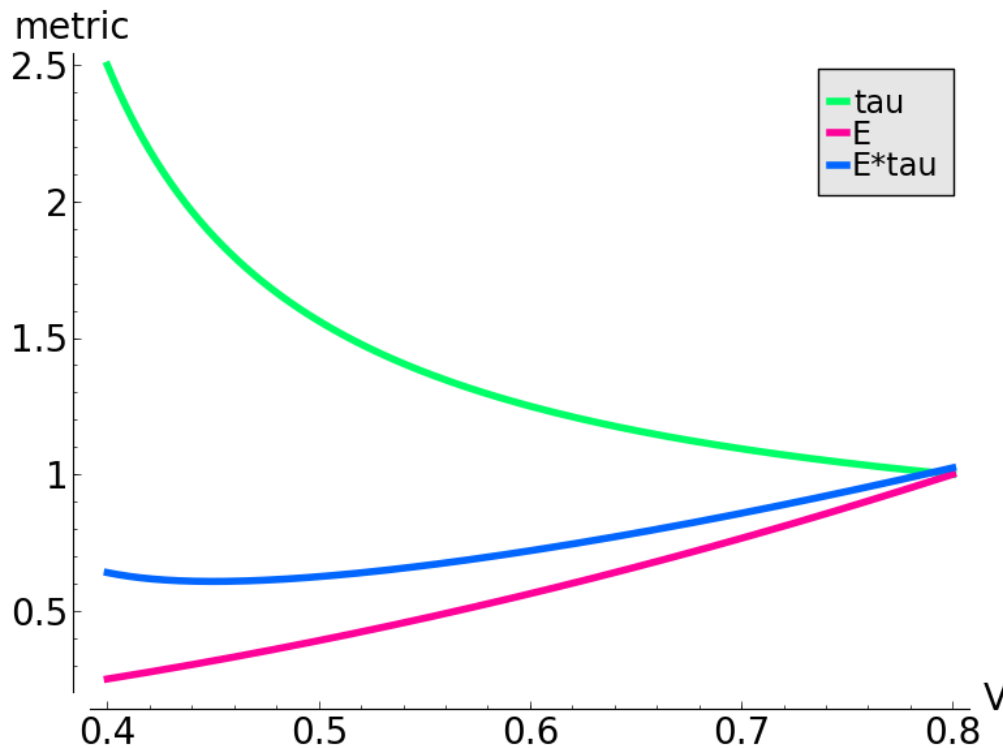
$$E \propto V^2$$

$$E\tau^2 \approx Const$$



Reduce V_{dd} : Velocity Saturation

- ❑ $\tau_{gd} = Q/I = (CV)/I$
- ❑ $I_d = (v_{sat} C_{OX})(W)(V_{gs} - V_{TH} - V_{DSAT}/2)$
- ❑ τ_{gd} impact?





Reduce V_{dd} (Preclass 3)

- $V_{thn} = |V_{thp}| = 300\text{mV}$, $V_{in} = V_{dd}$, estimate $E\tau$

V_{dd}	I_{dyn}	$\tau / (\tau @ V_{dd}=1)$	$E_{switch} / (E_{switch} @ V_d=1)$	$E\tau$
1V				
700mV				
500mV				
350mV				
260mV				

Increase V_{th} (Preclass 4)

- What is impact of increasing threshold on
 - Delay?
 - Leakage?
- $V_{dd}=1V, V_{in}=V_{dd}$

$V_{thn} = -V_{thp}$	I_{dyn}	$\tau / (\tau @ V_{th} = 300mV)$	I_{static}	$I_{stat} / (I_{stat} @ V_{th} = 300mV)$
300mV				
460mV				
600mV				



Big Ideas

- Three components of power
 - Static
 - Dynamic
 - Short-circuit
- $P_{tot} = P_{static} + P_{dyn} + P_{sc}$
- Tradeoff between energy and speed
 - Want to look at the energy-delay product for optimality



Admin

- ❑ HW 5 due Friday
- ❑ Proj 1 posted Friday
 - Design 8-bit adder (baseline design)
 - Milestone due following Friday 10/22
 - Will get feedback by Sunday morning
 - If you turn in on time
 - If you turn in late, you get feedback late