ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 17: October 18, 2021

Energy Optimization

Ratioed Logic

Today

- Energy Tradeoffs
  - Reduce dynamic power
- Ratioed Logic
  - Break all the rules… (lose our nice properties)
    - Not rail-to-rail signals, steady-state-current…
  - Correctness

Previously

- Three components of power
  - $P_{tot} = P_{static} + P_{dyn} + P_{sc}$
  - $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f + VI'_s(W/L)e^{-Vt/(nkT/q)}$

Reminder:

- Vdd=1V, Vthn=|Vthp|=300mV

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V	180pA	126uA	
140mV	6nA	100uA	
400mV		36uA	18uA
500mV			36uA
600mV		36uA	18uA
860mV	6nA	100uA	
1V	180pA	126uA	

Reduce V_{dd}

- What happens as reduce V?
  - Energy?
    - Static
    - Switching
  - Delay?

Reduce V_{dd} (Preclass 2)

- V_{dd}=520mV, V_{thn}=|V_{thp}|=300mV

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V			
140mV			
260mV			
380mV			
520mV			

Reduce V_{dd} (Preclass 2)

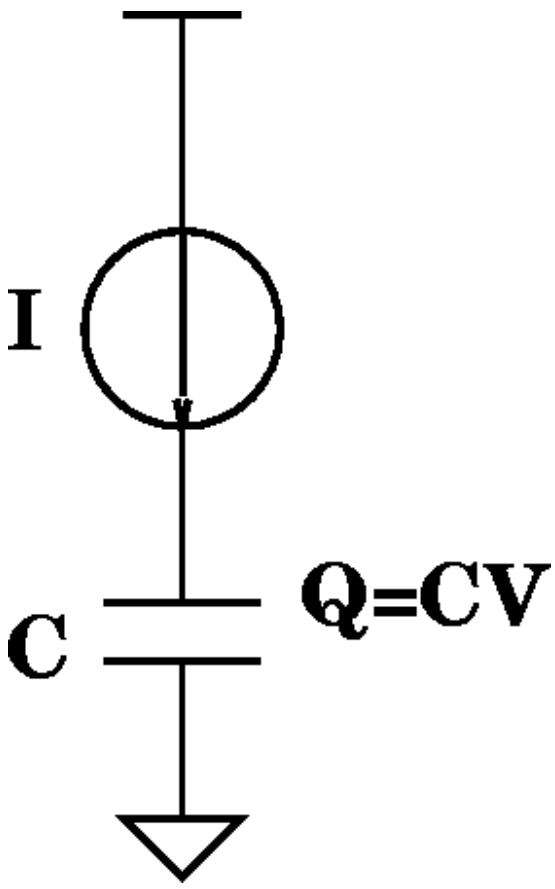
- V_{dd}=520mV, V_{thn}=|V_{thp}|=300mV

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V	180pA	39.6uA	
140mV	6nA	14.4uA	
260mV	111nA		
380mV	6nA	14.4uA	
520mV	180pA	39.6uA	

Reduce V (no velocity saturation)

- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?

- $\tau_{gd} \propto \frac{1}{V}$



Reduce V (no velocity saturation)

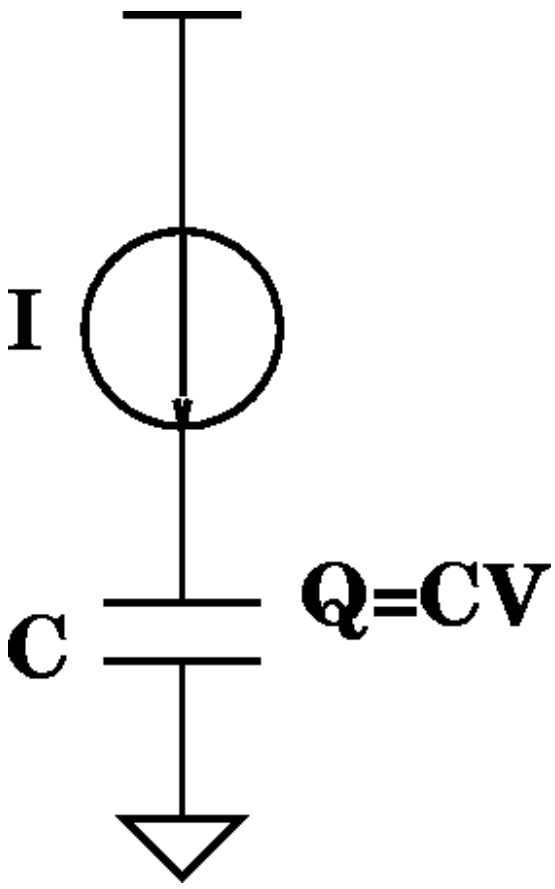
- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?

- $\tau_{gd} \propto \frac{1}{V}$

- Ignoring leakage:

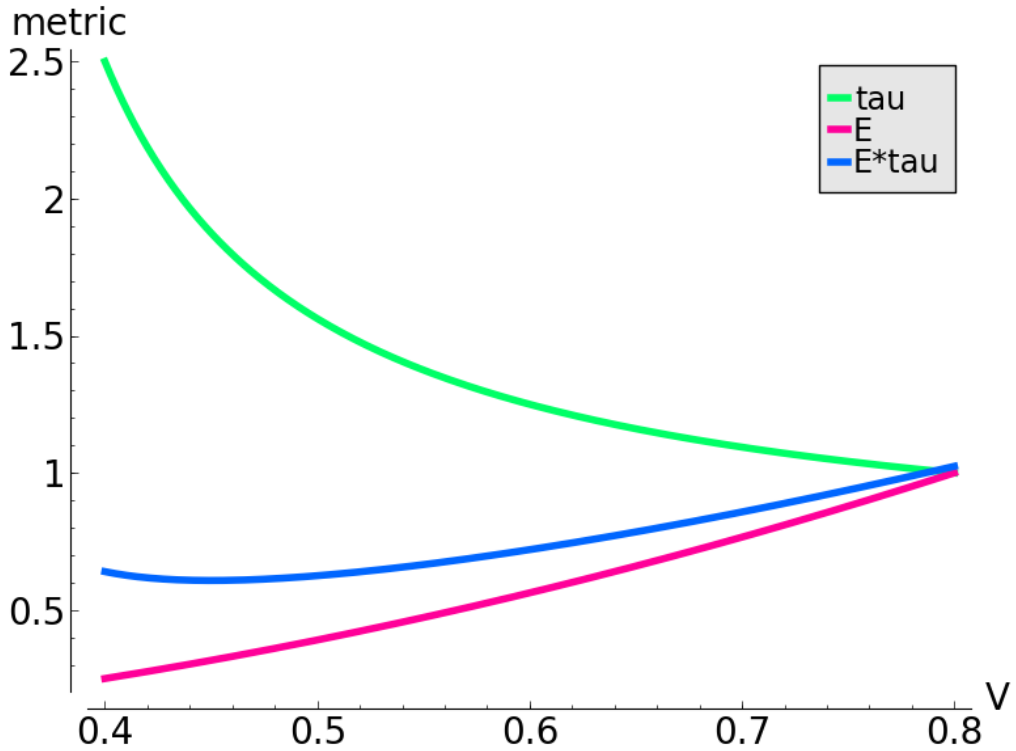
$$E \propto V^2$$

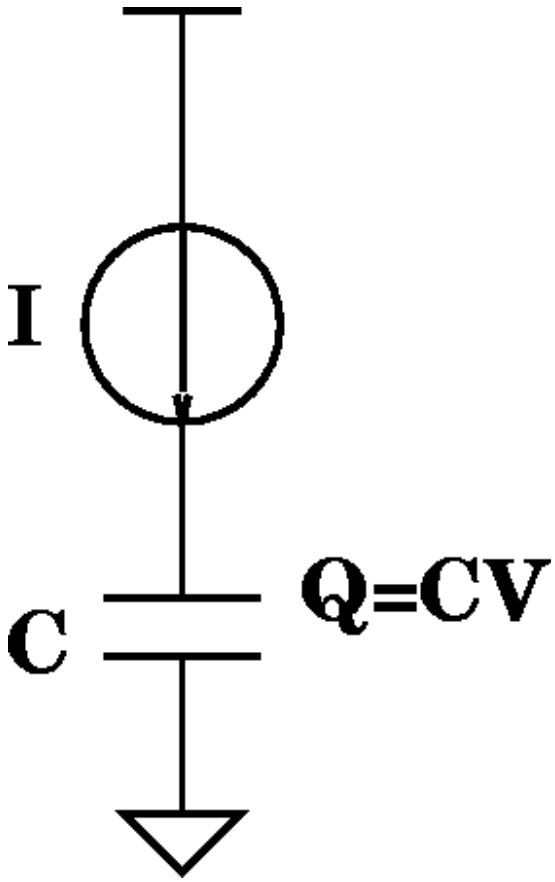
$$E\tau^2 \approx Const$$



Reduce V (velocity saturation)

- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\nu_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$





Reduce V_{dd} (Preclass 3)

- $V_{thn} = |V_{thp}| = 300mV$, $V_{in} = V_{dd}$, estimate $E\tau$

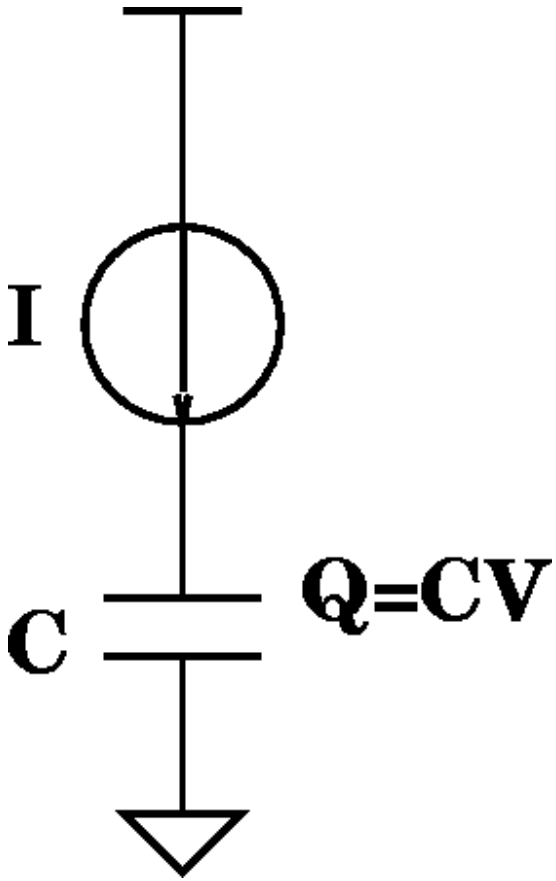
V_{dd}	I_{dyn}	$\tau/(\tau@V_{dd}=1)$	$E_{switch}/(E_{switch}@V_{dd}=1)$	$E\tau$
1V		1	1	1
700mV				
500mV				
350mV				
260mV				

Increase V_{th}?

- What is impact of increasing threshold on
  - Delay?
  - Leakage?

Increase V_{th}

- $\tau_{gd}=Q/I=(CV)/I$
- $I_{ds}=(\nu_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$



Increase V_{th} (Preclass 4)

- What is impact of increasing threshold on
  - Delay?
  - Leakage?
- V_{dd}=1V, V_{in}=V_{dd}

V_{thn}= -V_{thp}	I_{dyn}	$\tau/(\tau@V_{th}$=300mV)	I_{static}	$I_{stat}/(I_{stat}@V_{th}$=300 mV)
300mV		1		1
460mV				
600mV				

Idea

- Tradeoff (knobs: V_{dd}, V_{th}, a, etc.)
  - Speed
  - Switching energy
  - Leakage energy
- Energy-Delay tradeoff: $E\tau^2$, $E\tau$

Ratioed Logic

Previously

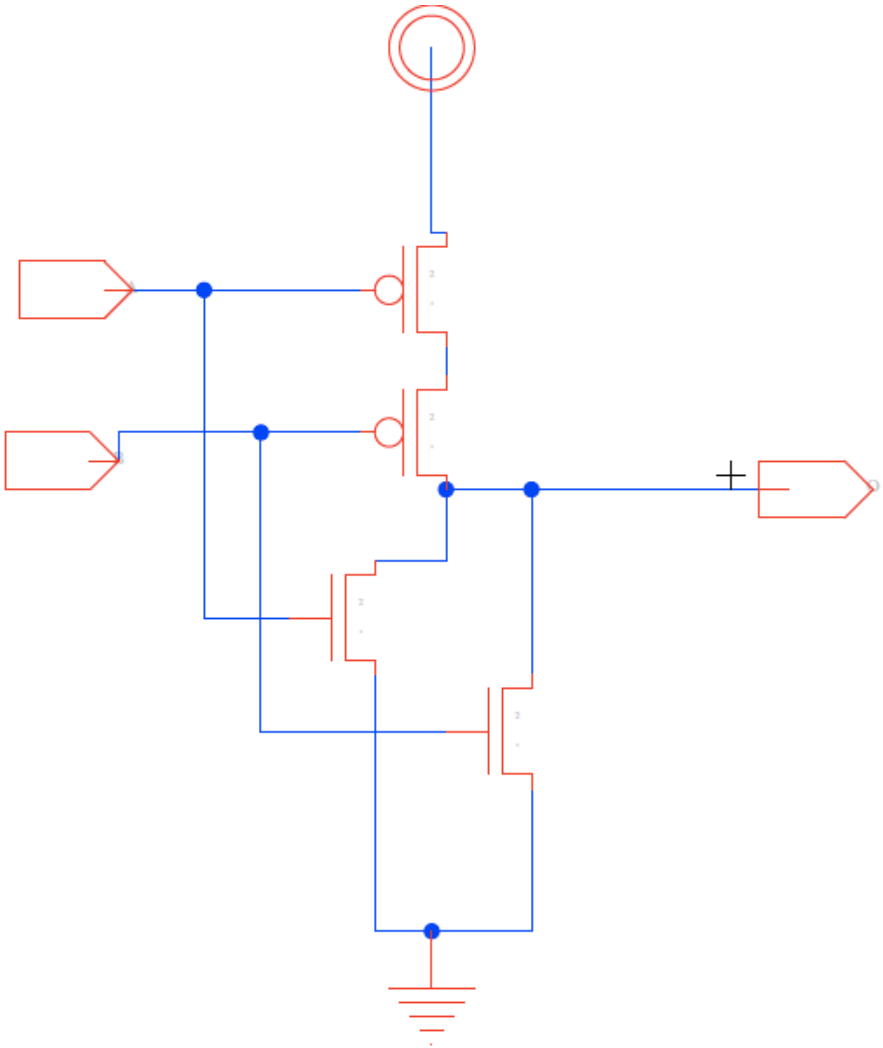
- Restoration and Noise Margins
  - Allows for gate abstraction
- CMOS Gates
  - Drive outputs rail-to-rail
  - Only one PDN/PUN turned on in steady state
    - Only subthreshold leakage current in steady state

Today

- Ratioed Gates
  - Break all the rules… (nice properties)
    - No rail-to-rail outputs, steady-state-current is not subthreshold…
  - Logic correctness
  - Performance
  - Power implications

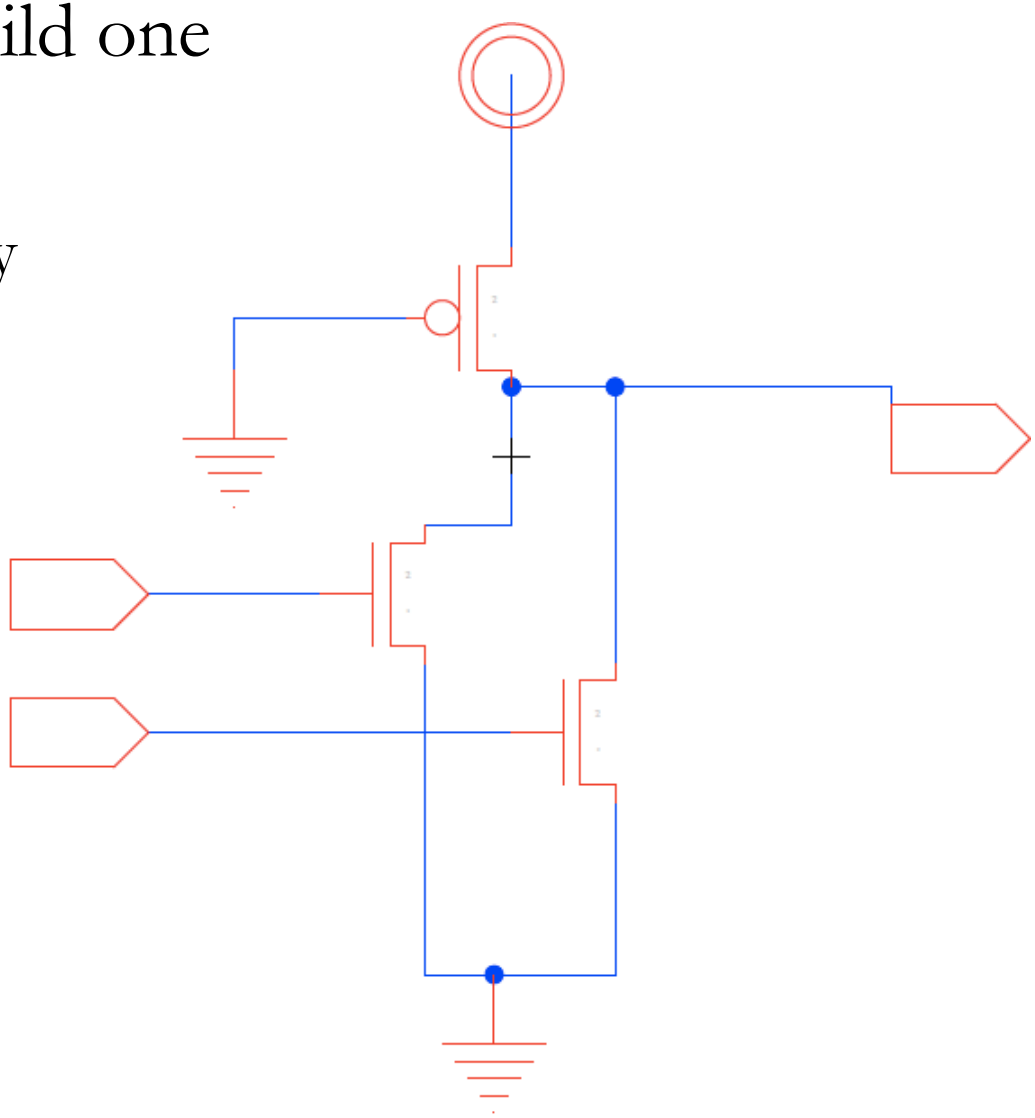
Idea

- Building both pull-up and pull-down can be expensive – many gates
- Seems wasteful to build logic function twice
  - Once in pullup, once in pulldown
  - Large gate capacitance



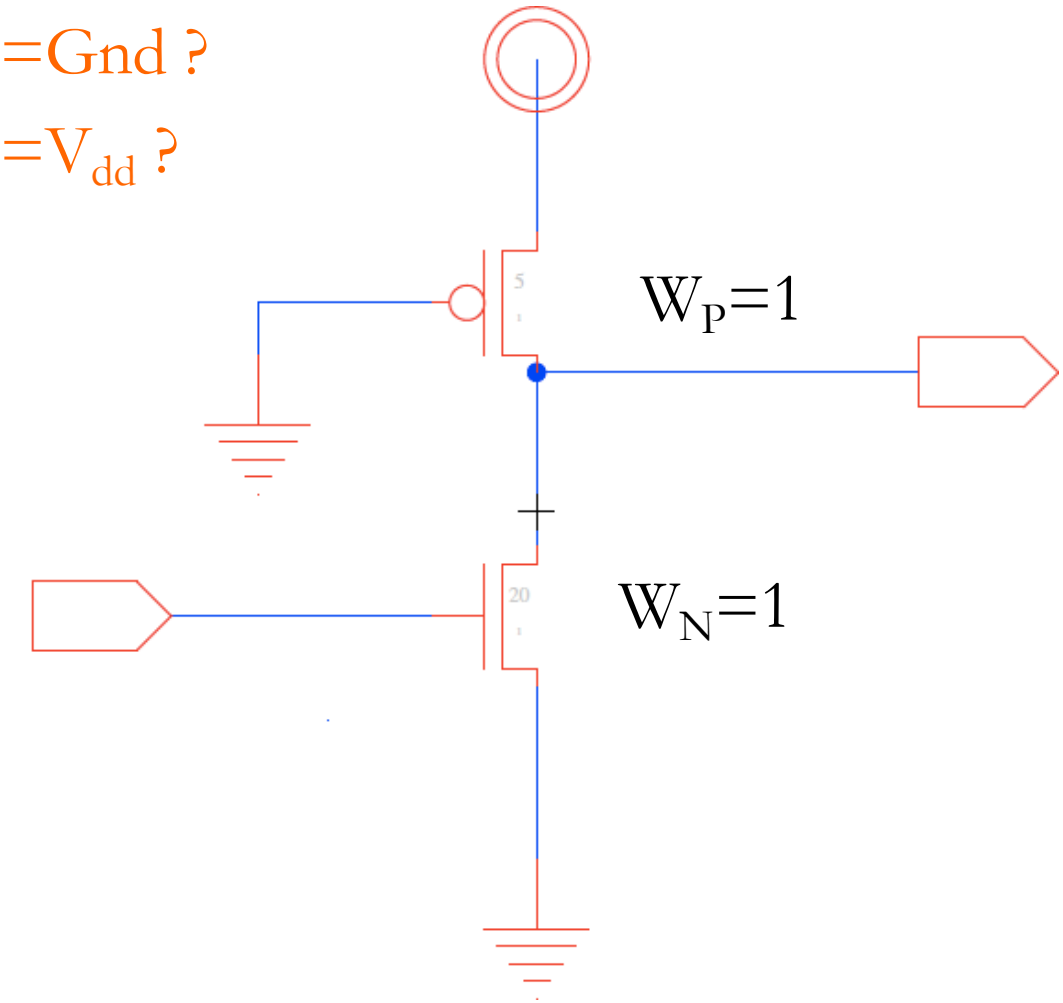
Idea

- Maybe only need to build one
- Build NFET pulldown
  - Exploit high N mobility
    - traditional

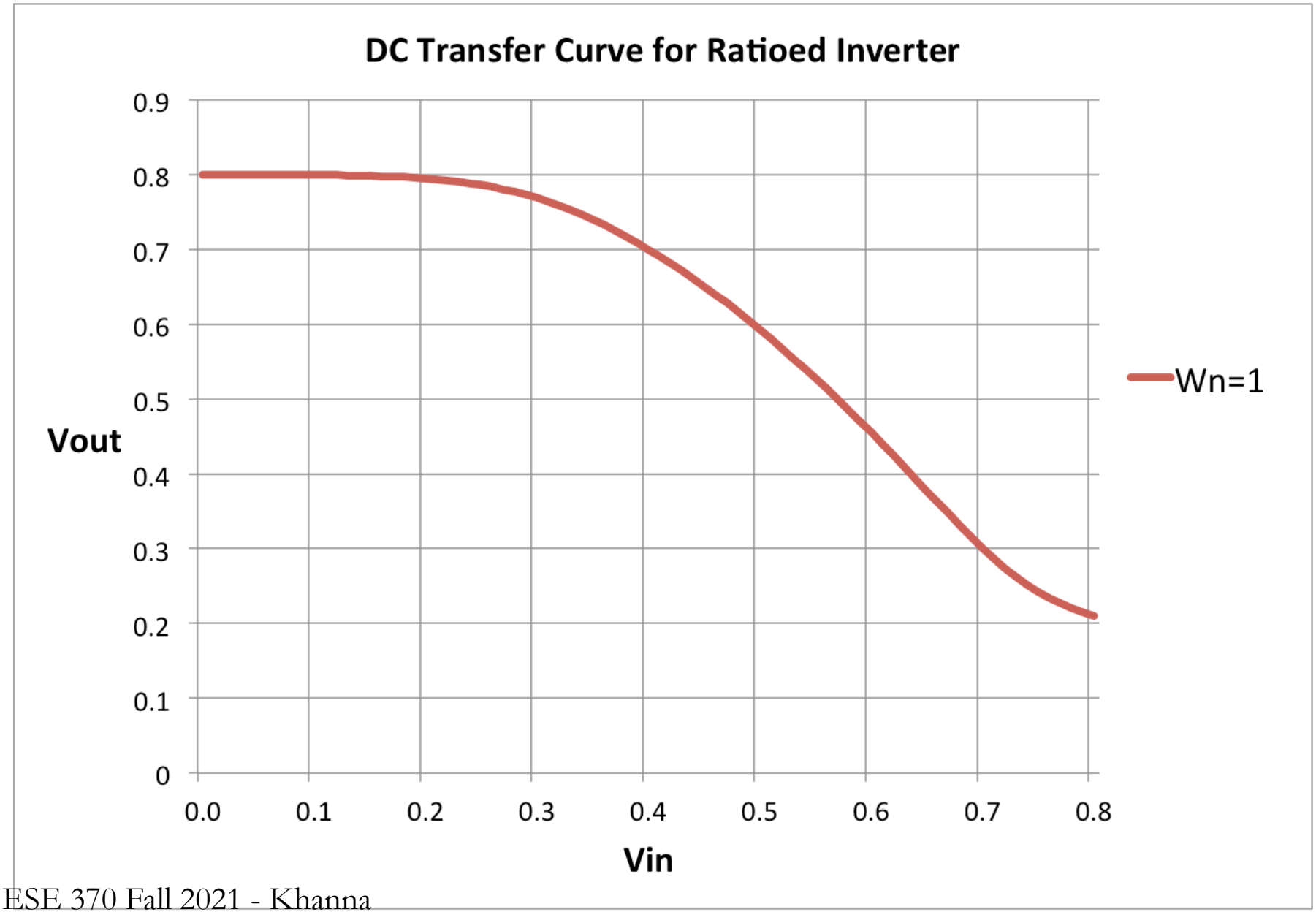


Ratioed Inverter

- Does this work?
  - What is V_{out} for V_{in}=Gnd ?
  - What is V_{out} for V_{in}=V_{dd} ?

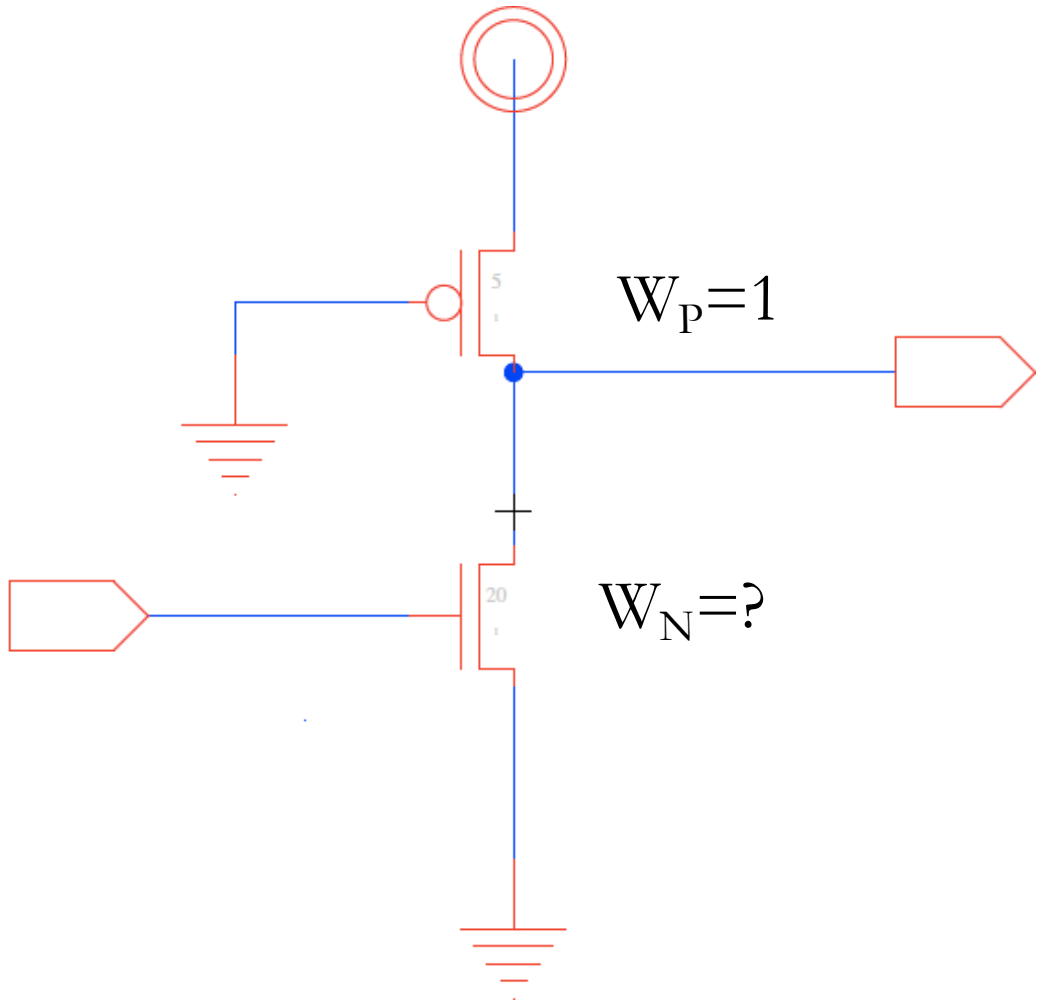


Ratioed Inverter in 22nm

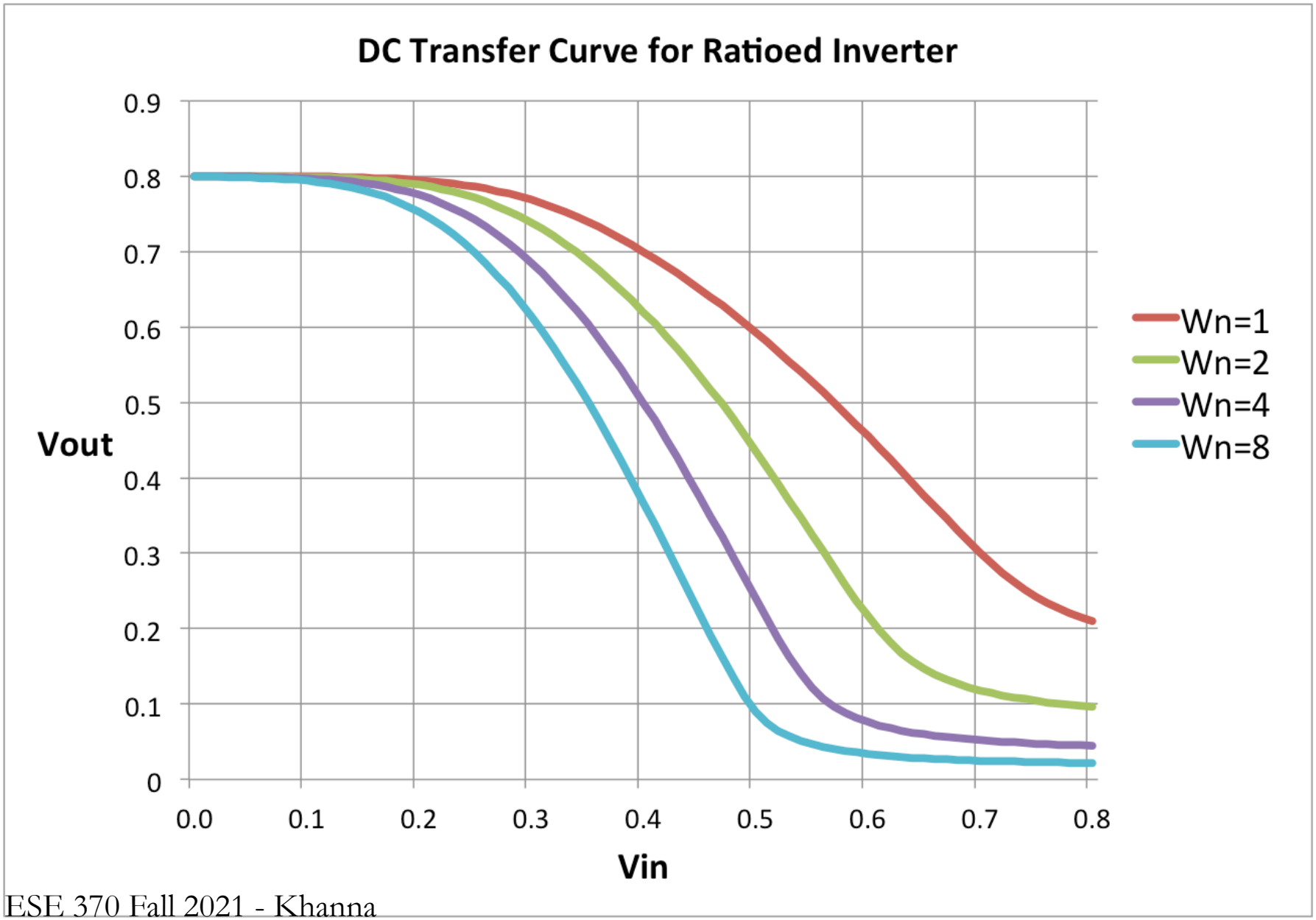


Ratioed Inverter (Preclass 5)

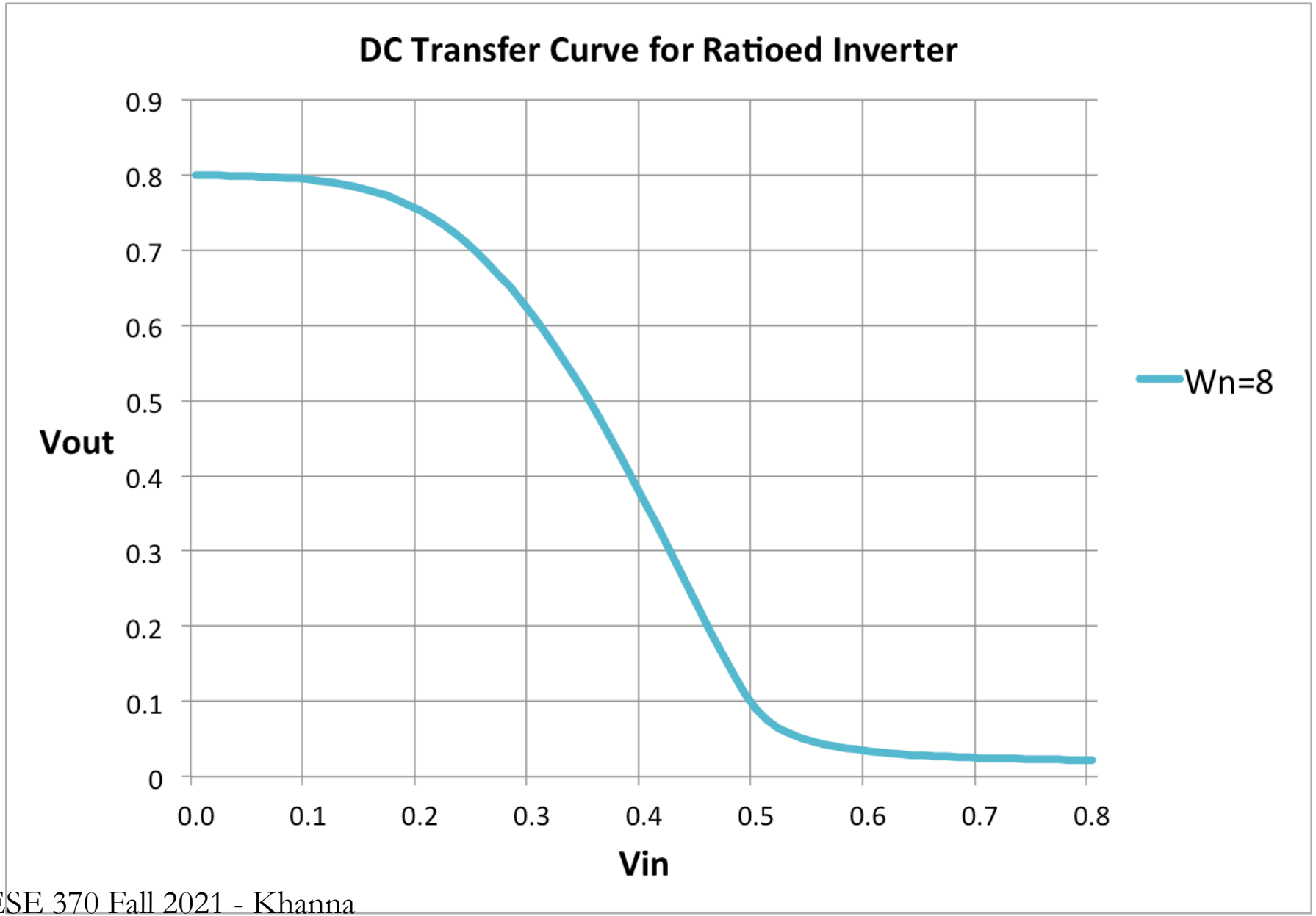
- How do we need to size N to make it "work"?
  - V_{DD}=0.8



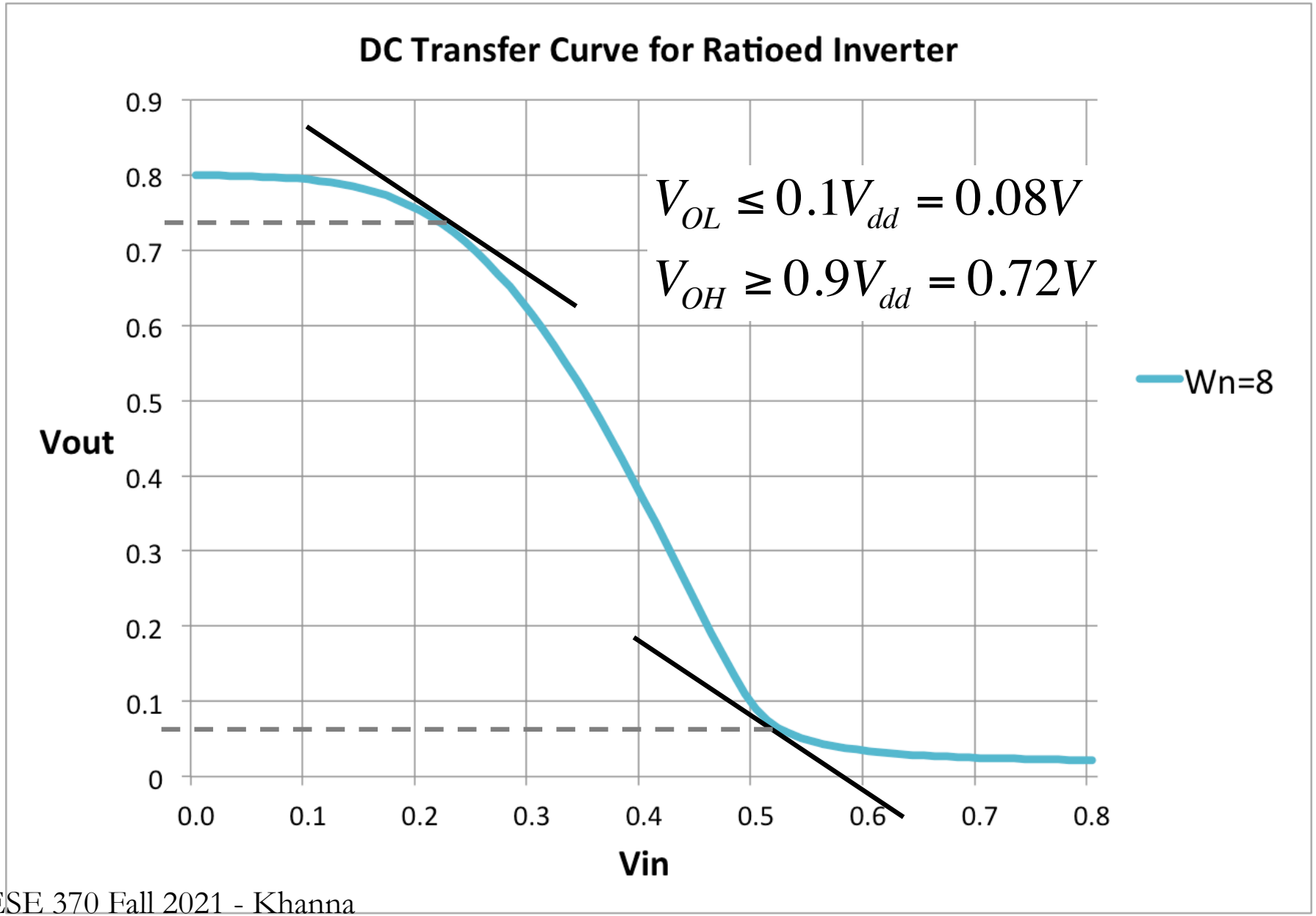
Ratioed Inverter in 22nm



DC Transfer Function

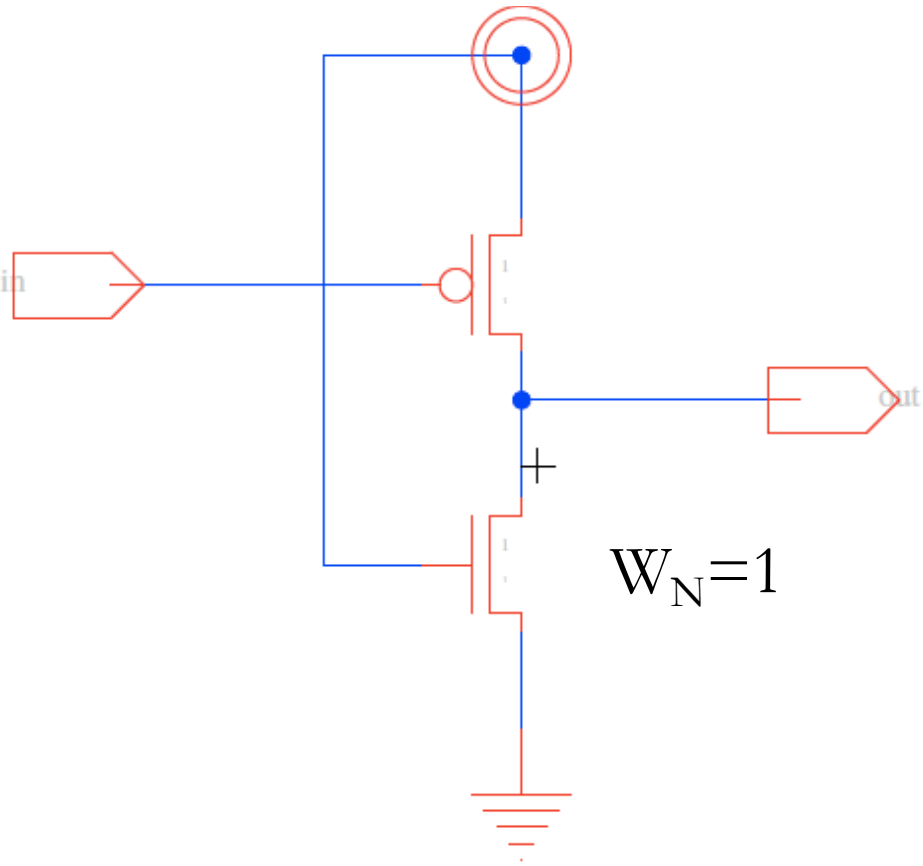


DC Transfer Function

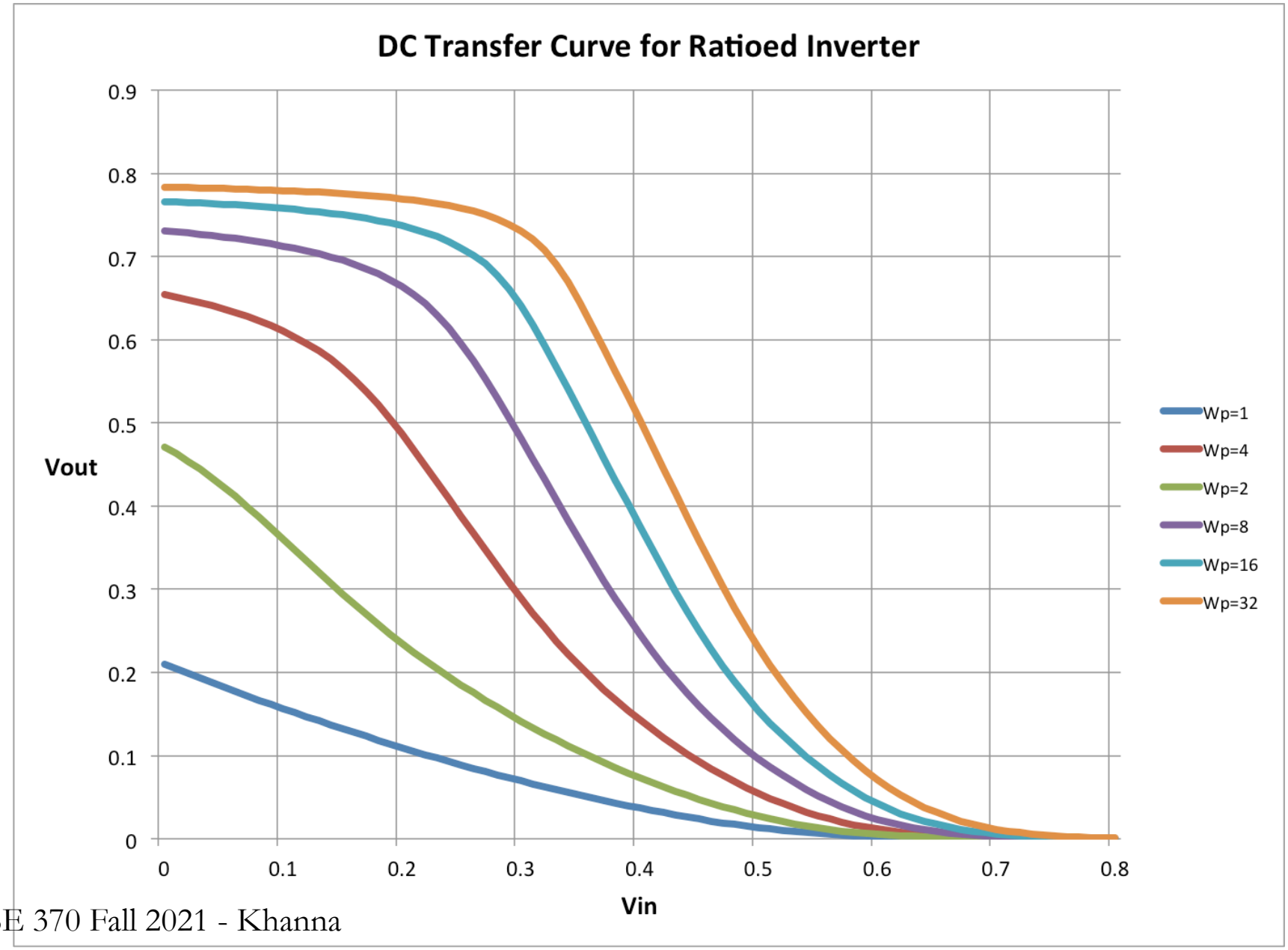


Ratioed Inverter (Preclass 5)

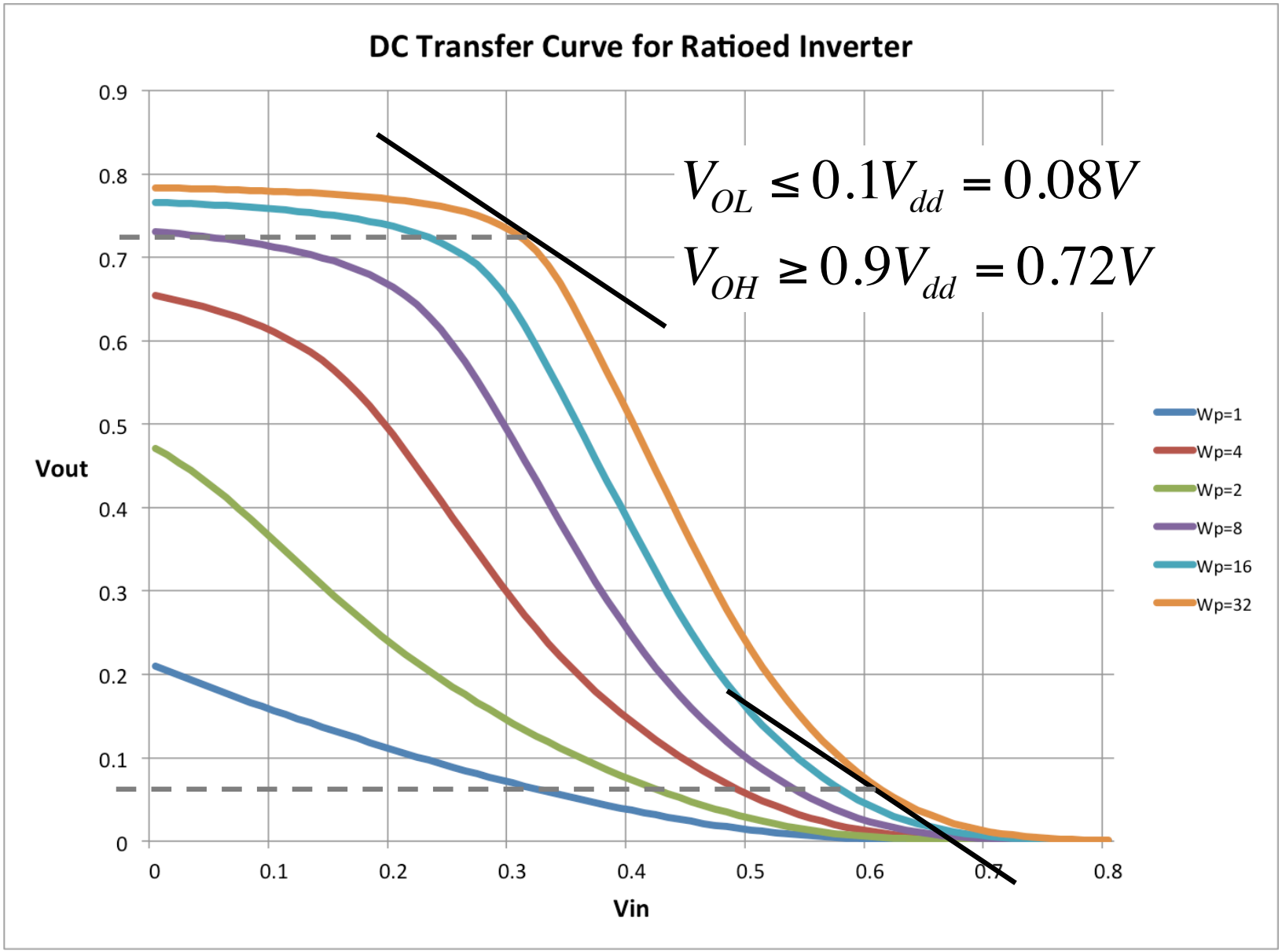
- How do we need to size P to make it work?
  - V_{DD}=0.8



Ratioed Inverter in 22nm

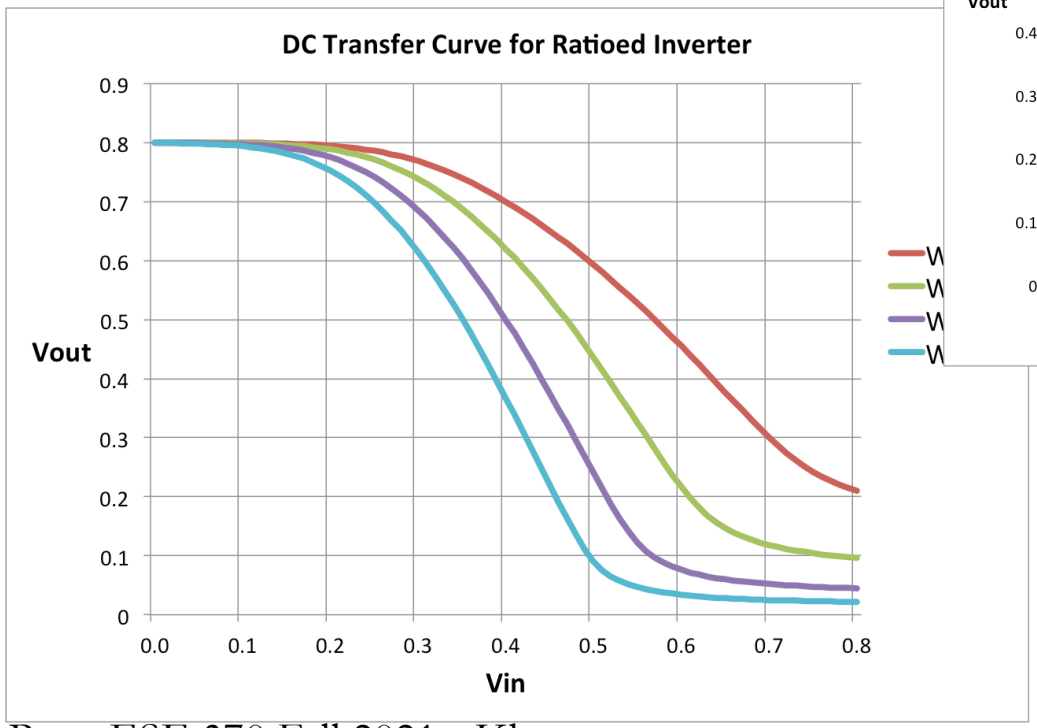


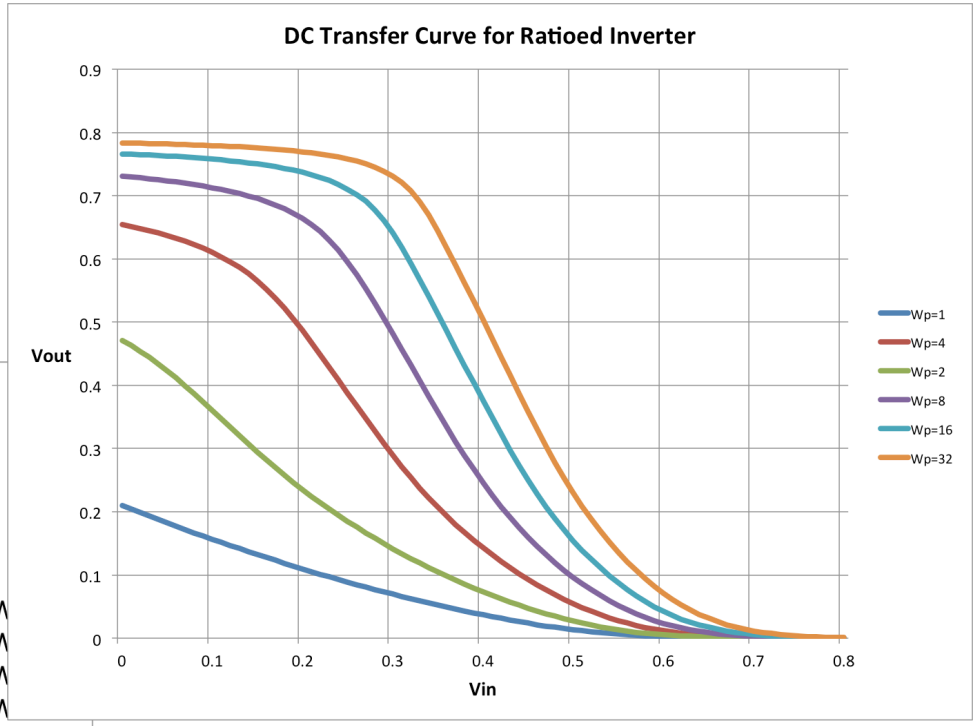
Ratioed Inverter in 22nm



P vs. N

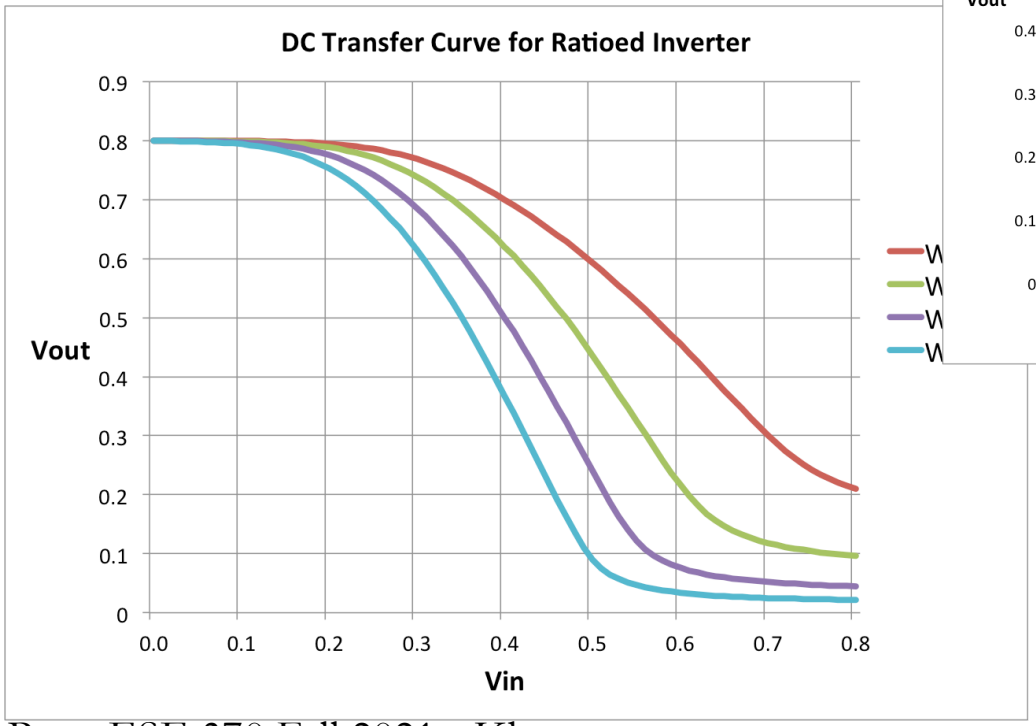
- **Conclude:** still prefer N to P for ratioed logic

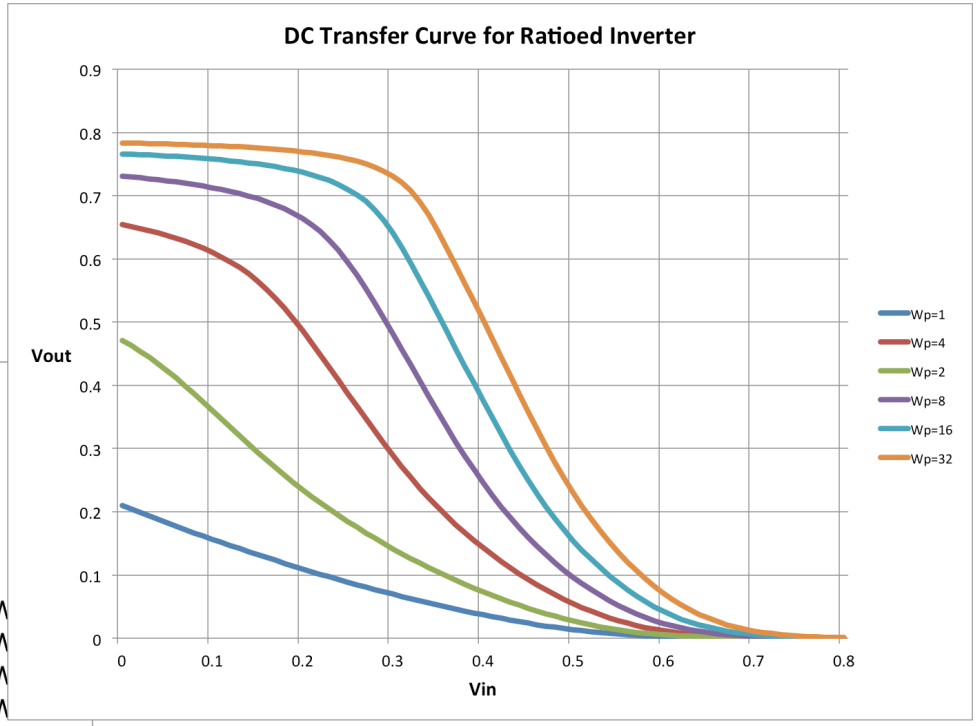




Noise Margin Tradeoff

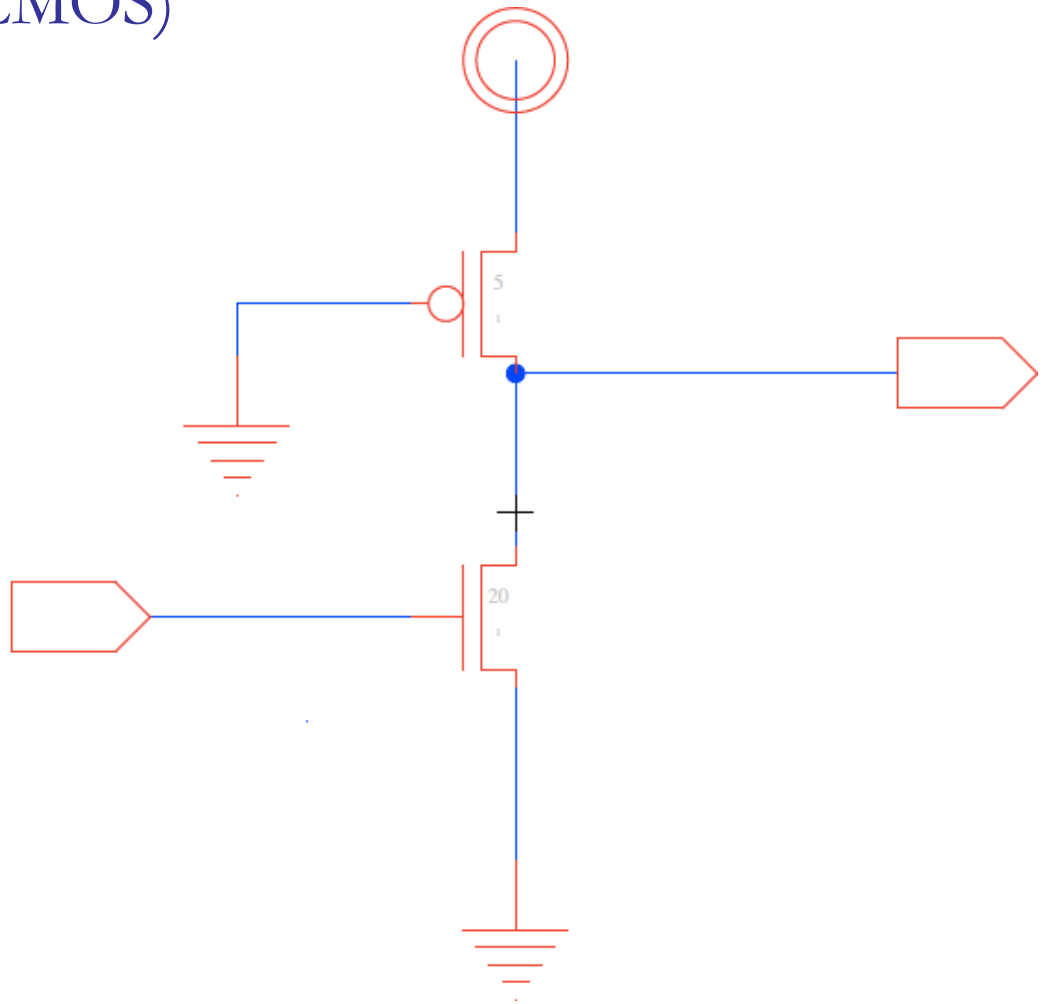
- What is impact of increasing noise margin?
  - On size
  - On input capacitance





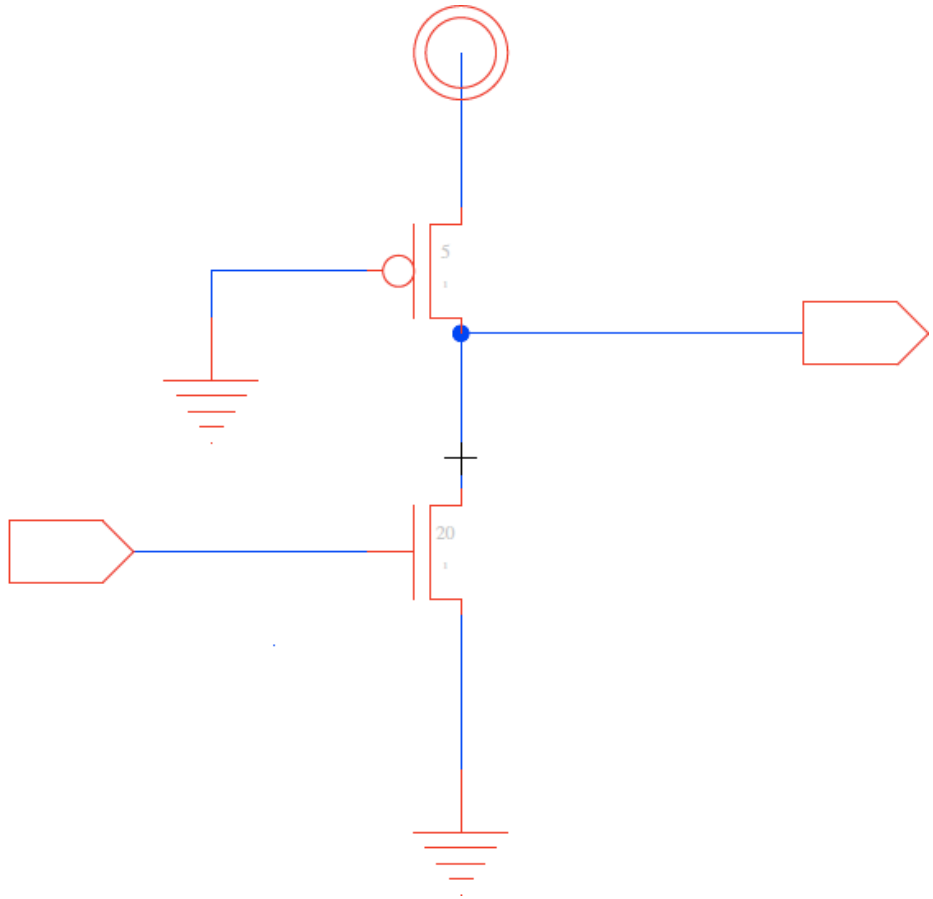
Size for $R_0/2$ drive?

- How do we size for $R_0/2$ drive?
  - (assume $R_{0p}=R_{0n}$ for CMOS)



Static Power

- I_{static} ?
- Input low-Output high?
  - I_{leak}
- Input high-Output low?
  - I_{pmos_on}
  - $\sim V_{dd}/(R_0/2)$ -- for our sample case



Total Power

- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f$

Total Power

- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f$
  $+ p(V_{out}=low)V^2/R_{pon}$
  $+ p(V_{out}=high)VI'_s(W/L)e^{-Vt/(nkT/q)}$

$p(V_{out}=low)$ – probability the output is low

$p(V_{out}=high)$ – probability the output is high

$p(V_{out}=high)=1-p(V_{out}=low)$

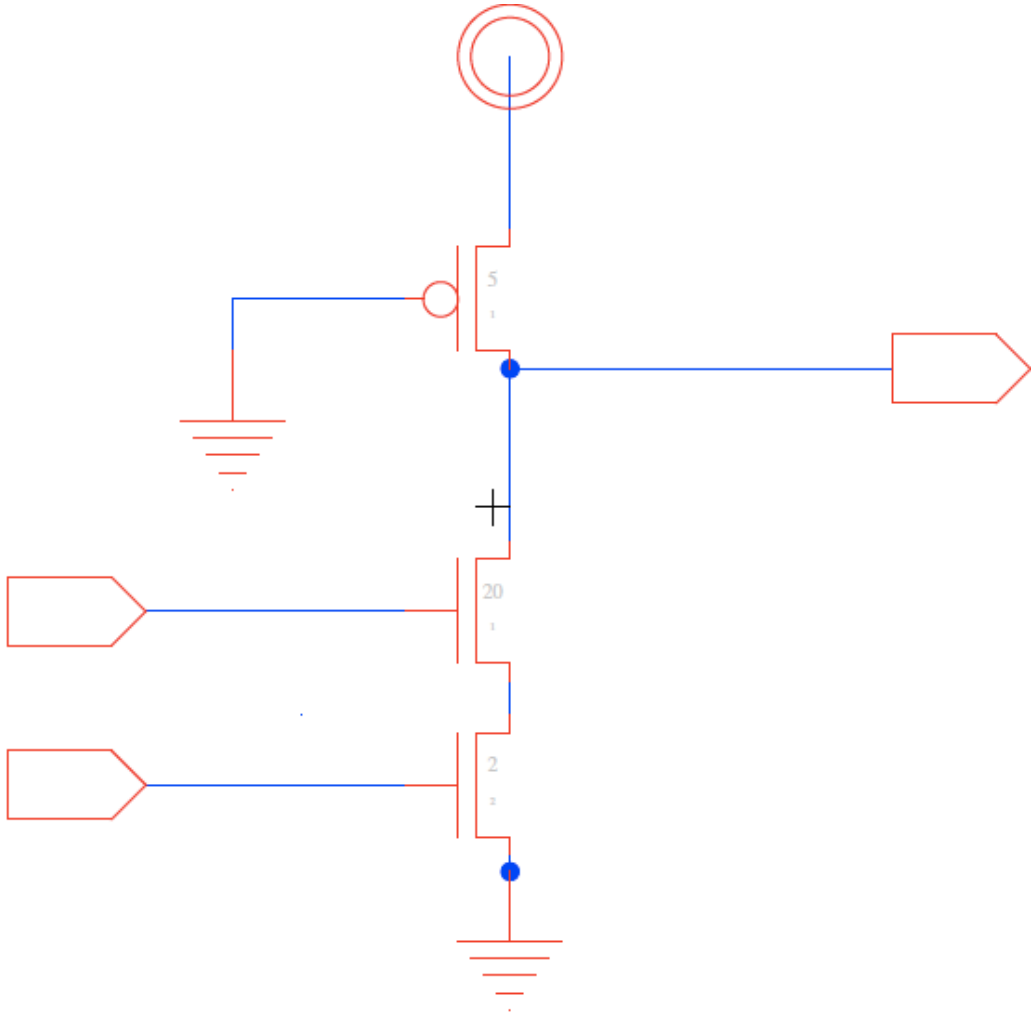
Compare Static CMOS

For $R_{drive}=R_0/2$ inverter (assume $R_{0p}=R_{0n}$ for CMOS)

- Total Transistor Width?
- Input capacitance load?

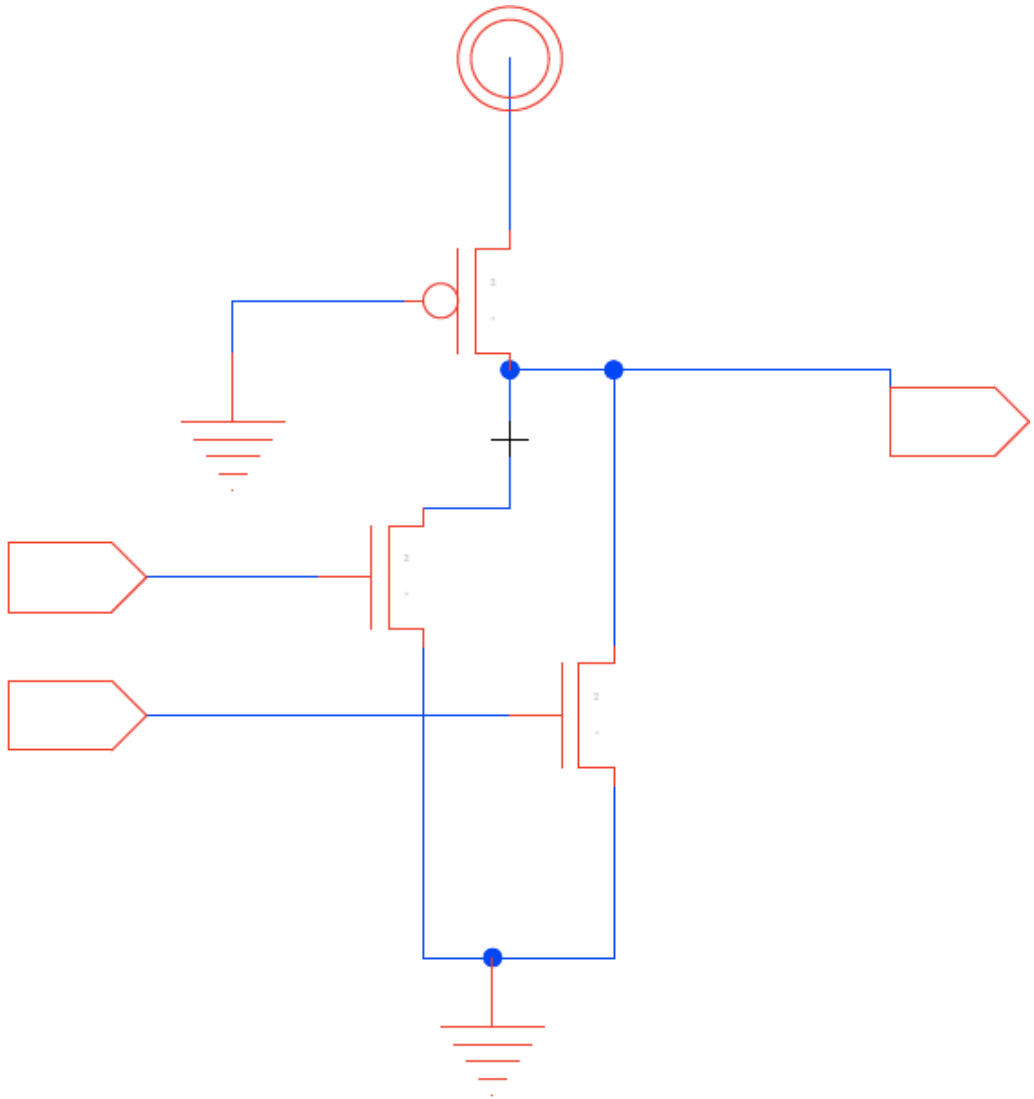
How do we size for $R_0/2$ drive?

- 2-input nand?



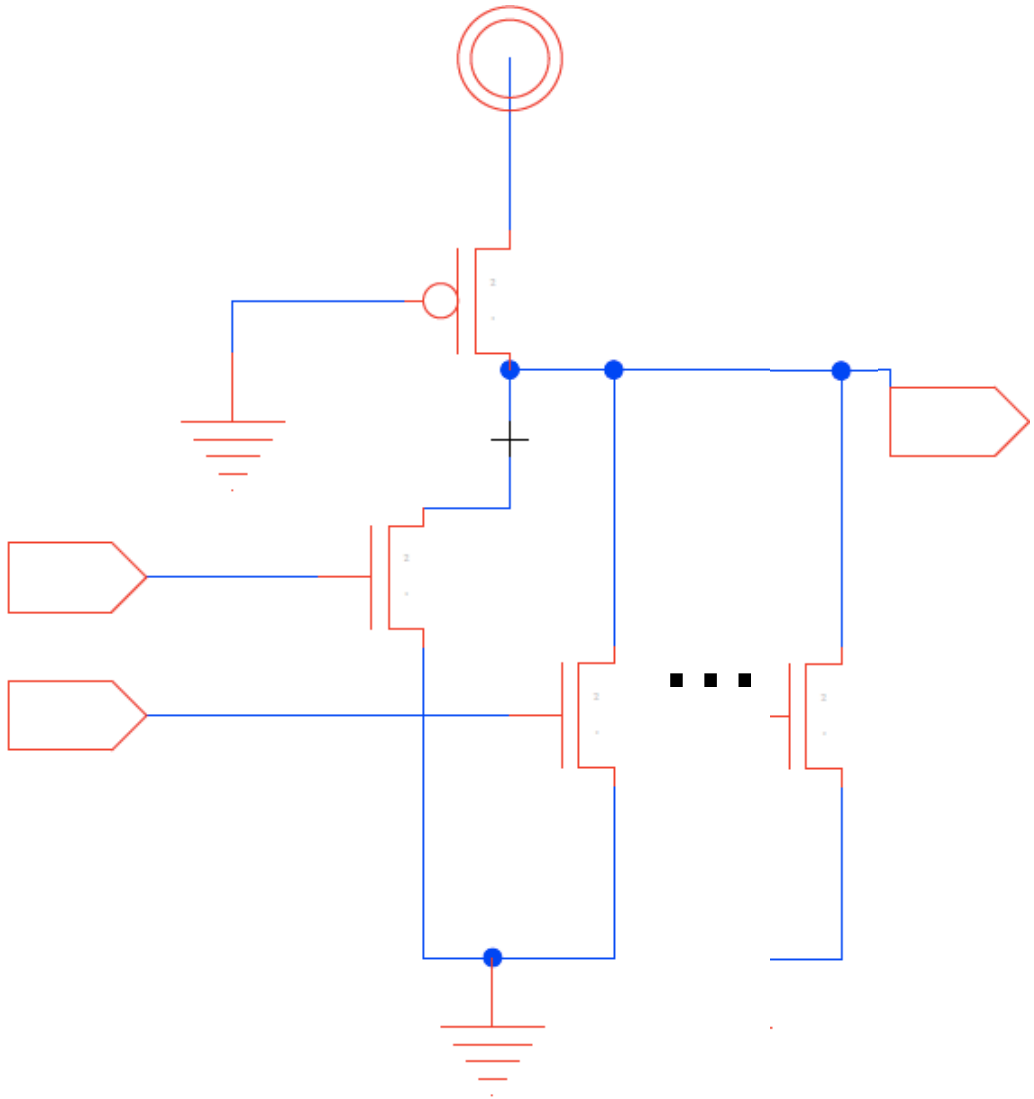
How do we size for $R_0/2$ drive?

- 2-input nor?

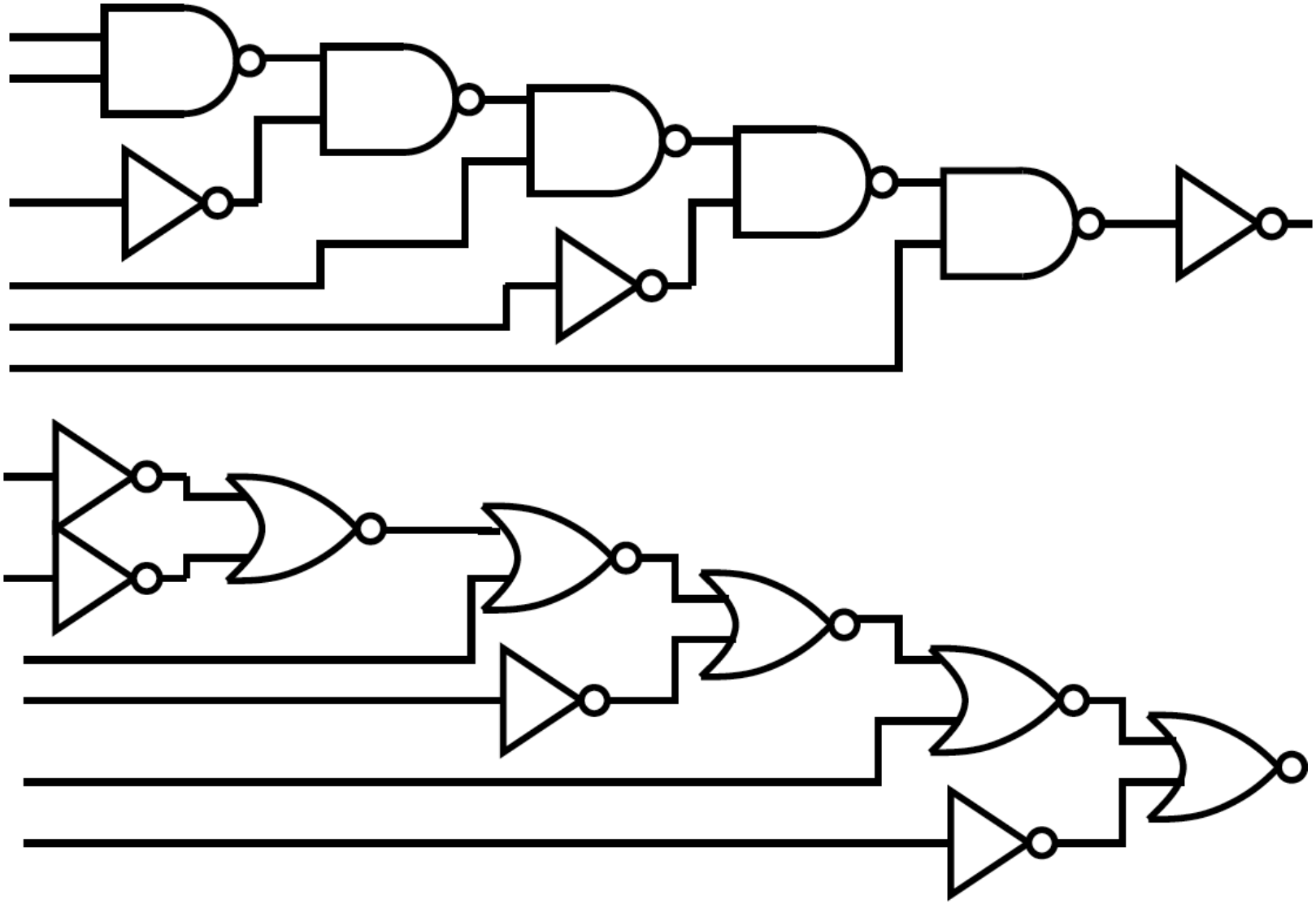


How do we size for $R_0/2$ drive?

- k-input nor?
- What is the input capacitance for k-input nor?



Which Implementation is faster in ratioed logic?



Ideas

- There are other logic disciplines
- You have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates non-leakage static power in one input case

Admin

- Project 1 out now
  - Milestone due Friday (10/22)
    - Baseline is bare minimum, but can start thinking/working on optimizations before
    - Will give you feedback by Sunday morning
  - Design 8-bit ripple-carry adder
    - You already know how to do this
    - Refresh yourself on binary addition of 2 bits
  - Work individually
  - Full Report in two weeks (F 10/29)