ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 18: October 20, 2021

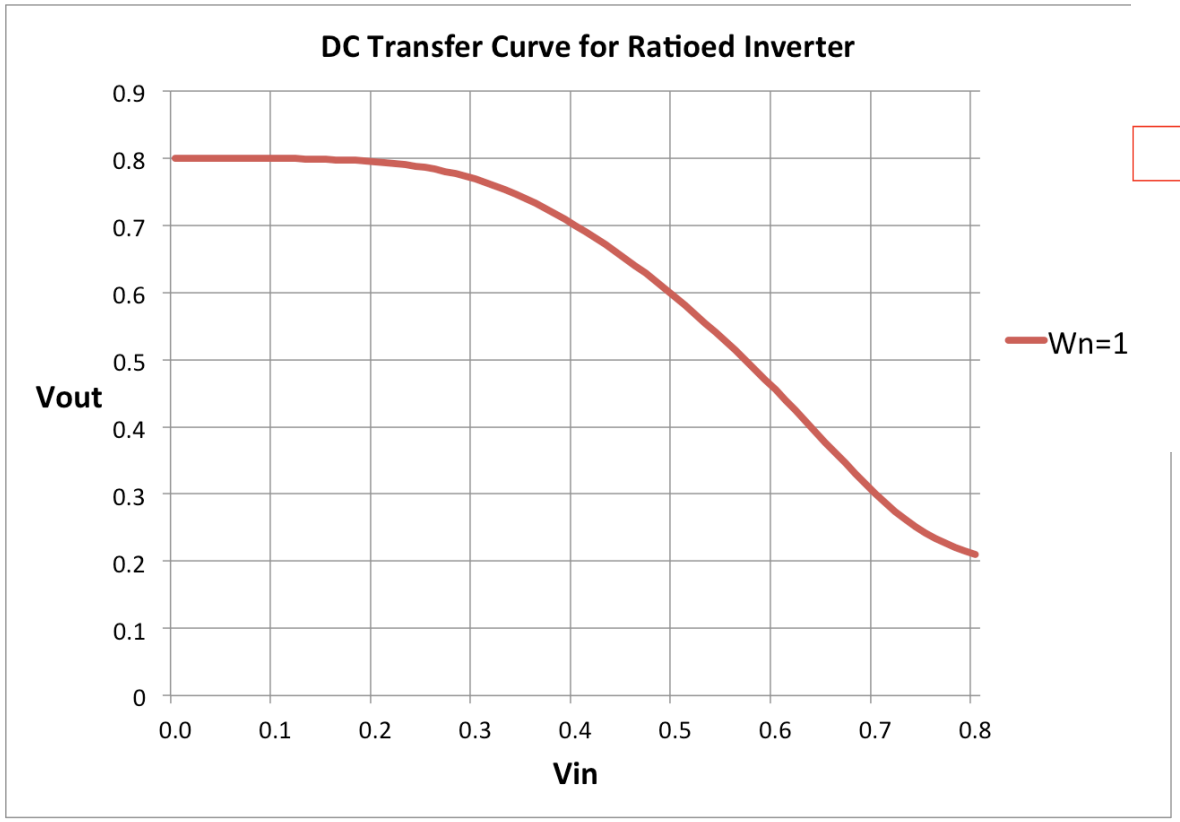
Ratioed Logic, Design Space Exploration

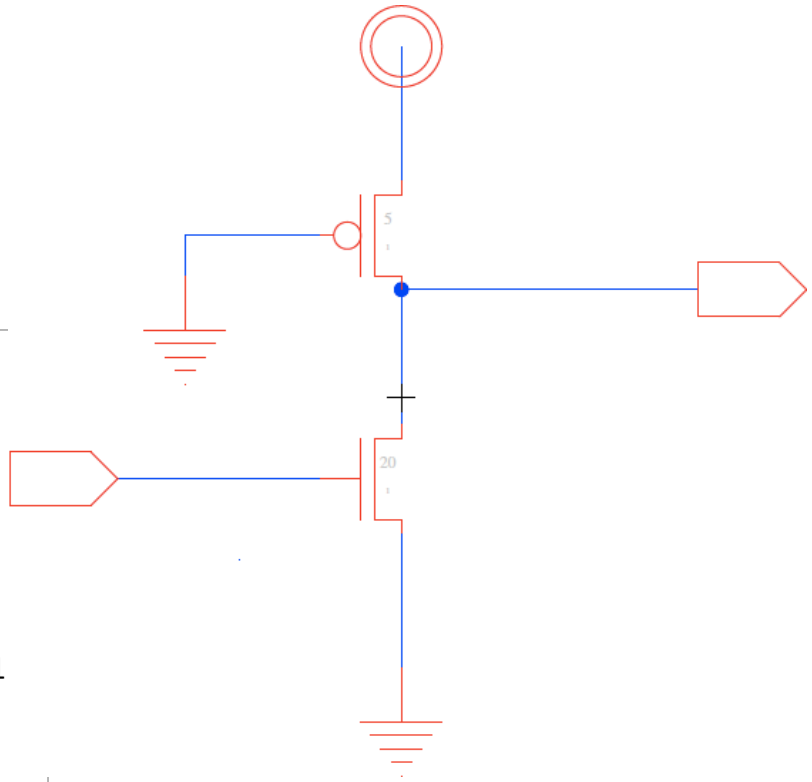
Today

- Finish Ratioed Gates
- Example to discuss and illustrate design space
  - You will want to be exploring design space for Project 2
  - Chance to talk about trends
    - Quantitatively not just qualitatively

Ratioed Inverter

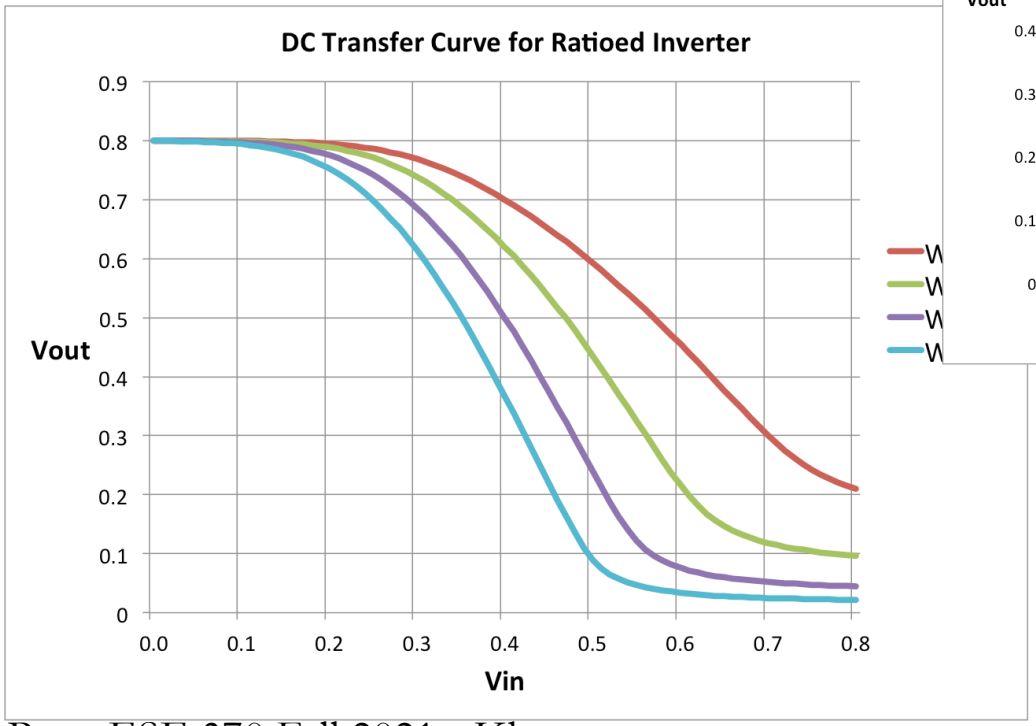
- Build NFET pulldown
  - Exploit high N mobility
    - traditional

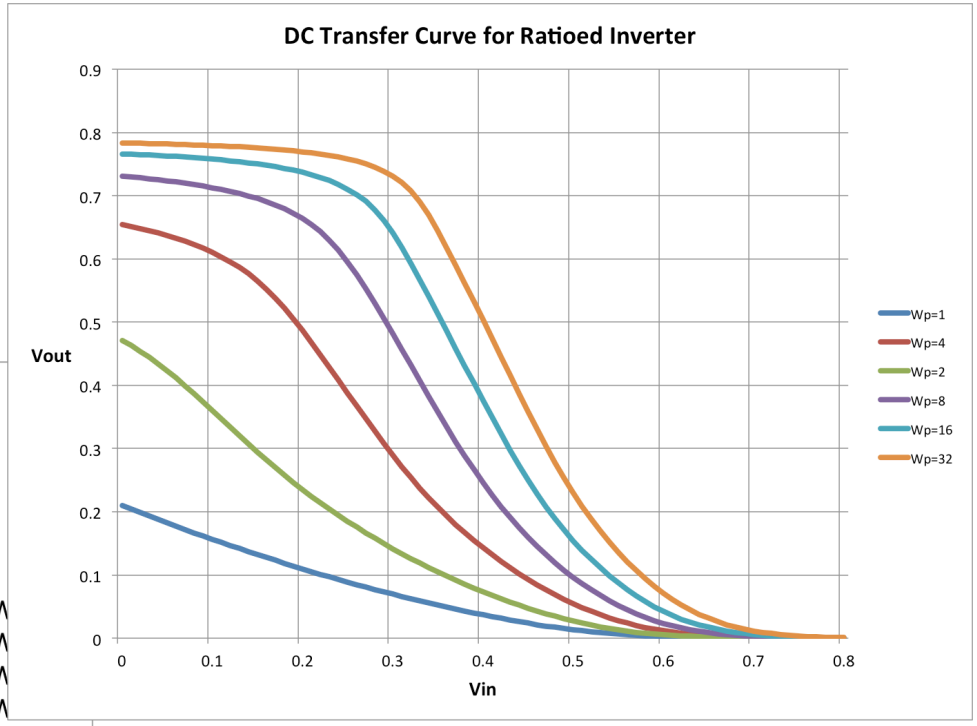




Noise Margin Tradeoff

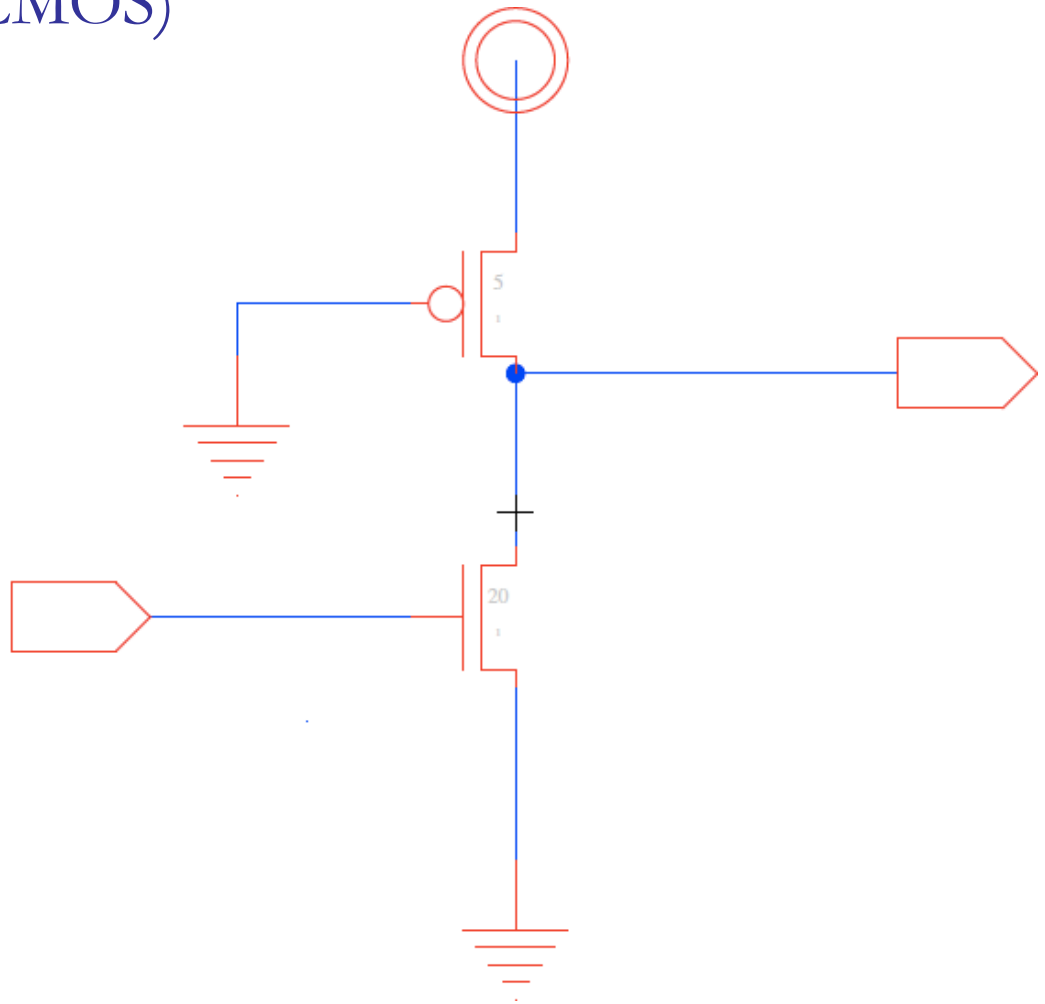
- What is impact of increasing noise margin?
  - On size
  - On input capacitance





Size for $R_0/2$ drive? (Preclass 2)

- How do we size for $R_0/2$ drive?
  - (assume $R_{0p}=R_{0n}$ for CMOS)



Size for $R_0/2$ drive? (Preclass 2)

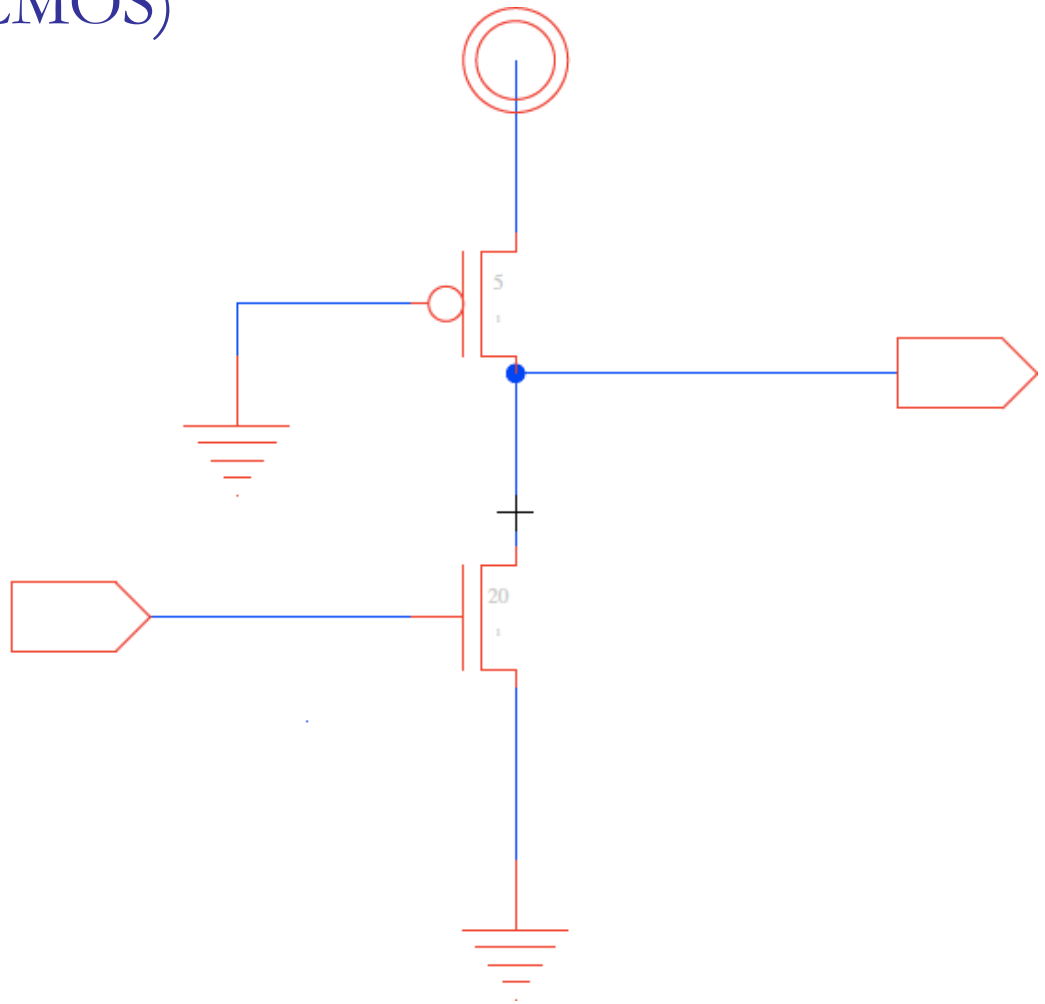
- How do we size for $R_0/2$ drive?
  - (assume $R_{0p}=R_{0n}$ for CMOS)

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$

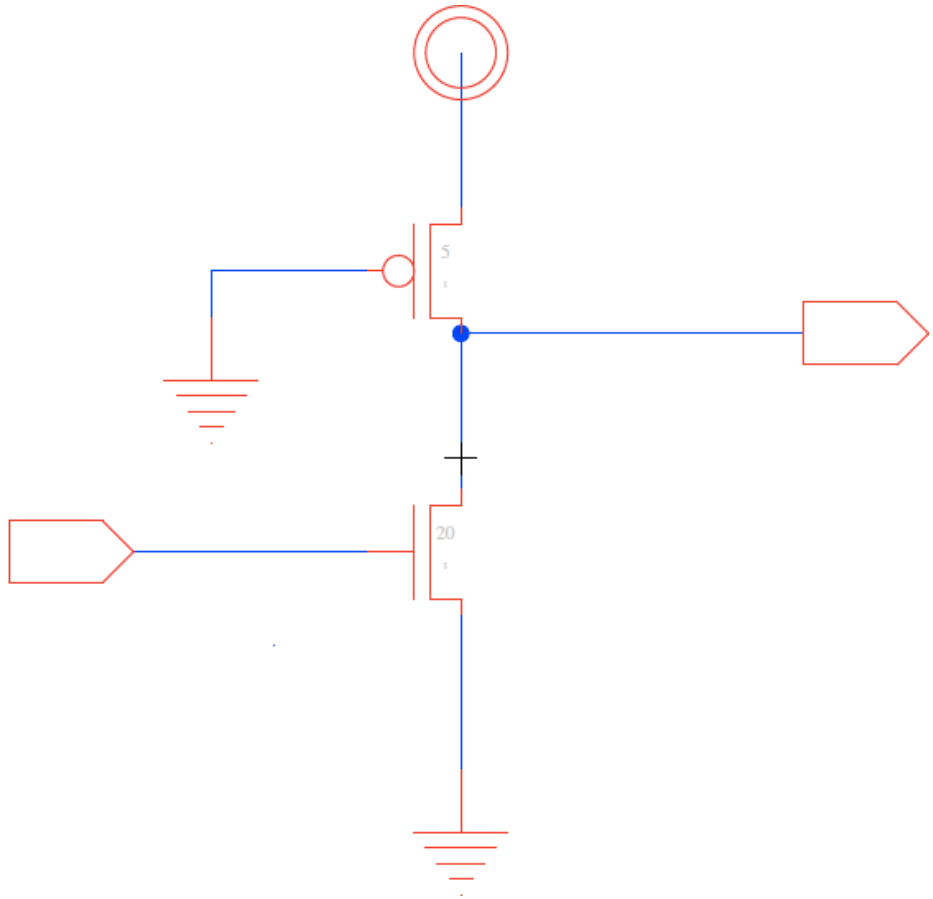
$$W_n > 8W_p$$

$$\Rightarrow W_n = 16$$



Static Power

- I_{static} ?
- Input low-Output high?
  - I_{leak}
- Input high-Output low?
  - I_{pmos_on}
  - $\sim V_{dd}/(R_0/2)$ -- for our sample case



Total Power

- $P_{tot} \approx a(C_{load}+2C_{sc})V^2f$

Total Power

- $P_{tot} \approx a(C_{load}+2C_{sc})V^2f$
  $+p(V_{out}=low)V^2/R_{pon}$
  $+p(V_{out}=high)VI'_s(W/L)e^{-Vt/(nkT/q)}$

$p(V_{out}=low)$ – probability the output is low

$p(V_{out}=high)$ – probability the output is high

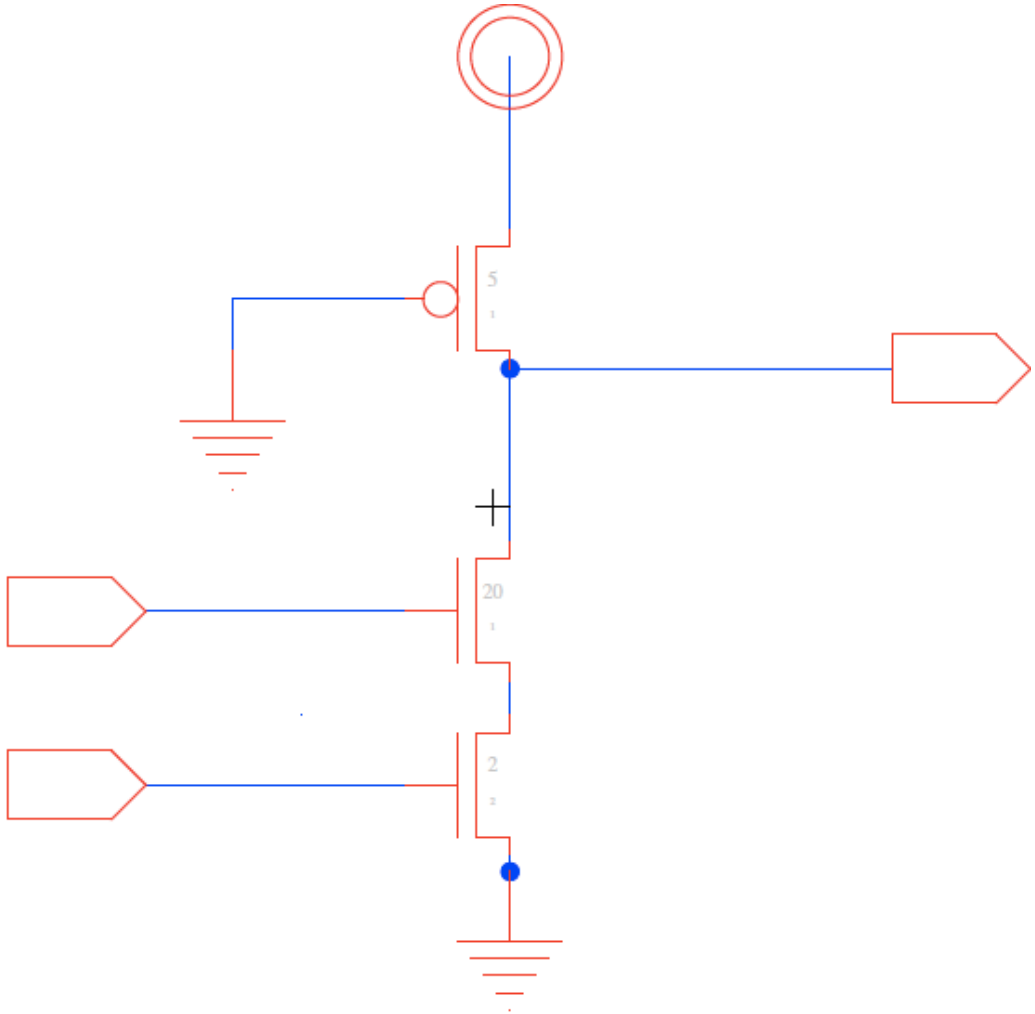
$p(V_{out}=high)=1-p(V_{out}=low)$

Compare Static CMOS

For $R_{drive}=R_0/2$ inverter (assume $R_{0p}=R_{0n}$ for CMOS)

- Total Transistor Width?
- Input capacitance load?

Size for $R_0/2$ drive? (Preclass 2)



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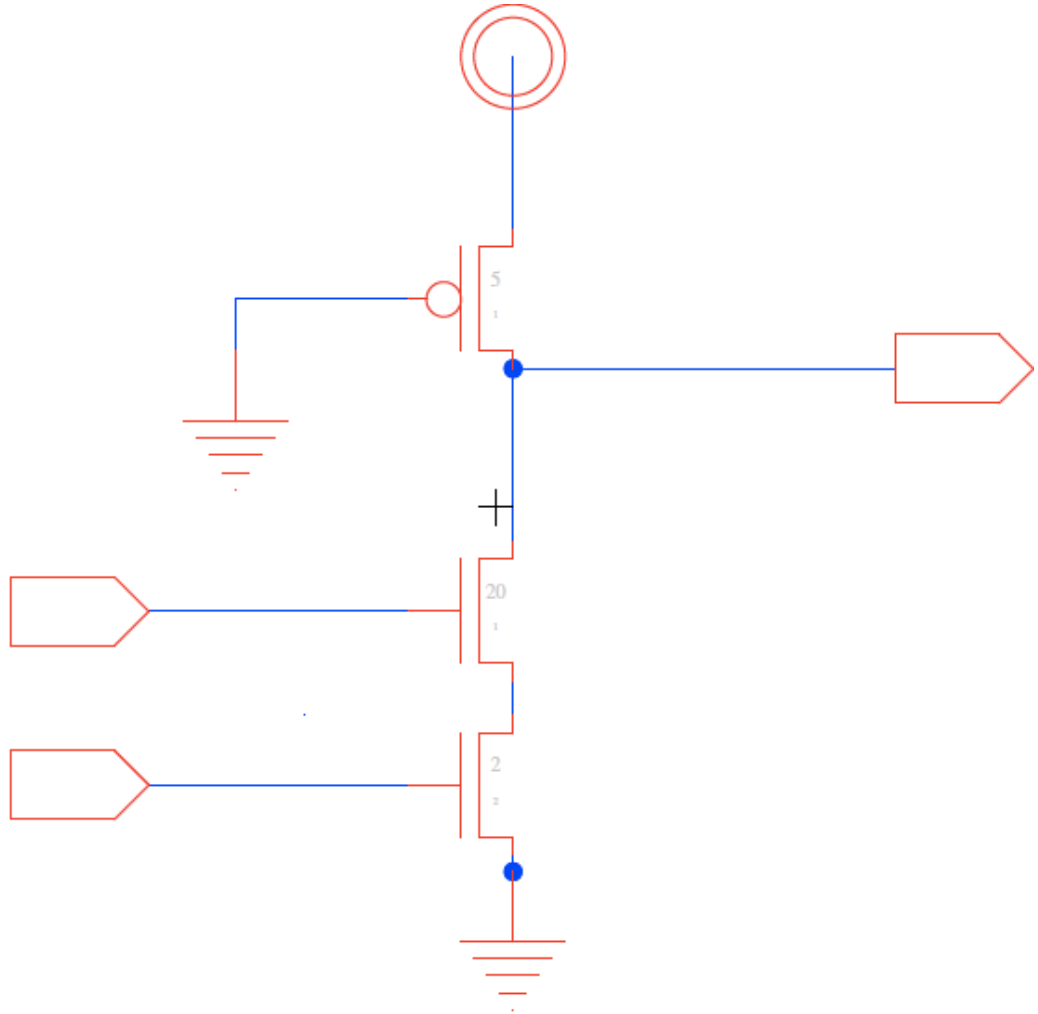


Size for $R_0/2$ drive? (Preclass 2)

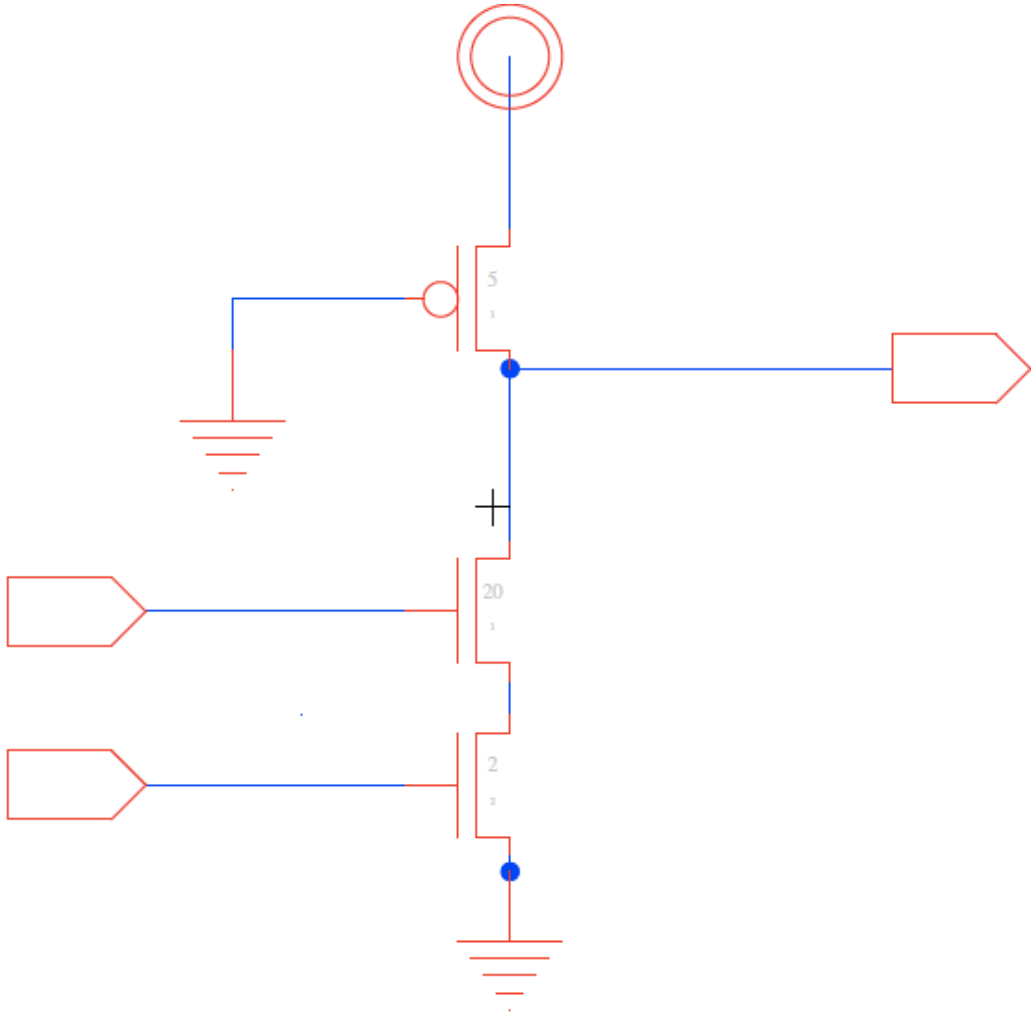
$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$

$$R_{drive,pdn} = \frac{2R_0}{W_n} = \frac{R_0}{W_n/2}$$

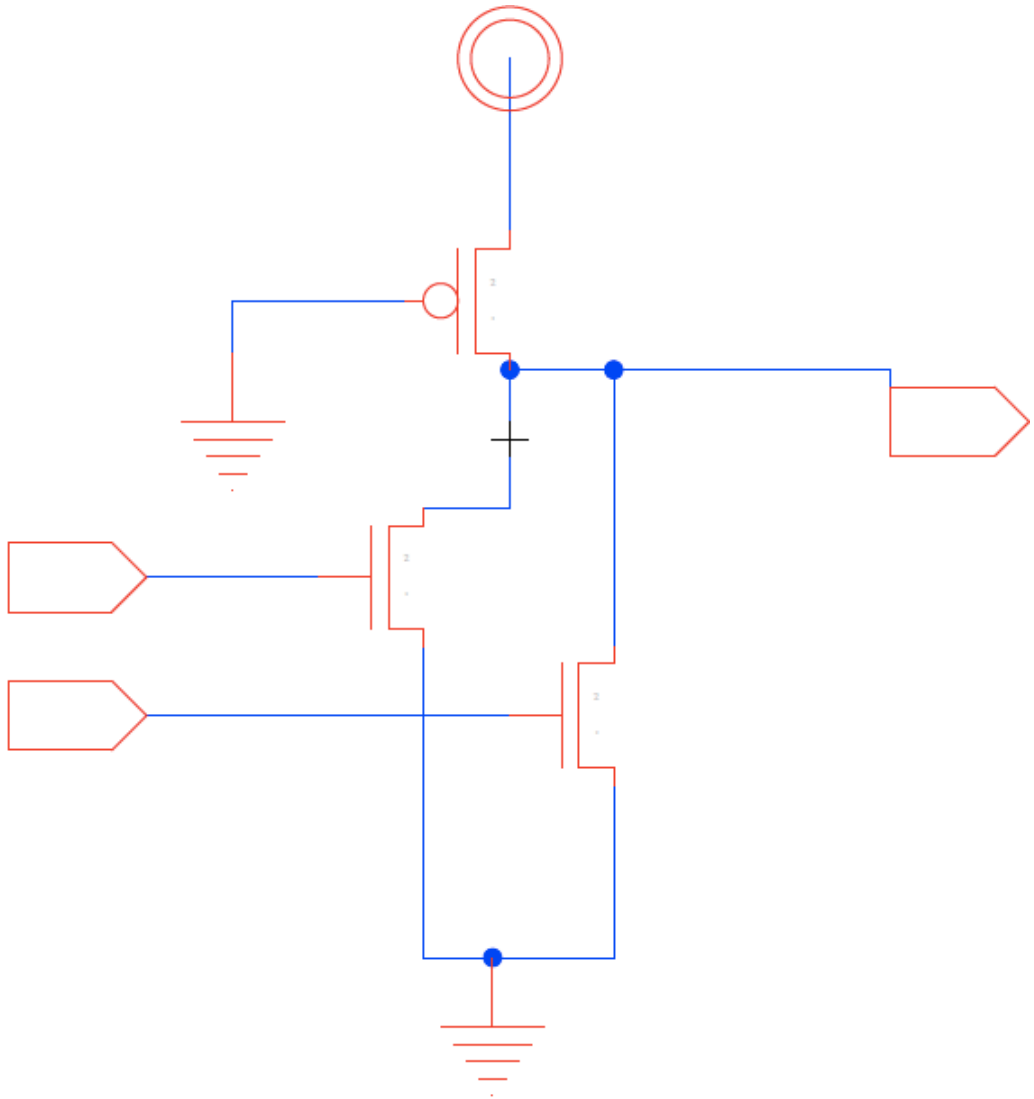
$$W_n/2 > 8W_p$$

$$\Rightarrow W_n = 32$$



Size for $R_0/2$ drive? (Preclass 2)

- 2-input nor?



Size for $R_0/2$ drive? (Preclass 2)

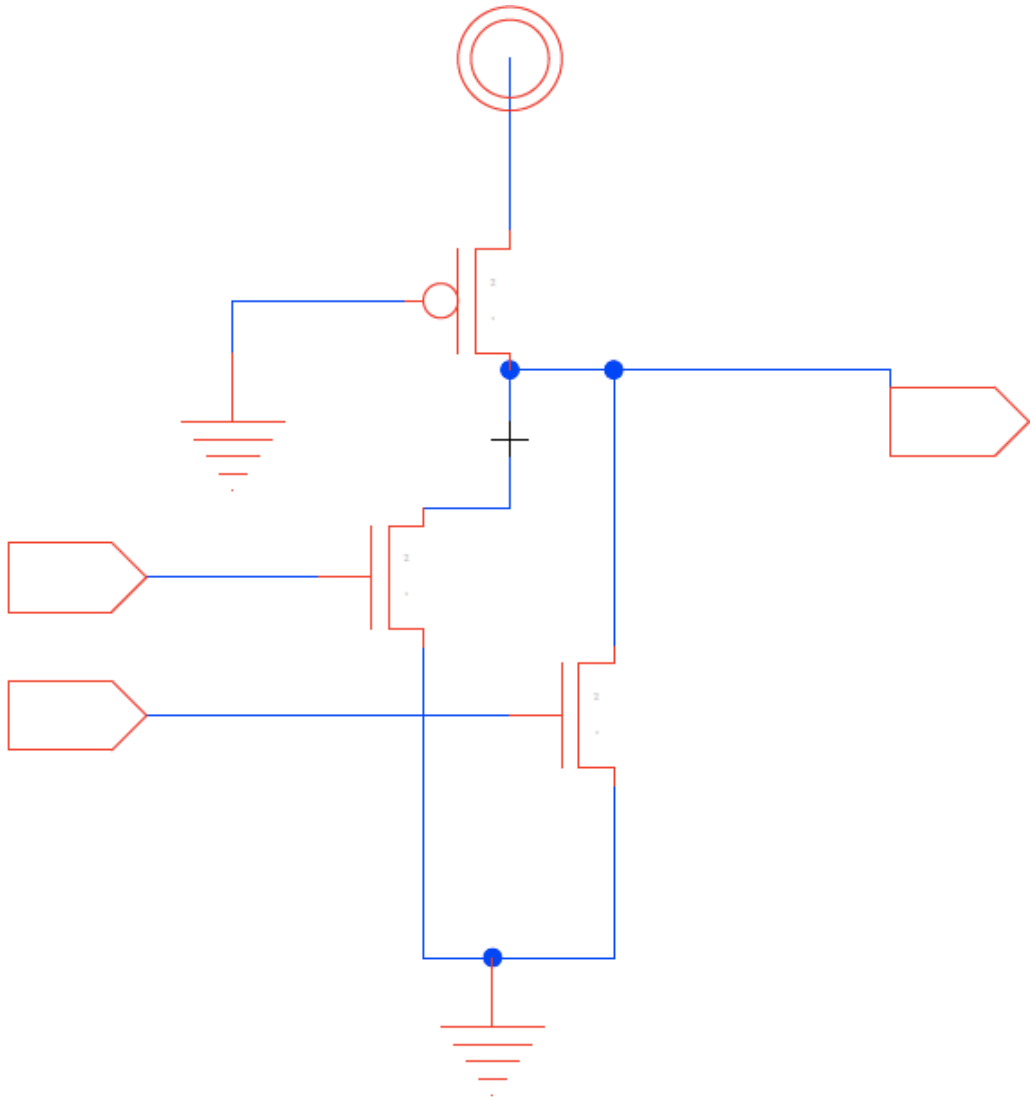
- 2-input nor?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{2R_o}{W_p} = \frac{R_o}{2}$$

$$\Rightarrow W_p = 2$$

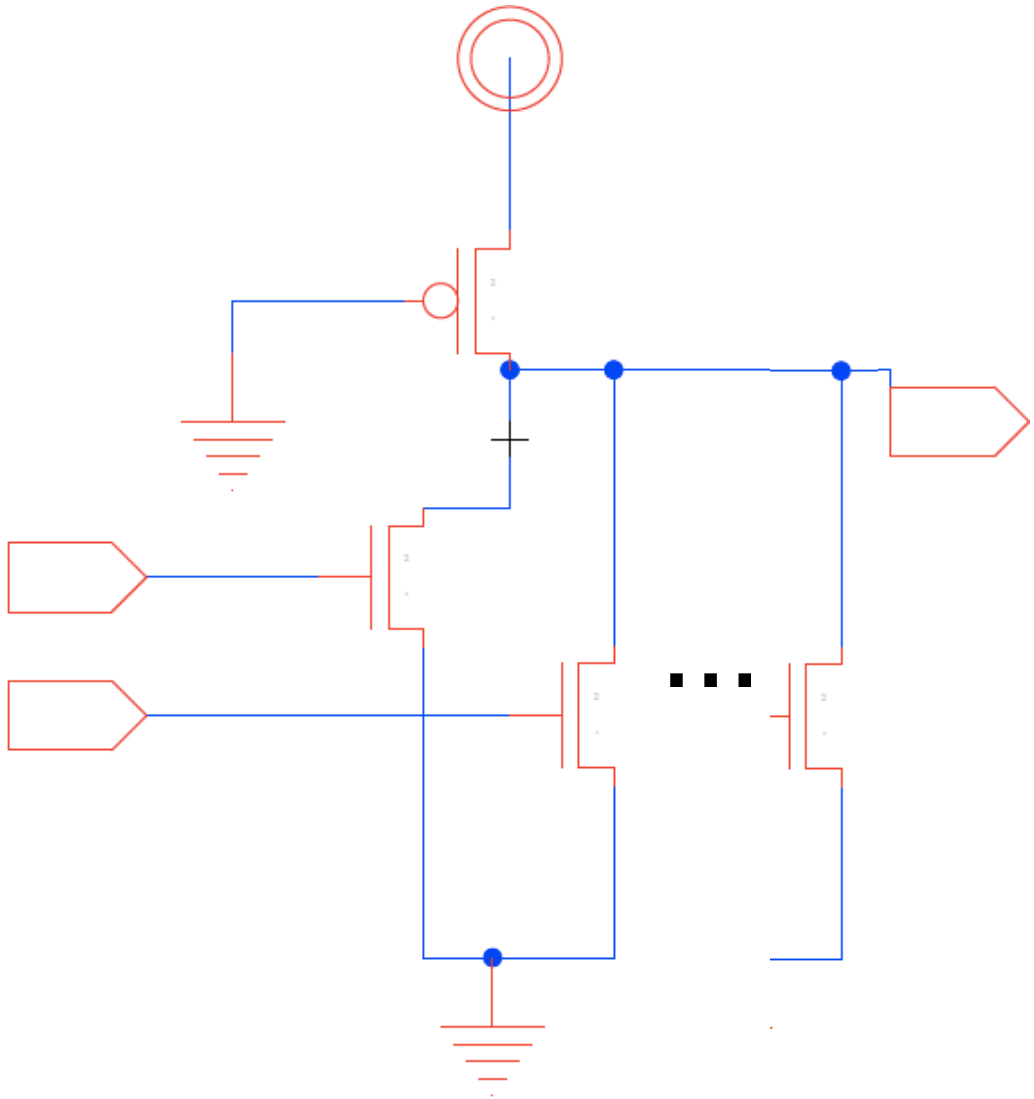
$$W_n > 8W_p$$

$$\Rightarrow W_n = 16$$



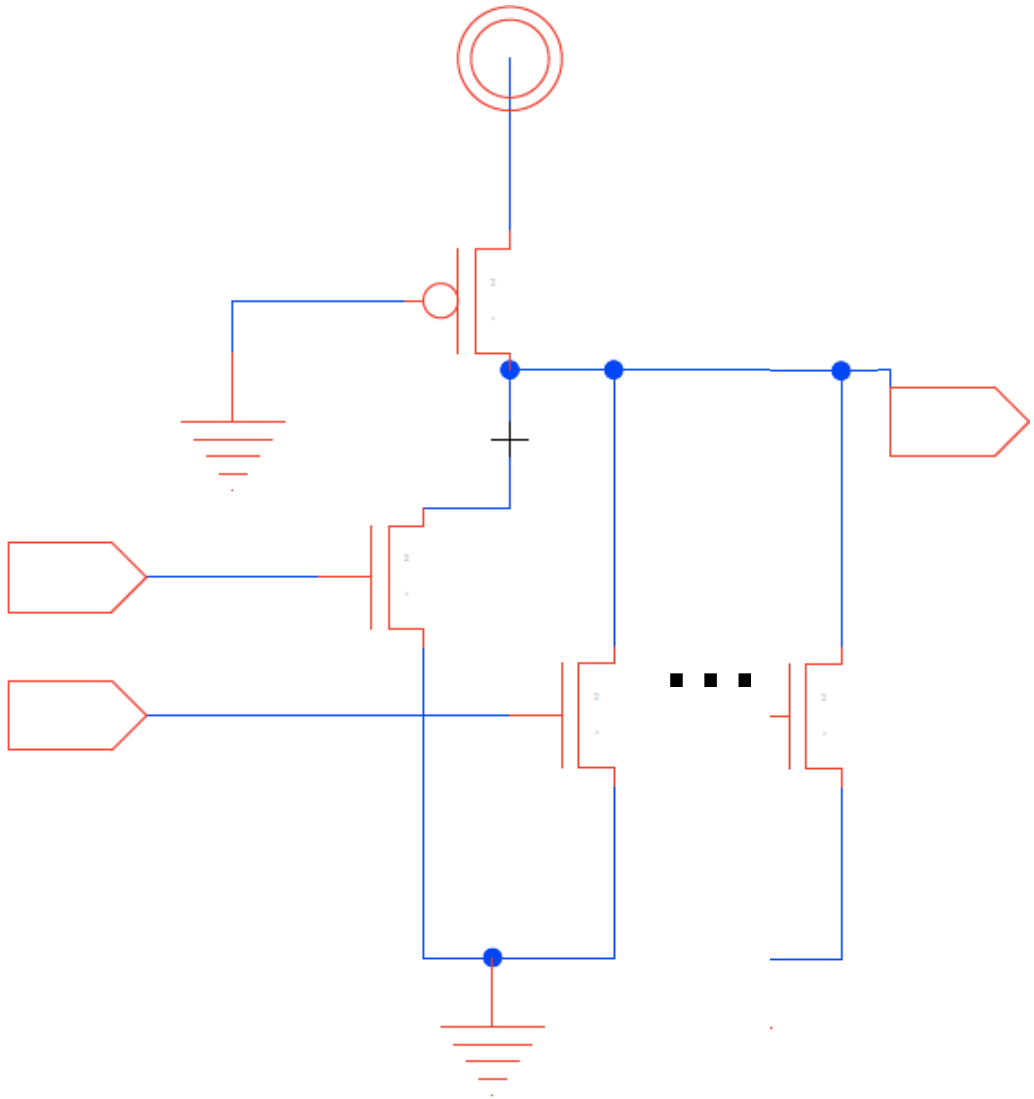
Size for $R_0/2$ drive? (Preclass 3)

- k-input nor?
- What is the input capacitance for k-input nor?

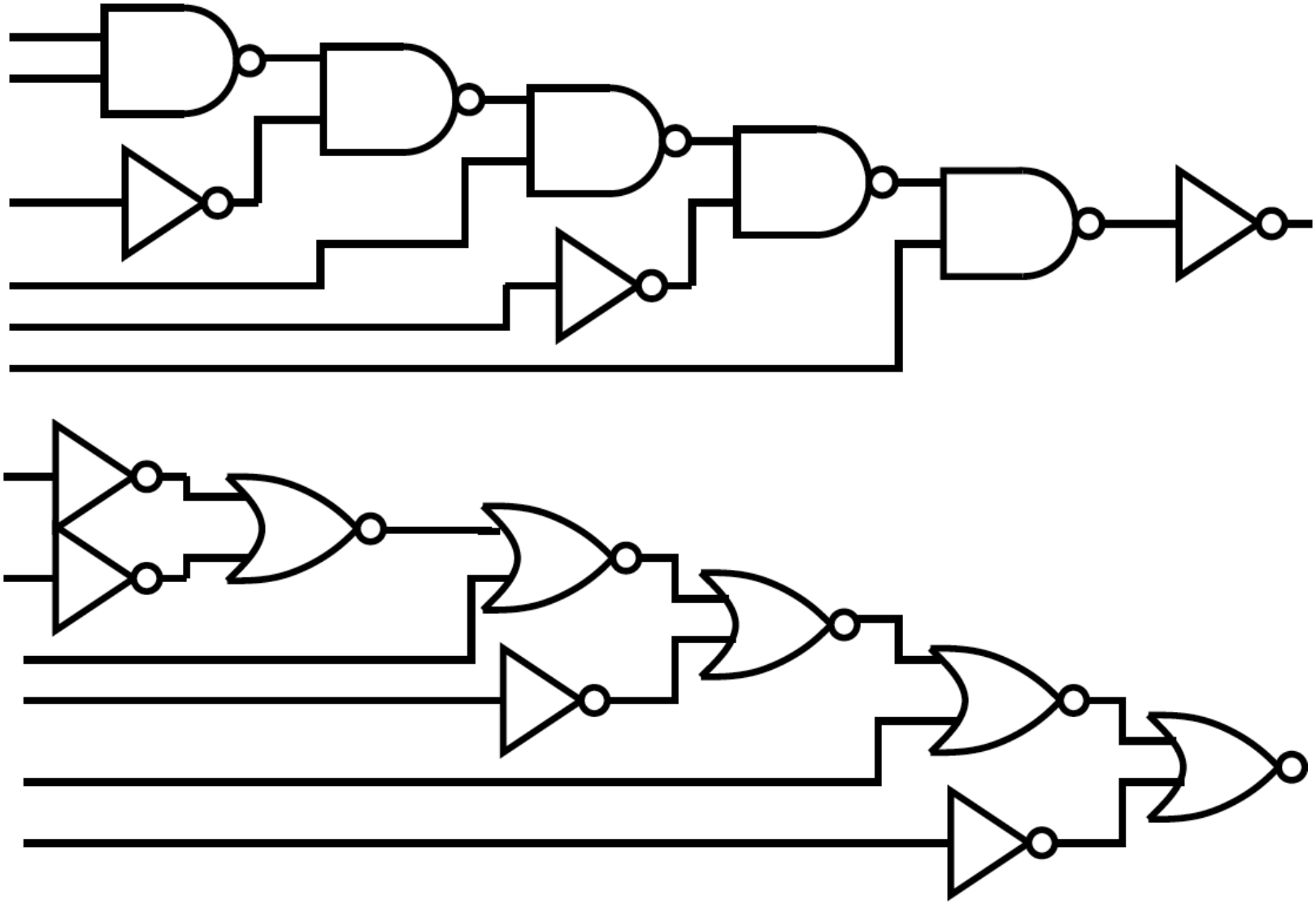


Size for $R_0/2$ drive? (Preclass 4)

- k-input nor?
- What is the input capacitance for k-input nor?
- For what k does ratioed gate have lower C_{in}?



Which implementation is faster in ratioed logic?



Ideas

- There are other logic disciplines
- You have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates non-leakage static power in one input case

Design Space Exploration

Design Problem

- Function: Identify equivalence of two 32bit inputs
- Optimize: Minimize total energy
- Assumptions: Match case uncommon
  - Ie. Most of the time, the inputs won't be matched

- Deliberately focus on Energy to complement project
  - …but will still talk about delay

Last page of preclass

Idea: Design Space Explore

- Identify options
  - All the knobs you can turn
- Explore space systematically
- Formulate continuum where possible
  - i.e. formulate trends and tradeoffs quantitatively

Problem Solvable (preclass 1)

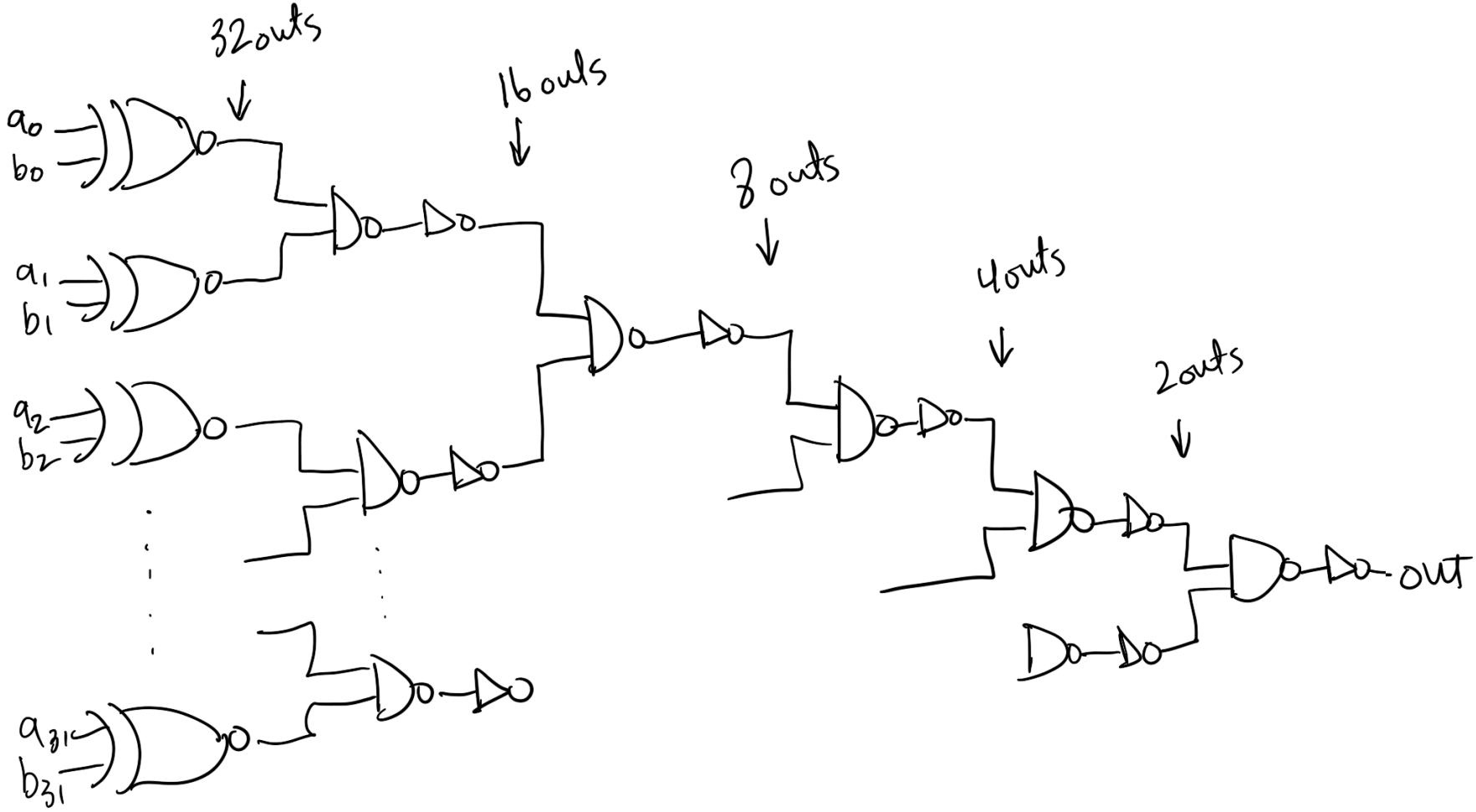
- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization

- How do we decompose the problem?

Problem Solvable (preclass 2)

- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization
- How do we decompose the problem?
- What look like built out of nand2 gates and inverters?

Nand2 and inverter implementation



Single Gate Match Condition (preclass 3)

- Design a single gate for match comparison

Total Power

- Static CMOS:
  - $P_{tot} \approx a(C_{load}+2C_{sc})V^2f+VI'_s(W/L)e^{-Vt/(nkT/q)}$
- Ratioed Logic:
  - $P_{tot} \approx a(C_{load}+2C_{sc})V^2f$

    $+p(V_{out}=low)V^2/R_{pon}$

    $+(1-p(V_{out}=low))VI'_s(W/L)e^{-Vt/(nkT/q)}$
- What can we do to reduce power?

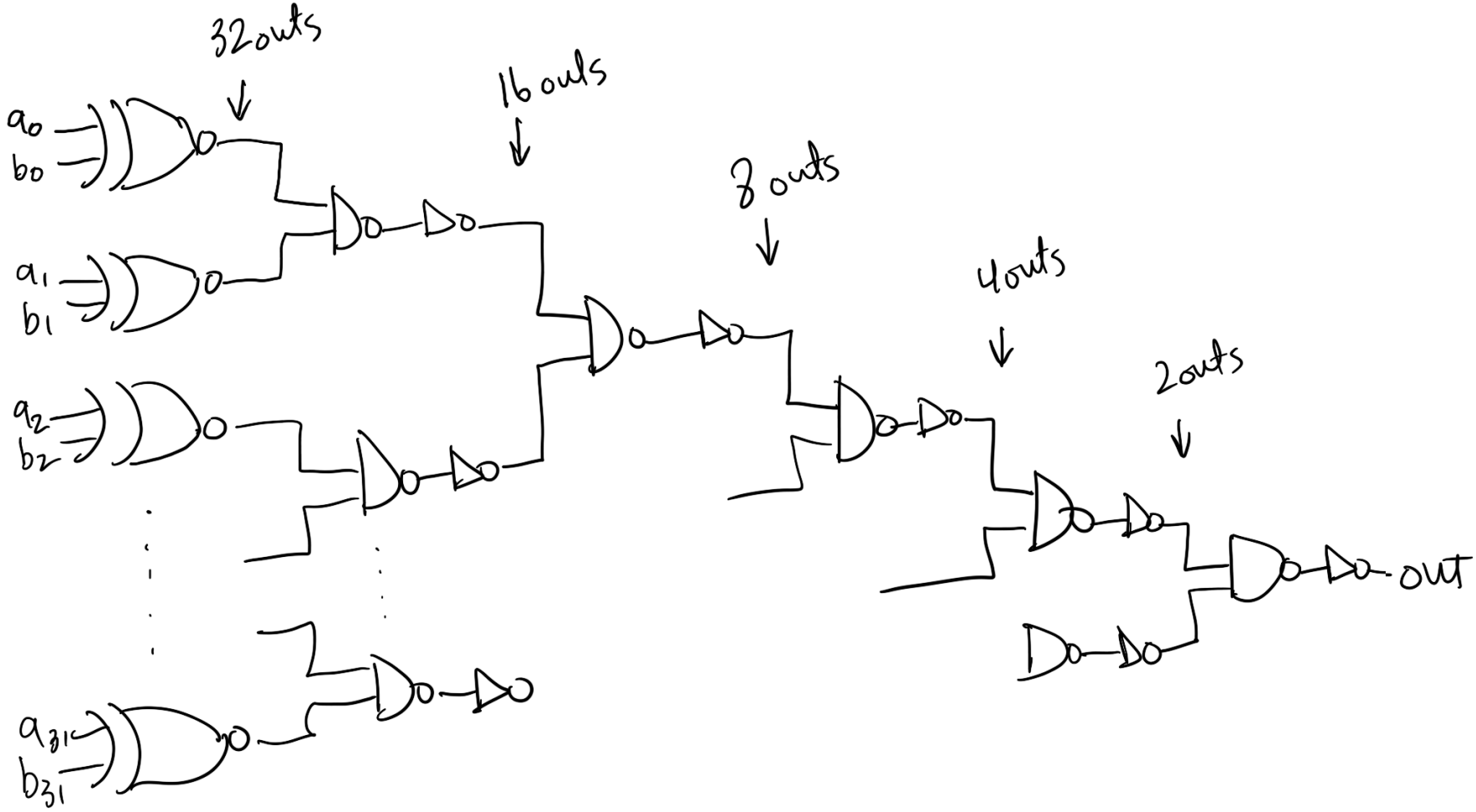
Knobs (preclass 4)

- What are the options and knobs we can turn?

Design Space Dimensions

- Topology
  - (A) Gate choice, logical optimization
  - (B) Fanin, fanout, (C) Serial vs. parallel
- Gate style / logic family
  - (D) CMOS, Ratioed (N load, P load)
- (E) Transistor Sizing
- (F) Vdd
- (G) Vth

Gate



Gate

- (B) High fanin?

Gate

- (C) Serial-Parallel?

(D) Logic Family

- Considerations for each logic family?
  - CMOS
  - Ratioed with PMOS load
  - Ratioed with NMOS load

- Ratioed Logic
  - Reduced C_{loads} result in lower switching power (P_{dyn} ↓)
  - Increased static power

(E) Sizing

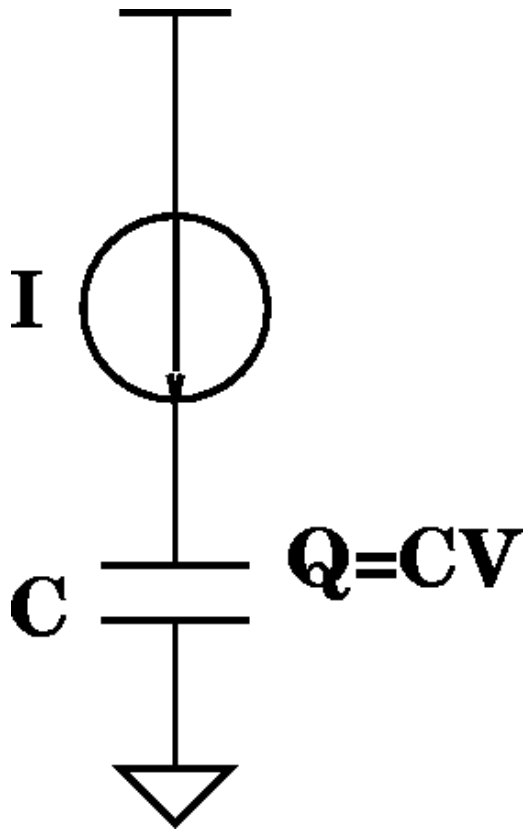
- How do we want to size gates?
  - Sizing transistors up will reduce delay →
    - Reduces short circuit power

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

    - Increases dynamic power

(F) Reduce Vdd

- What happens as reduce V?
  - Energy?
    - Dynamic ↓
    - Static ↓
  - Switching Delay? ↑



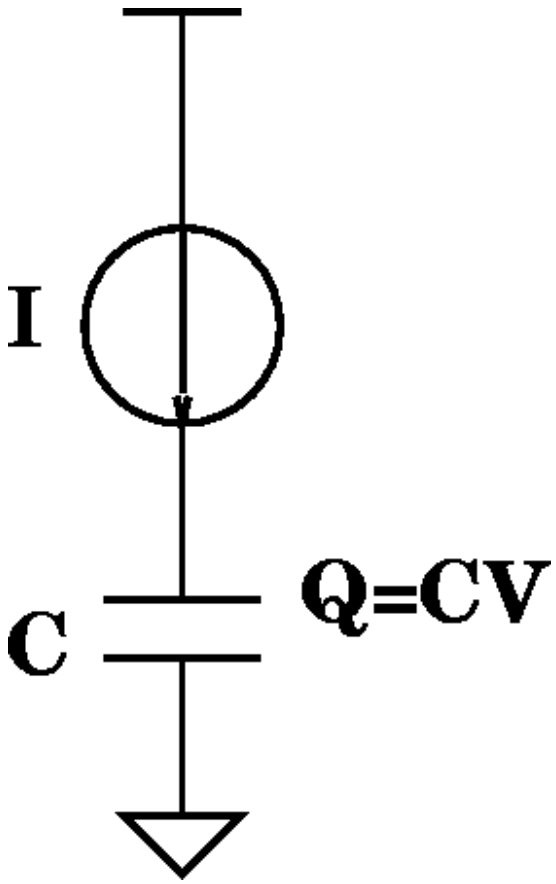
- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?
- $\tau_{gd} \propto 1/V$

- Limit on Vdd?

(G) Increase V_{th}?

- What is impact of increasing threshold on
  - Dynamic Energy? ↓
  - Leakage Energy? ↓
  - Delay? ↑

- $\tau_{gd}=Q/I=(CV)/I$
- $I_{ds}=(\nu_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$



Ideas

- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs
  - …don't over-tune

Admin

- Project out now
- Milestone due 10/22
  - baseline is a bare minimum
    - Really should be into exploring optimizations to try
- Final report due 10/29
  - Final report should be single document typed with all figures, schematics, graphs, equations, etc. computer generated. Anything handwritten will not be looked at. Anything outside of that document won't be looked at.
  - YOUR OWN WORK!
    - You should understand everything you turn in, and I reserve the right to test you on that