ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 19: October 22, 2021

Design Space Exploration (con't)

Pass Transistor Logic

Design Space Exploration

Design Problem

- Function: Identify equivalence of two 32bit inputs
- Optimize: Minimize total energy
- Assumptions: Match case uncommon
  - Ie. Most of the time, the inputs won't be matched

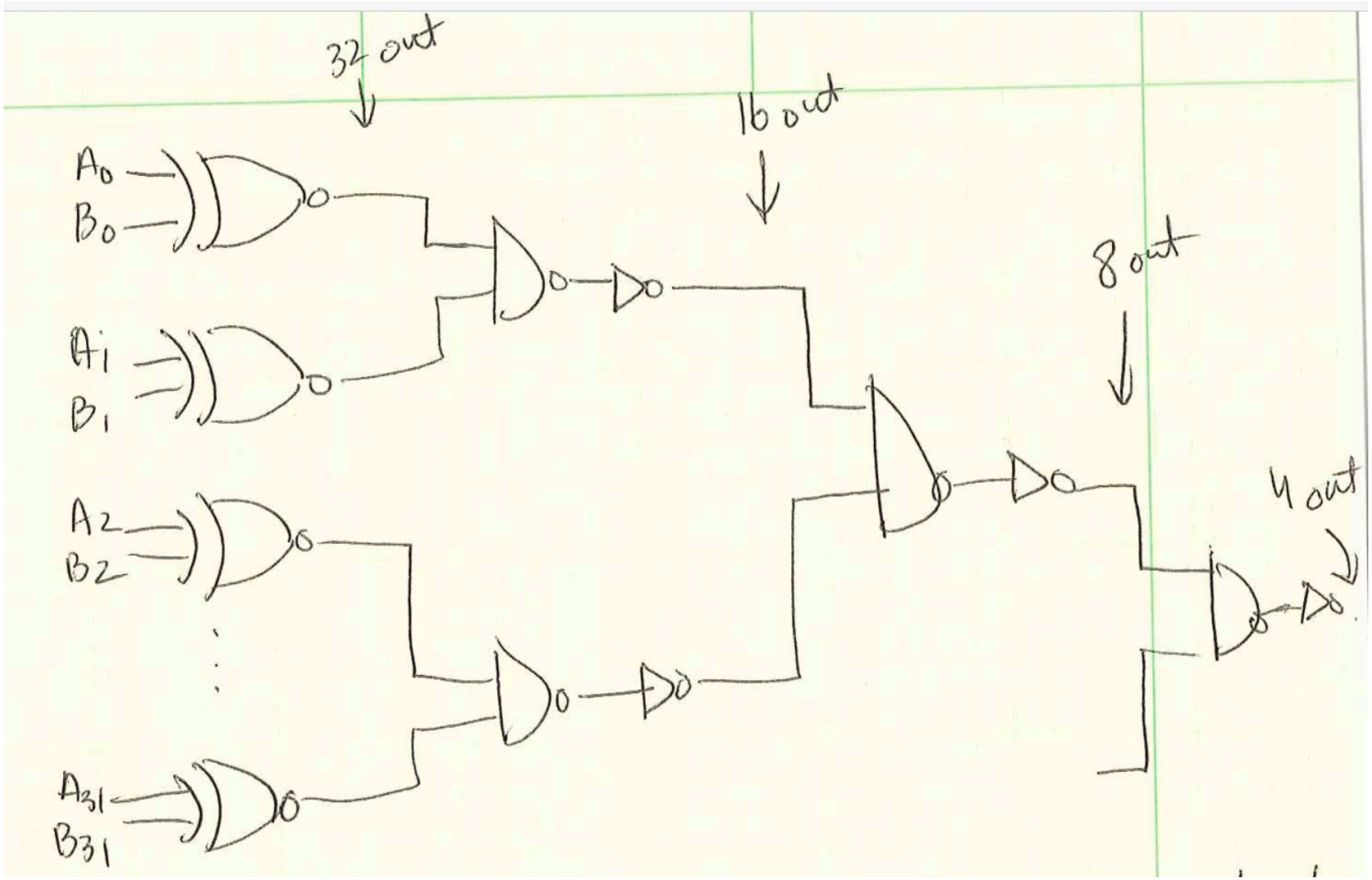
- Deliberately focus on Energy to complement project
  - …but will still talk about delay

Design Space Dimensions

- Topology
  - (A) Gate choice, logical optimization
  - (B) Fanin, fanout,
  - (C) Serial vs. parallel
    - Chain vs. tree
- Gate style / logic family
  - (D) CMOS, Ratioed (N load, P load), Pass (coming soon)
- (E) Transistor Sizing
- (F) Vdd
- (G) Vth

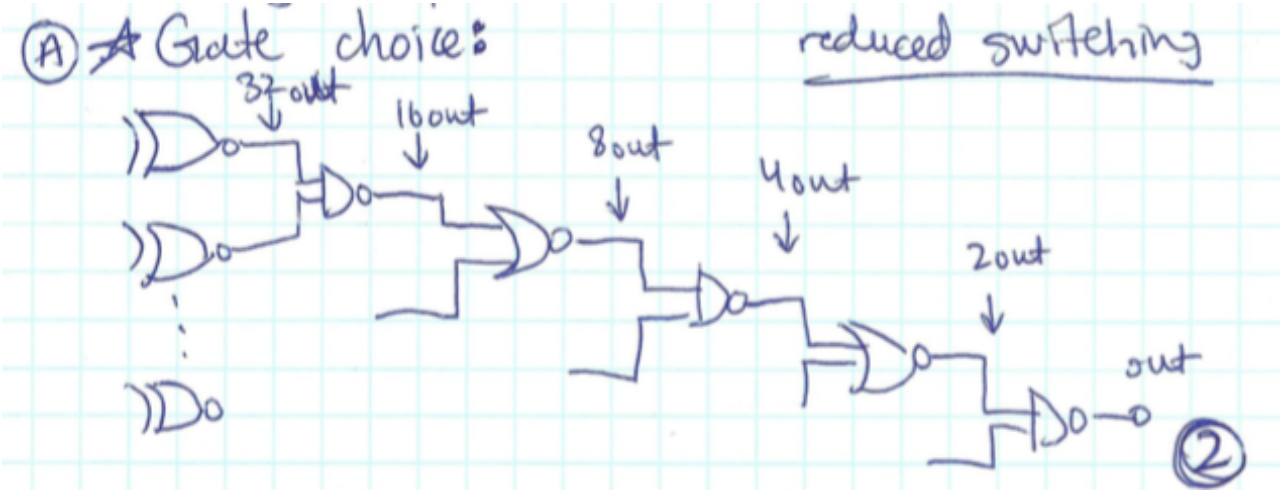
Gate Choice

- (A) What gates might we build?



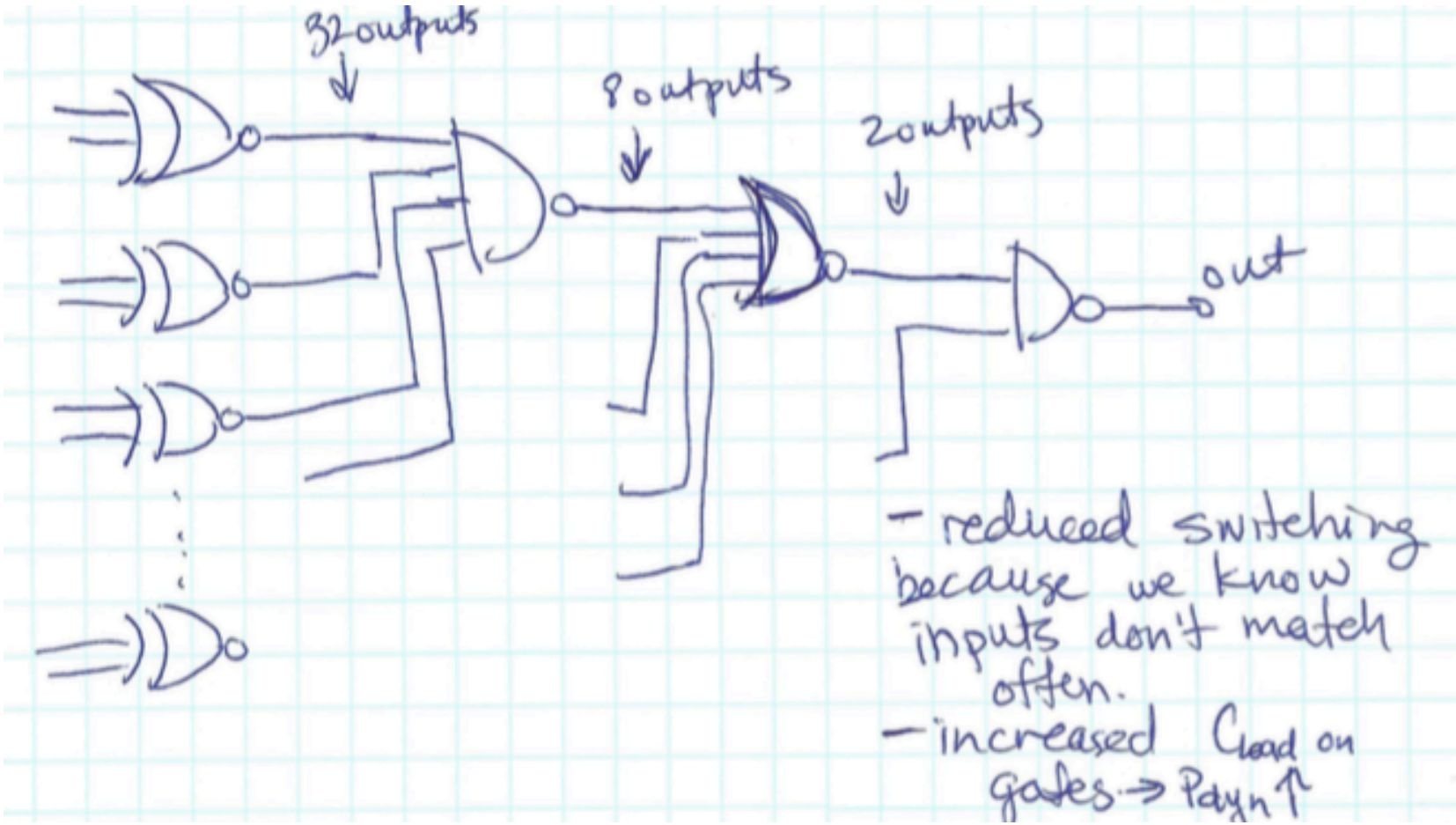
Gate Choice

- (A) What gates might we build?



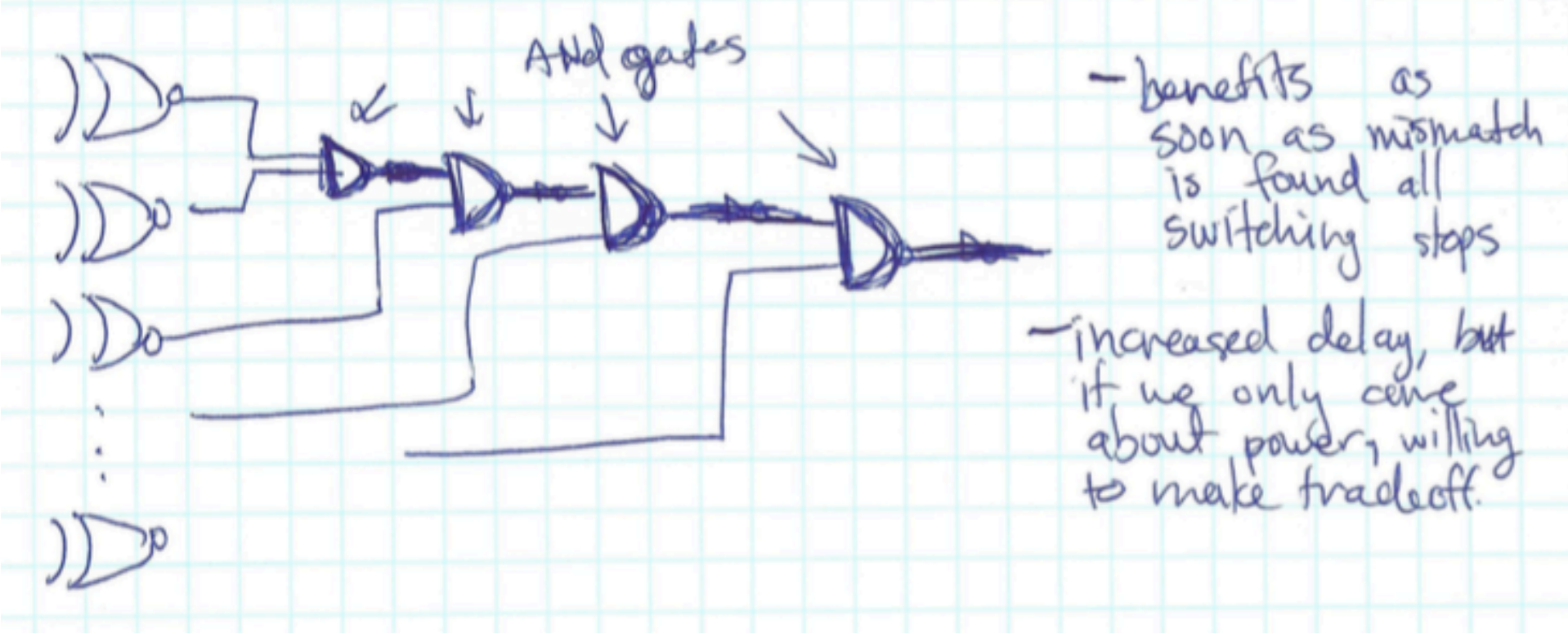
Gate Fan-in

- (B) High fan-in?



Gate Topology

- (C) Serial-Parallel?



(D) Logic Family

- Considerations for each logic family?
  - CMOS
  - Ratioed with PMOS load
  - Ratioed with NMOS load

- Ratioed Logic
  - Reduced C_{loads} result in lower switching power (P_{dyn} ↓)
  - Increased static power

(E) Sizing

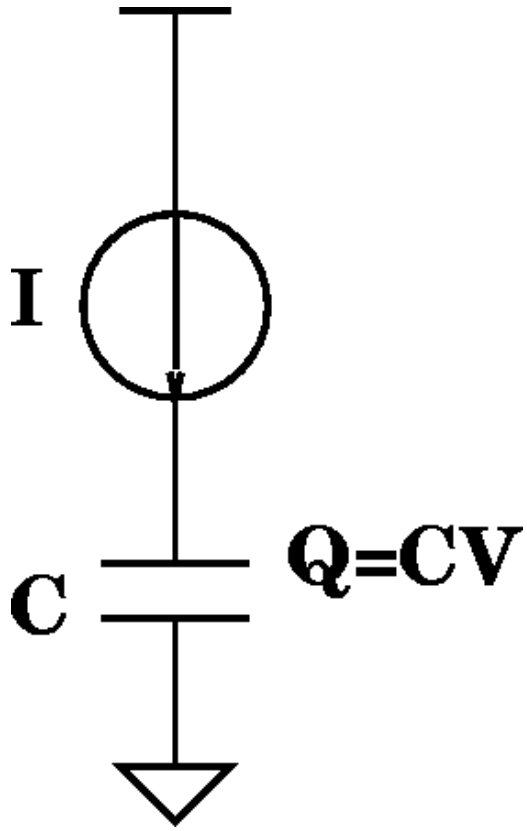
- How do we want to size gates?
  - Sizing transistors up will reduce delay →
    - Reduces short circuit power

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

    - Increases dynamic power

(F) Reduce Vdd

- What happens as reduce V?
  - Energy?
    - Dynamic ↓
    - Static ↓
  - Switching Delay? ↑



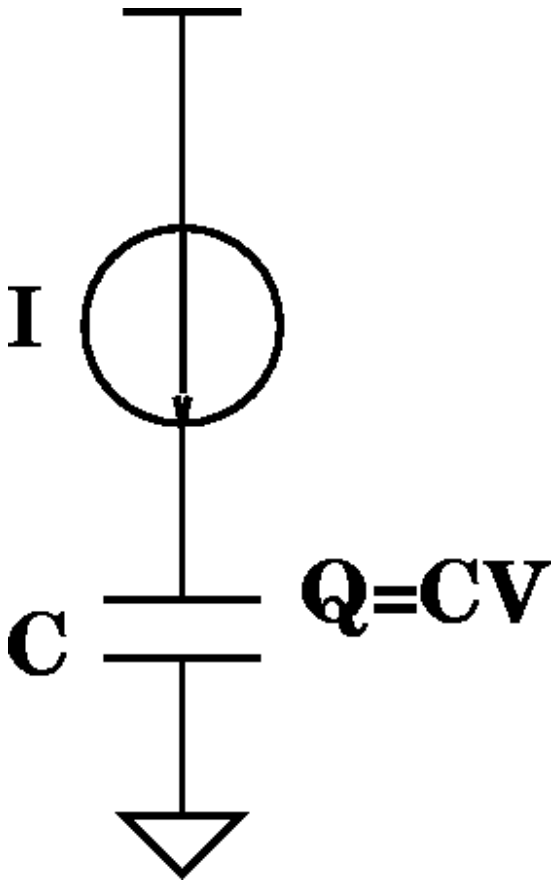
- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?
- $\tau_{gd} \propto 1/V$

- Limit on Vdd?

(G) Increase V_{th}?

- What is impact of increasing threshold on
  - Dynamic Energy? ↓
  - Leakage Energy? ↓
  - Delay? ↑

- $\tau_{gd}=Q/I=(CV)/I$
- $I_{ds}=(\nu_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$



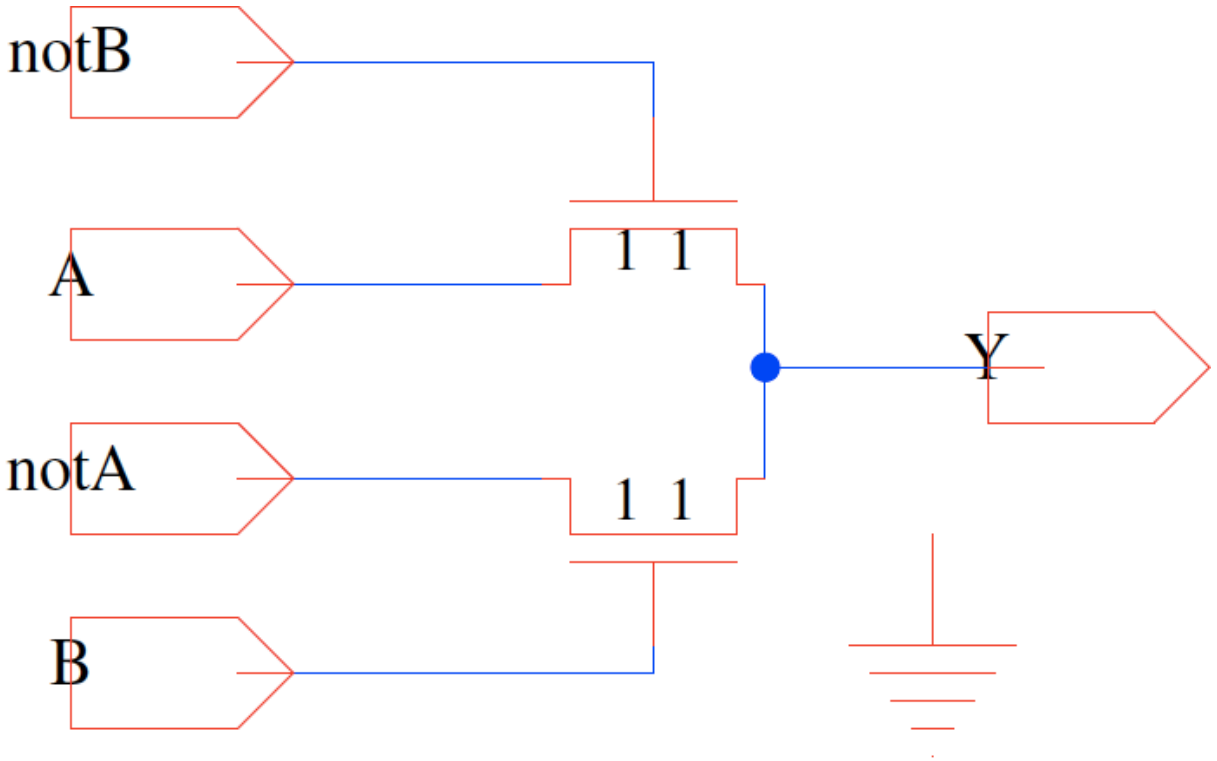
Ideas

- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs
  - …don't over-tune

Pass Transistor Logic

Pass Transistor Logic (Preclass 1)

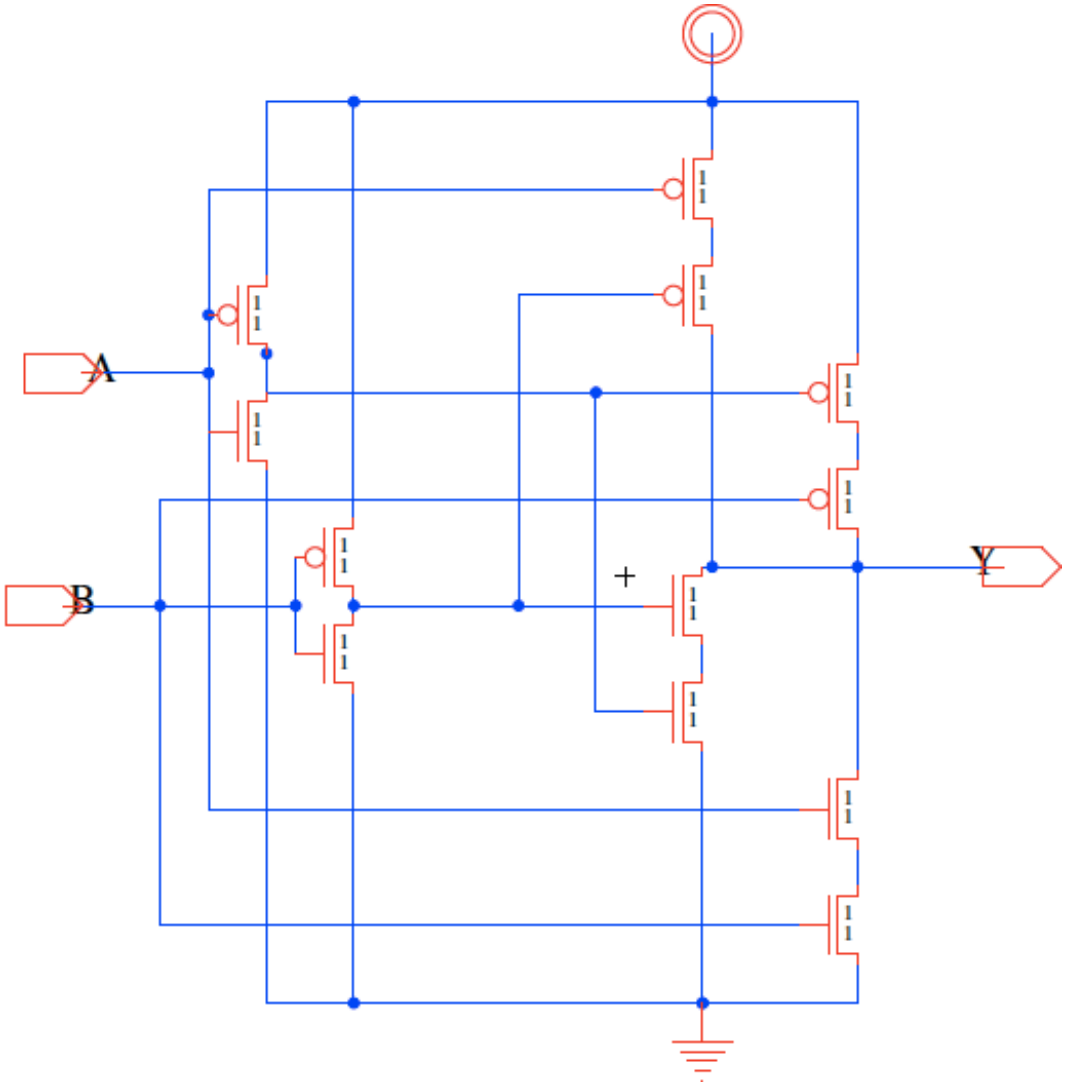
- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

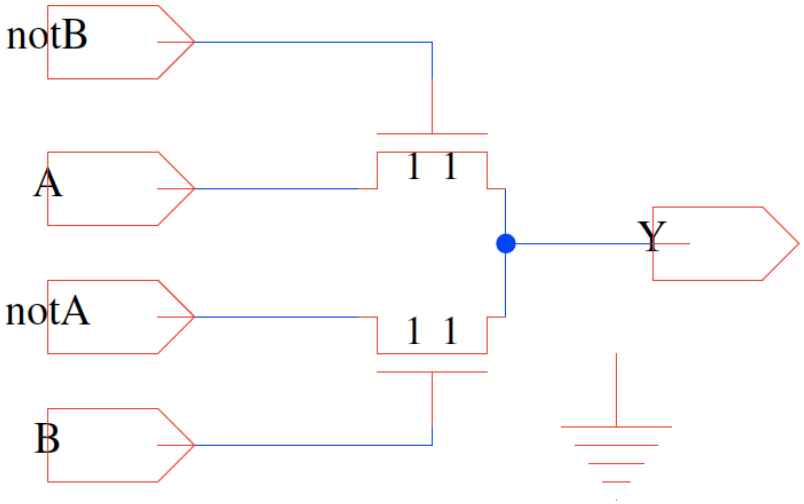
Identify Function (Preclass 2)

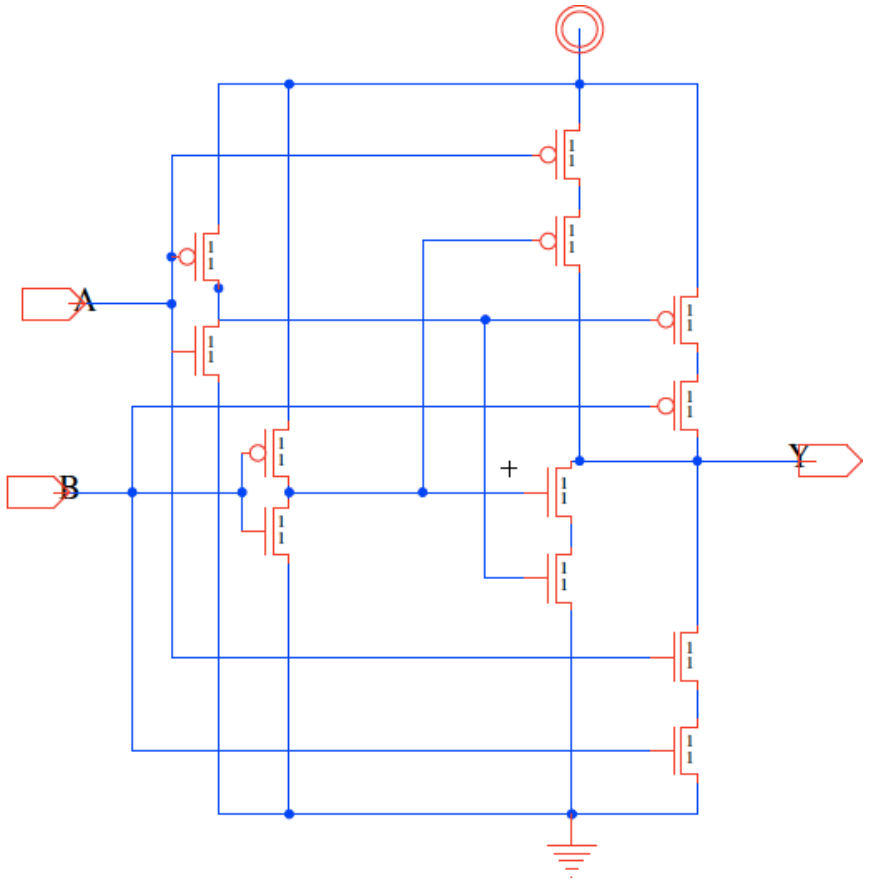
- What function is this?



Area

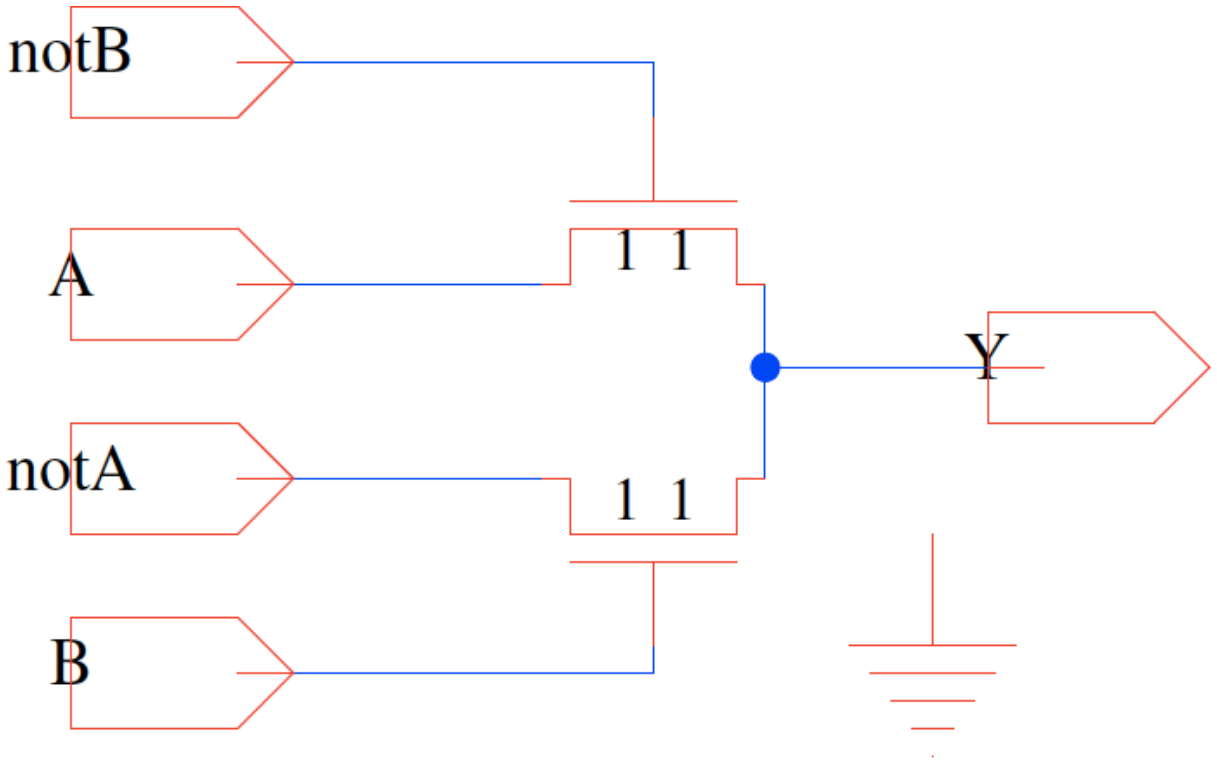
- Compare PT with CMOS circuit?





Output

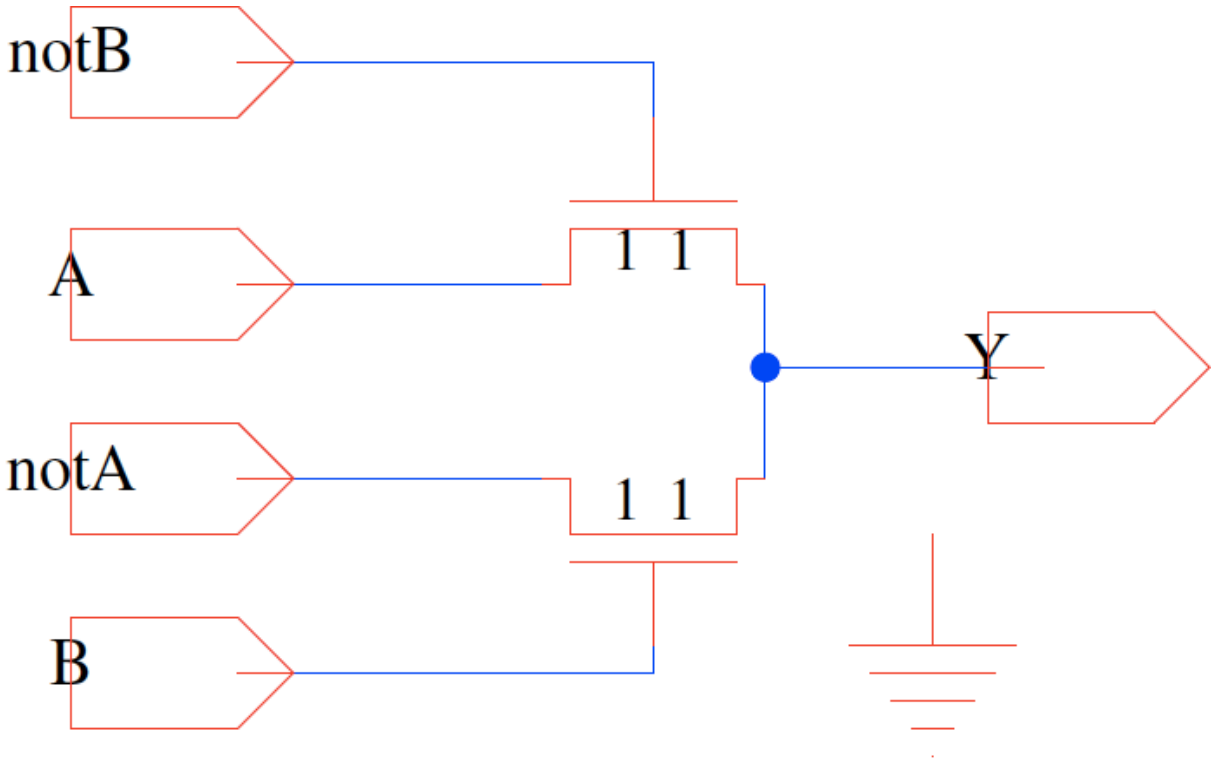
- Is this a regenerating/restoring gate?



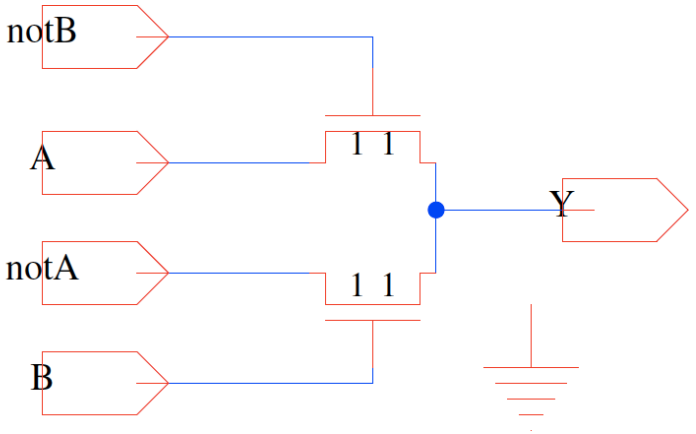
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

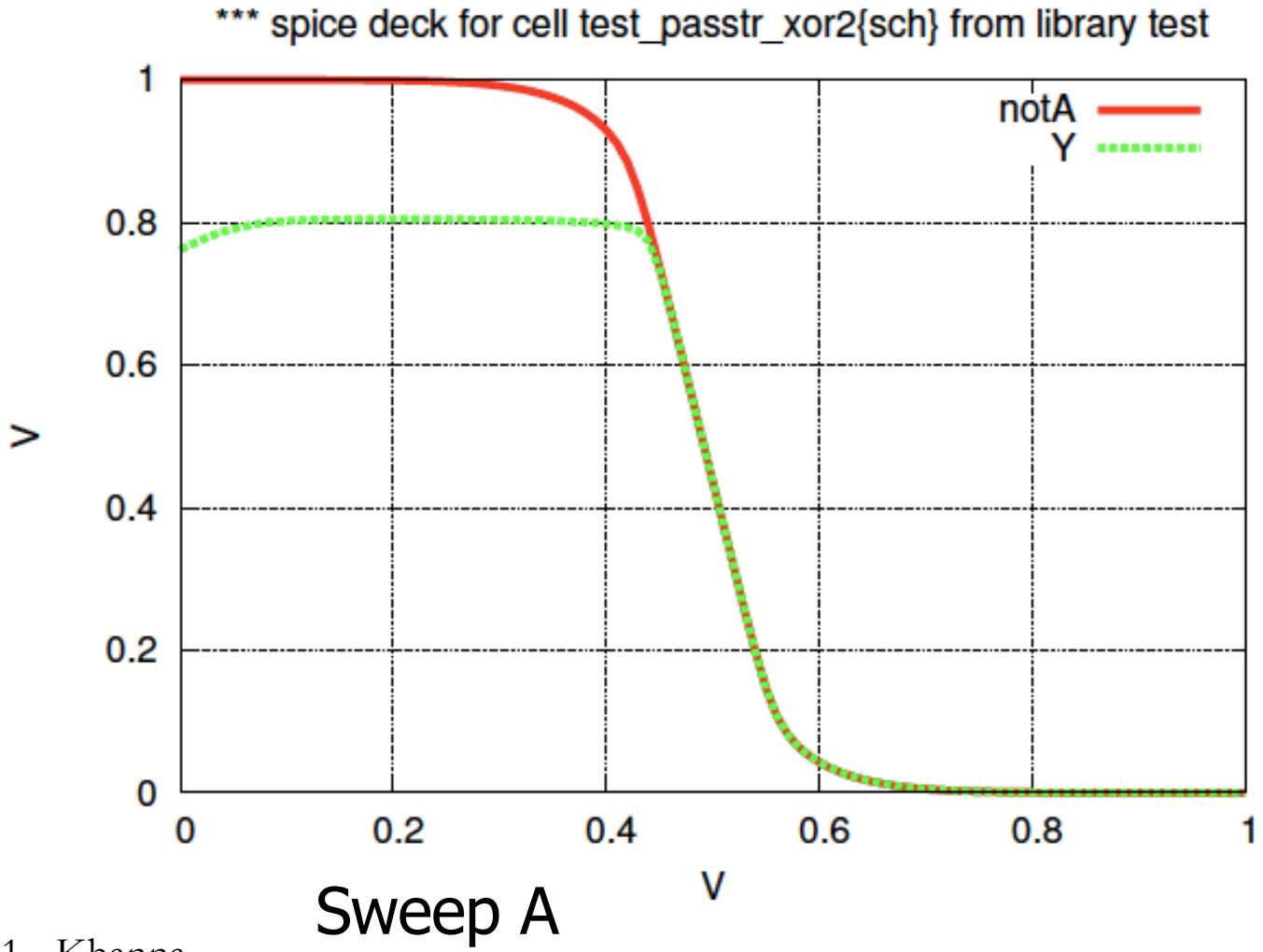
Output

- What does output look like (DC transfer)?
  - (B=1, notB=0, sweep A, notA=CMOS inv(A))



Pass TR transfer (B=1)

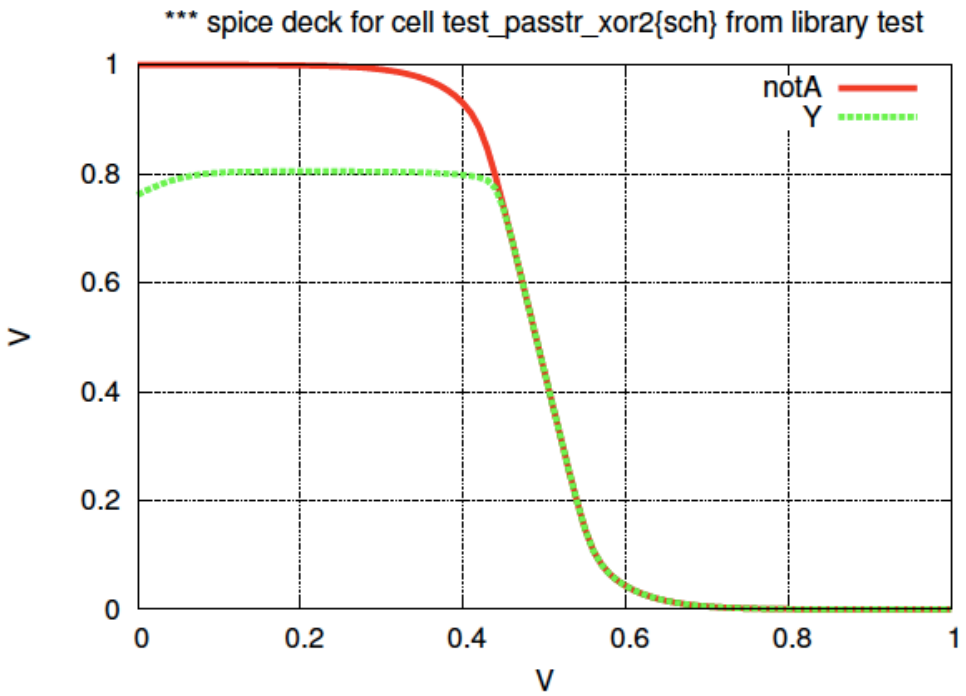


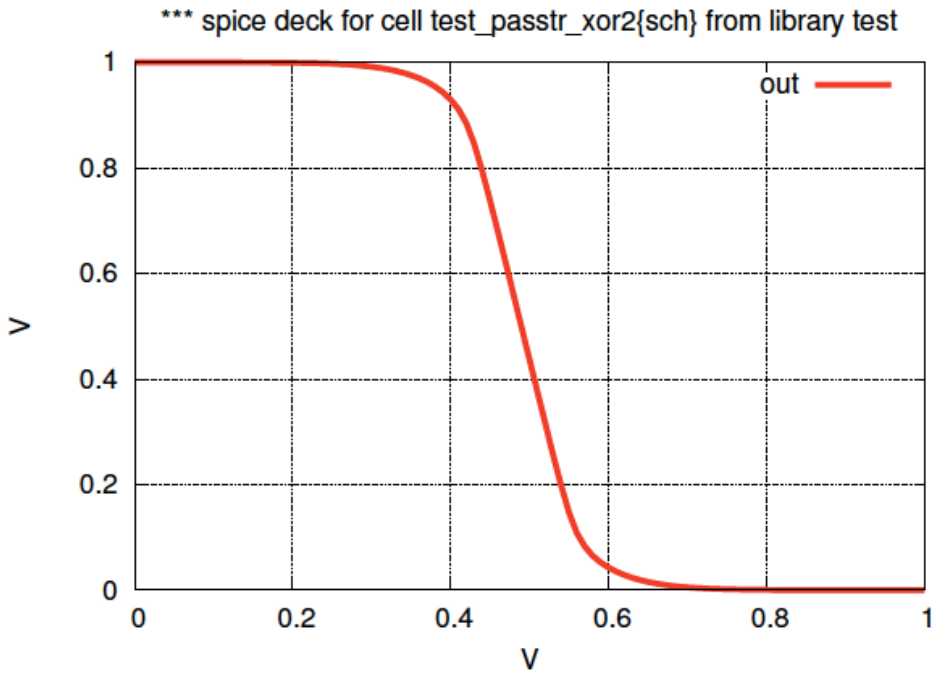


Sweep A

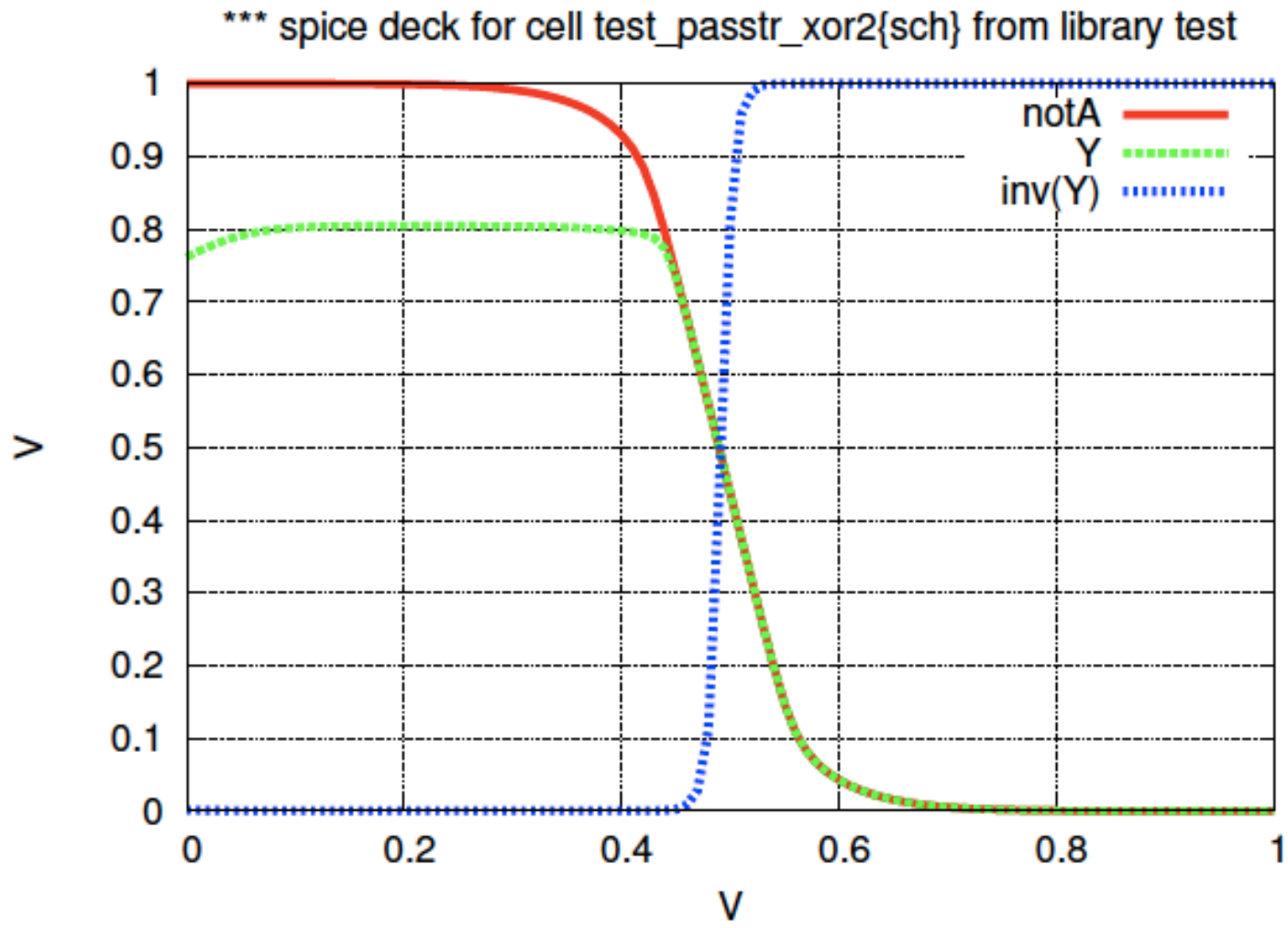
XOR Output

- Reasonable Input to CMOS Inverter?





Pass Transistor xor2 with inv restore

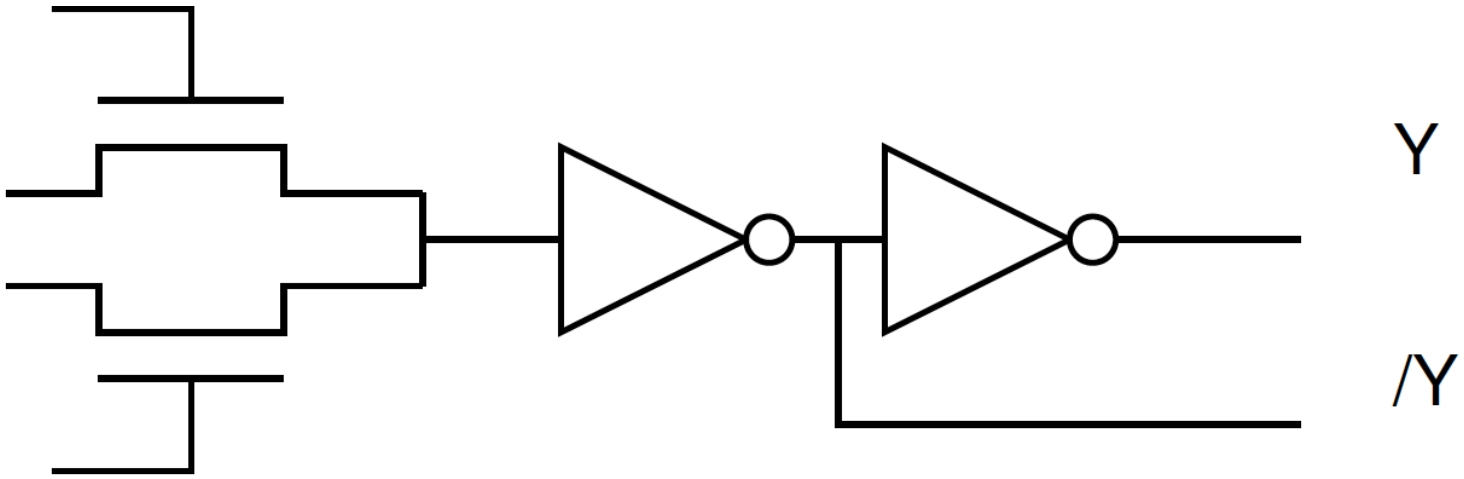


Required to use?

- What should we add to make suitable comparison with CMOS?

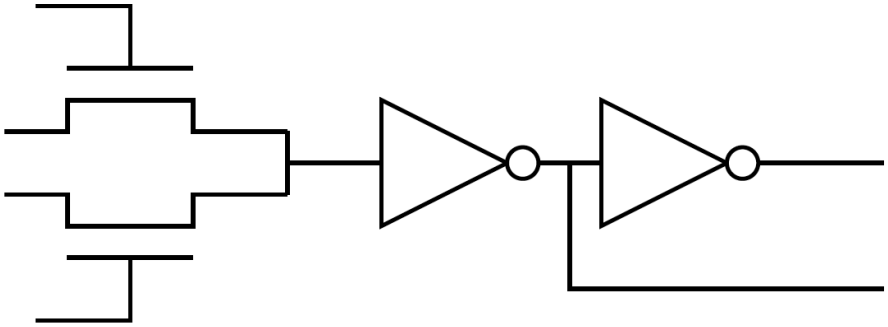
Restore Output

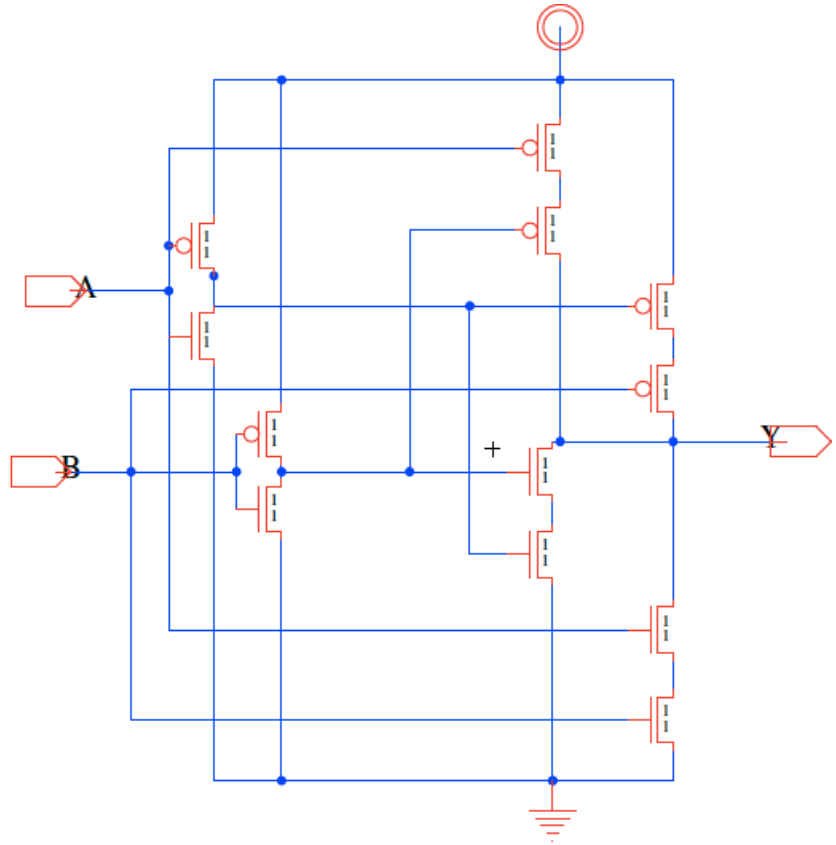
- What should we add to make suitable comparison with CMOS?



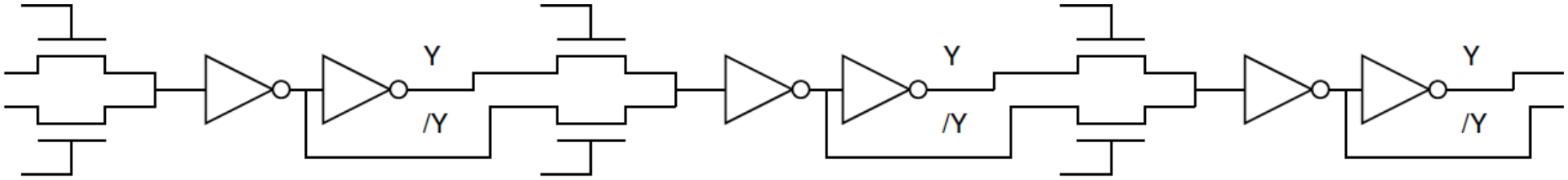
Restore Output

- Area? (compare to CMOS)

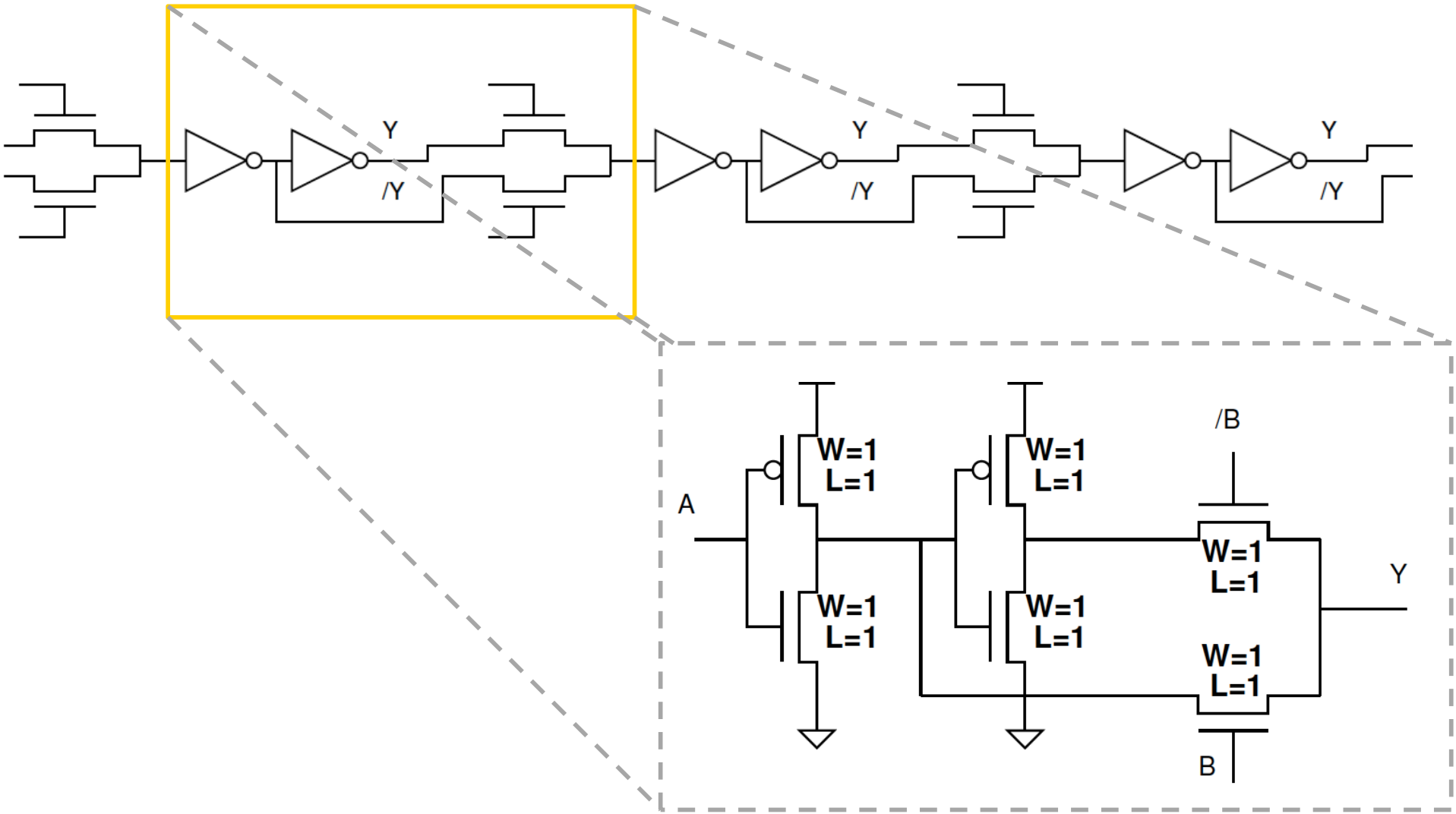




Chain Together

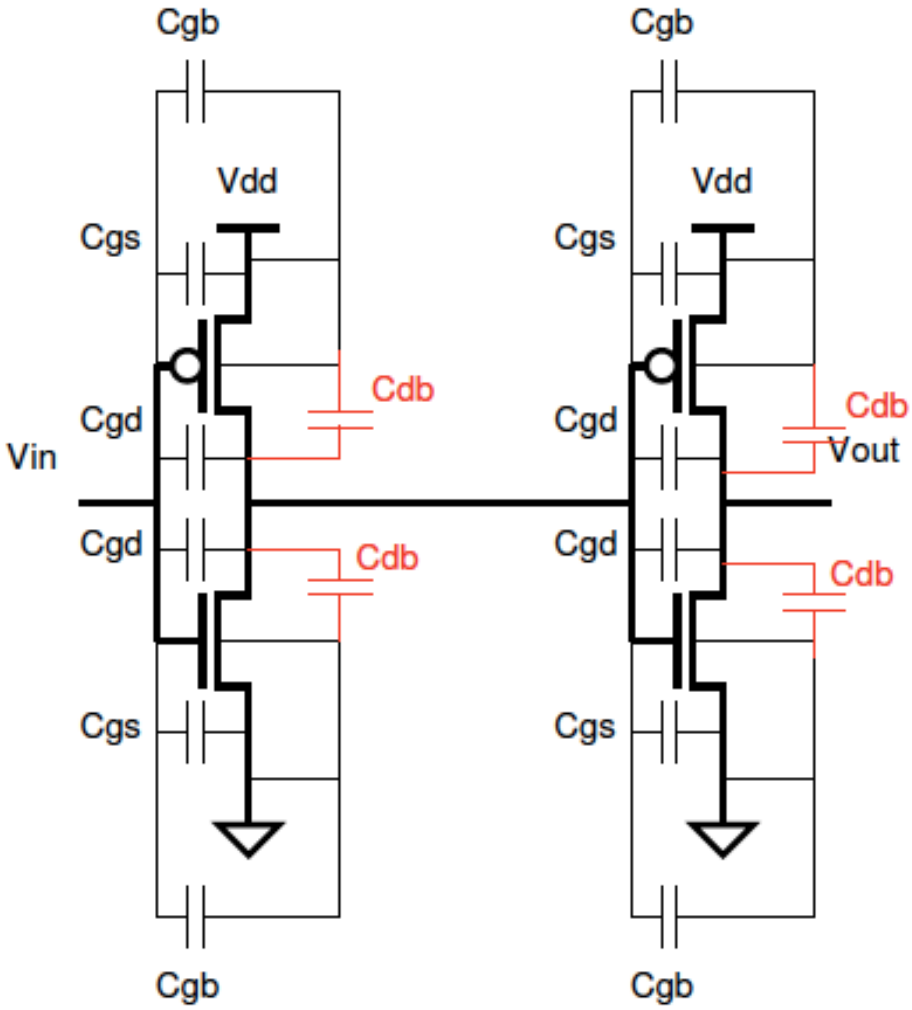


Analyze Stage



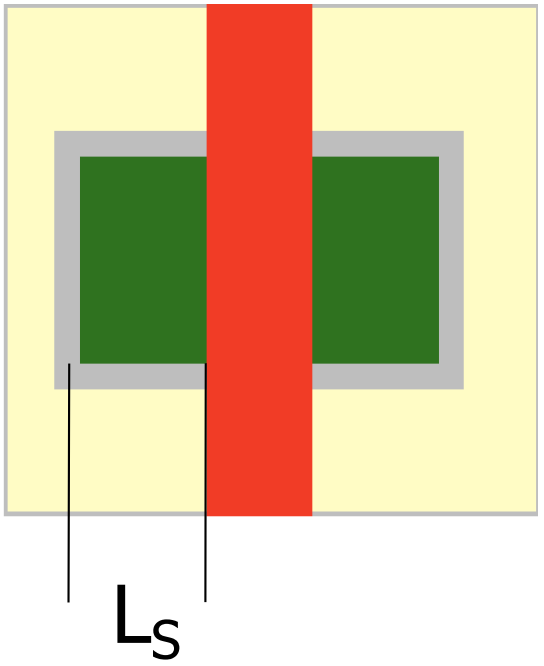
Impact of Capacitance

- $C_{GS}=C_{GCS}+C_{GSO}$
- $C_{GD}=C_{GCD}+C_{GDO}$
- $C_{GB}=C_{GCB}$
- $C_{SB}=C_{diff}$
- $C_{DB}=C_{diff}$



Contact/Diffusion Capacitance

- C_j – diffusion depletion
- C_{jsw} – sidewall capacitance
- L_S – length of diffusion

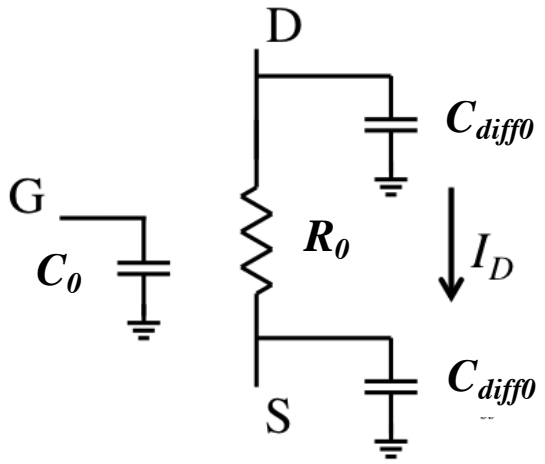


$$C_{diff} = C_j L_S W + C_{jsw}\left(2L_S + W\right)$$

Define: $C_{diff\,0} \approx \gamma C_0$

$$C_{diff} \approx W C_{diff\,0} = W \cdot \gamma C_0$$

First Order Model



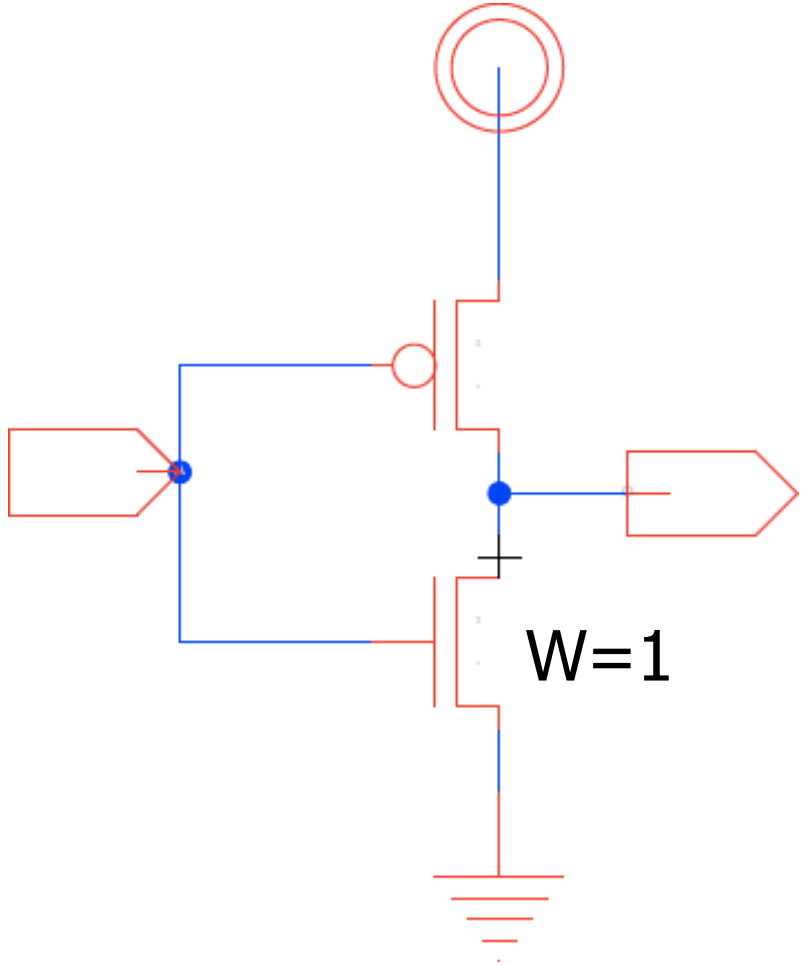
- Switch
  - Loads all terminals capacitively
    - Draw no steady-state current for a CMOS gate
    - Does not impact steady-state output voltage
    - Impacts Settling time/Delay
  - Has finite drive strength
    - Could form voltage divider with resistive load
    - Impacts Settling time/Delay

First Order Delay

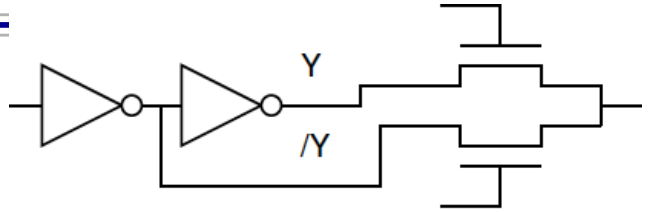
- R_0 = Resistance of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- C_{diff0} = diffusion capacitance on minimum size NMOS
  - $C_{diff0} = \gamma C_0$
- $R_{drive} = R_0/W$
- $C_g = WC_0$
- $C_{diff} = WC_{diff0} = \gamma WC_0$

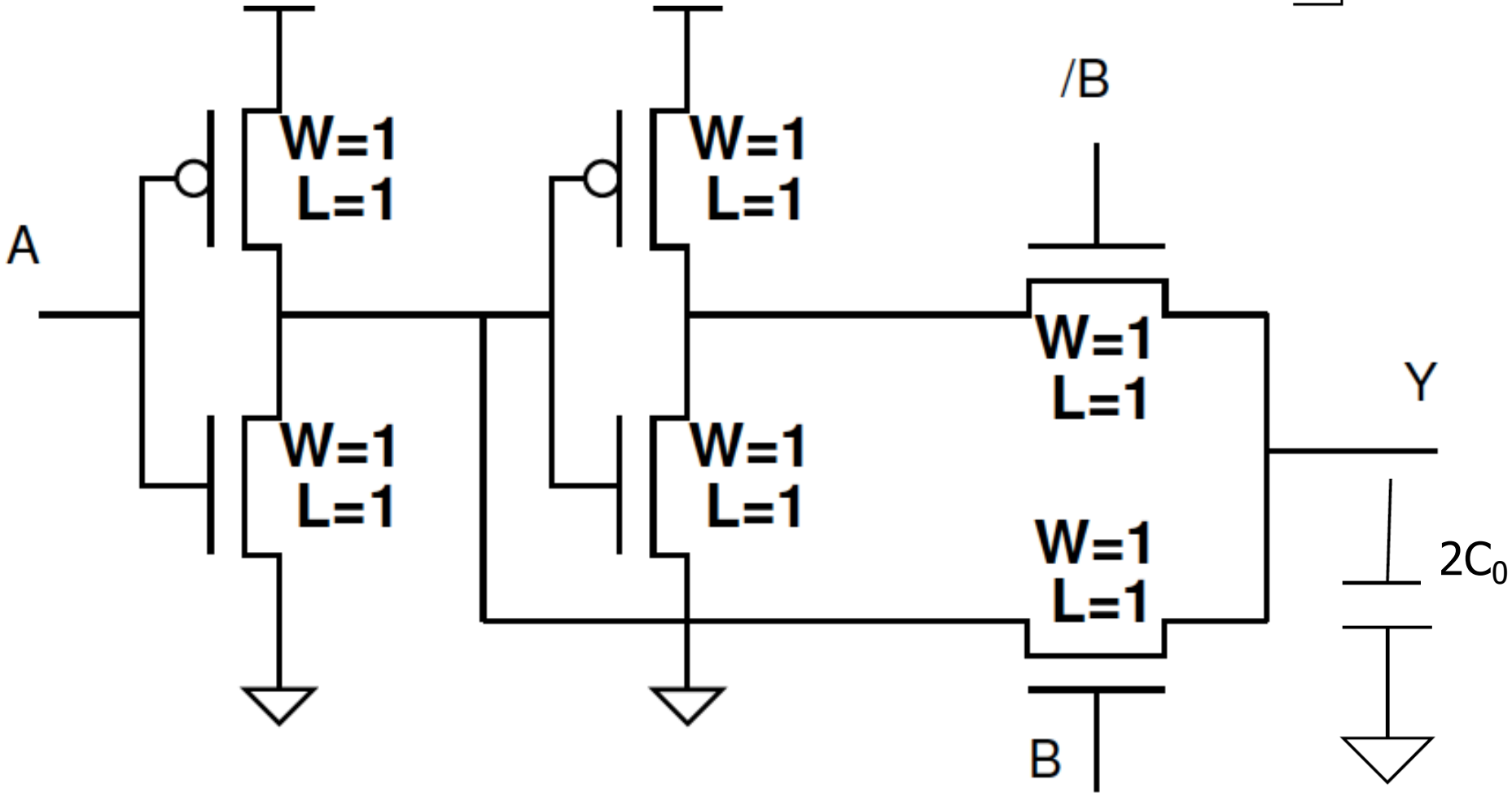
Inverter Delay

- Delay driving another (min size) inverter?
  - Include $C_{diff}=\gamma C_g=\gamma W C_0$



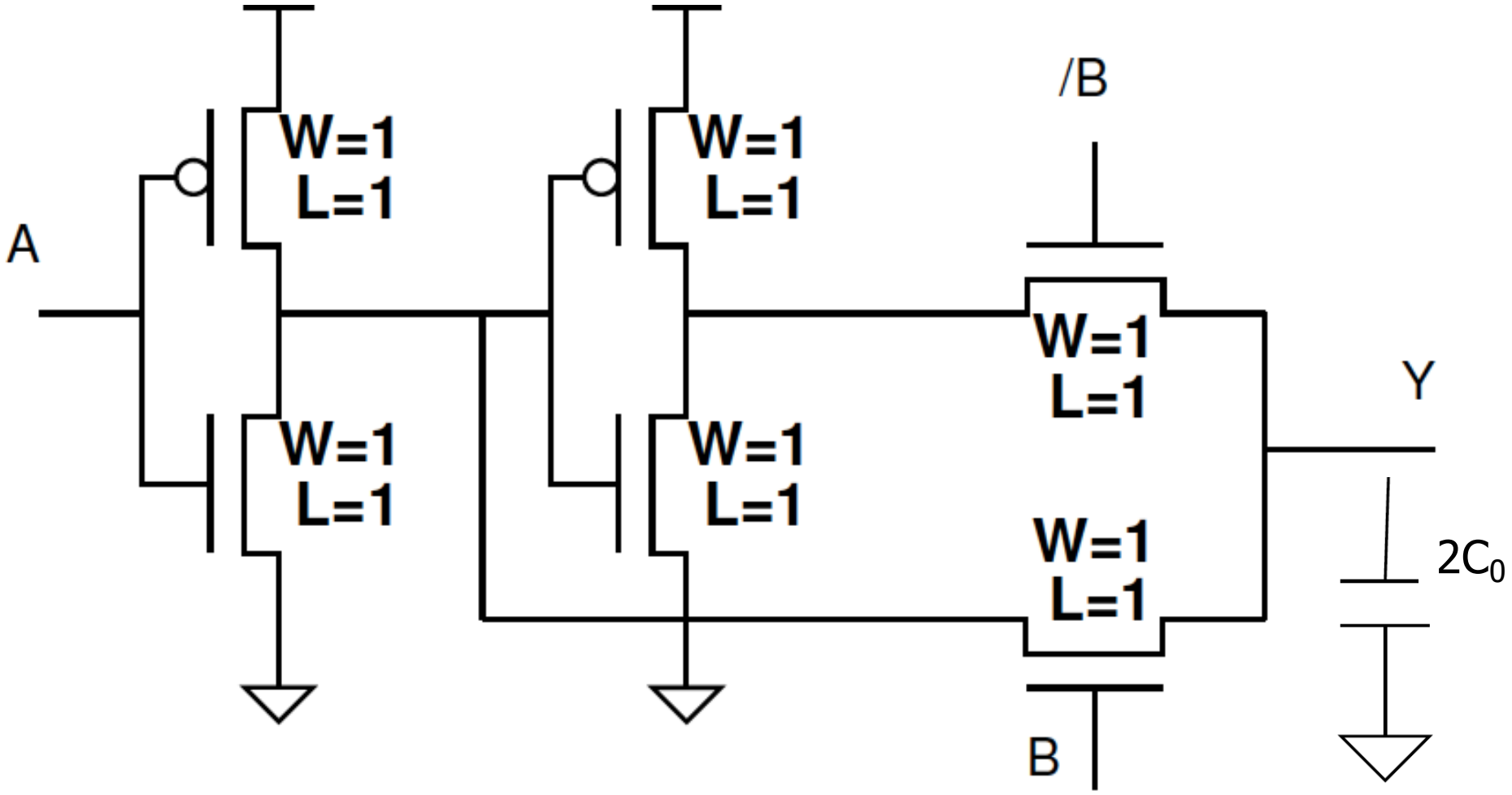
Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)





Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

- What's the equivalent RC circuit?



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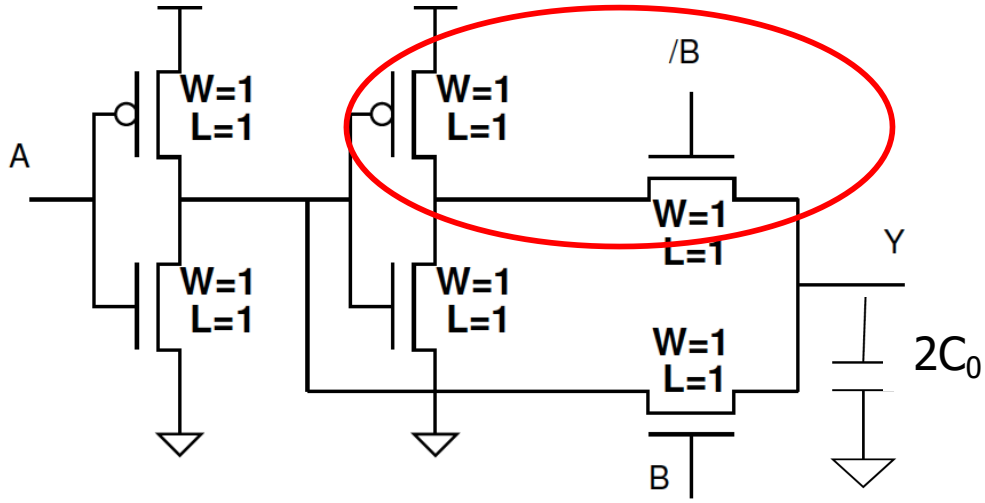

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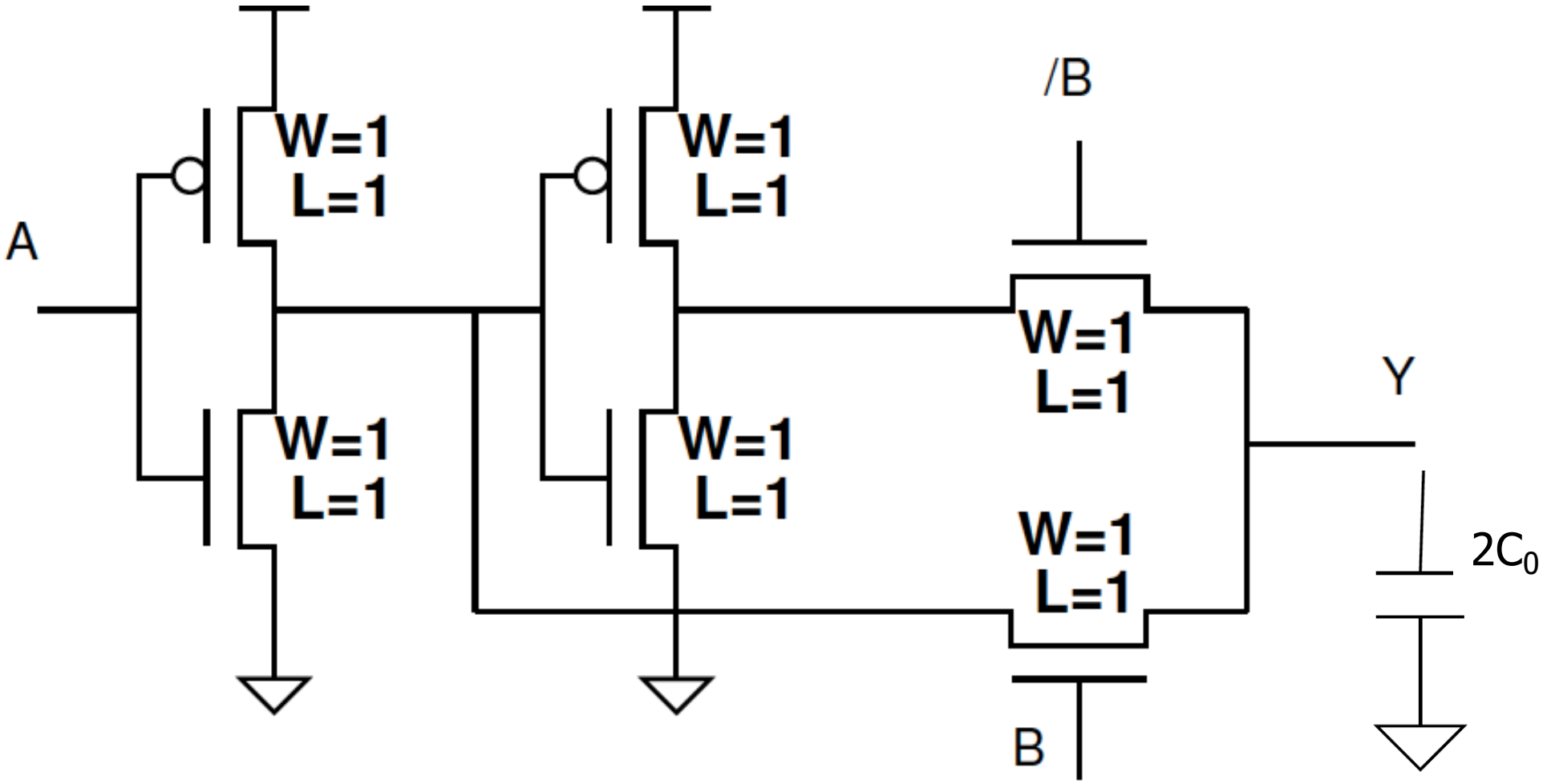

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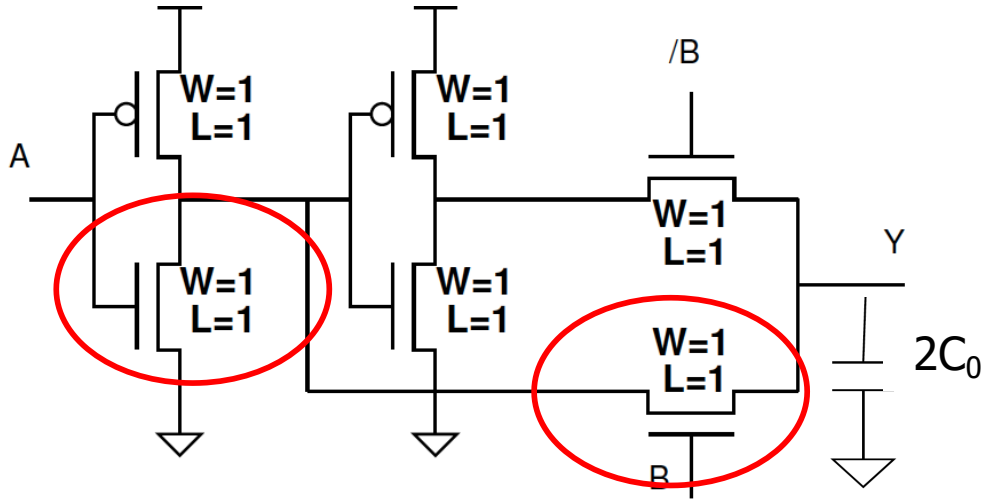
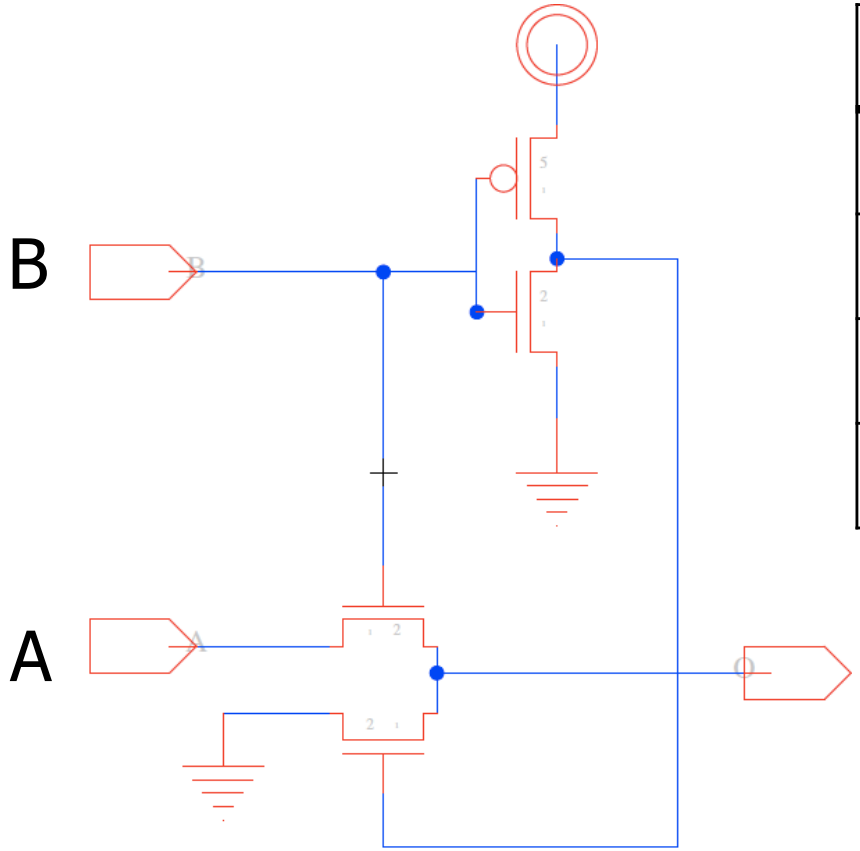


Bonus

- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

Idea

- There are other circuit disciplines
- Can use pass transistors for logic
  - Sometimes gives area or delay win

Admin

- Project 1
  - Milestone due tonight @midnight
    - Will get feedback by Sunday morning
  - Can't pass the class if you don't turn in projects
    - Can't do project last minute
  - Really should be into exploring optimizations for baseline