Course Webpage

Circuit-Level Modeling, Design, and Optimization for Digital Systems

Course: ESE370

Units: 1.0 CU
Term: Fall 2021
When: MWF 12-1pm EST (all times below are EST)
Where: Towne 307
Instructor: Tania Khanna (Levine 262, seas: taniak)
Instructor Office Hours: T 2-3pm (via Zoom, see Piazza for link), W 1-2:30pm in person, or by appointment
TA: Felicity Qin (seas: feli) (office hours: M 2-3pm, F 11am-12pm (via Zoom, see Piazza for link), Th 3-4:30pm (in-person, room TBD))

Prerequisites: ESE 150, ESE 215, CIS 240 is also highly recommended. Roundup of topics you should be familiar with.
URL: <http://www.seas.upenn.edu/~ese370/>

Quick Links: [Course Objectives] [Grading] [Policies] [Fall 2021 Calendar] [Reading] [Student Advice] [Piazza] [Tool Guides]

Catalog Level Description: Circuit-level design and modeling of gates, storage, and interconnect. Emphasis on understanding physical aspects which drive energy, delay, area, and noise in digital circuits. Impact of physical effects on design and achievable performance.

Role and Objectives

The goal of this course is to teach students what they need to know about the physical aspects (area, delay, energy, noise) of electronic circuits to support high-speed, low-energy, area-efficient design of robust digital and computer systems. Students will learn:

- disciplines for robust digital logic and signaling (e.g., restoration, clocking, handshaking)
- where delay, energy, area, and noise arises in gates, memory, and interconnect
- how to model these physical effects both for back-of-the-envelope design (e.g. RC and Elmore delay) and detailed simulation (e.g., SPICE)
- the nature of tradeoffs in optimization
- how to design and optimize logic, memory, and interconnect structures at the gate, transistor, and wire level
- how technology scales and its impact on digital circuits and computer systems

This course comes after a basic introduction to devices and circuits (ESE215) and a course on gate-level digital design (ESE150/CIS240). It should serve both students who will go on to do circuit-level design and

https://www.seas.upenn.edu/~ese370/

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ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 1: September 1, 2021
Introduction and Overview

Penn

Penn ESE370 Fall 2021 – Khanna

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Your First Priority

- Your first priority is your health
  - You should abide by all health guidelines
    - Wear a mask
    - Wash your hands
    - Don't touch your face
    - Maintain ~~social~~ physical distancing
      - Careful and thoughtful social interaction is encouraged!
    - Stay home if you're sick
  - Part of your health is your mental and emotional health
    - See https://caps.wellness.upenn.edu/selfhelp/ for help
  - For more: https://coronavirus.upenn.edu/

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I want to hear from you…

- Accessibility Survey in Canvas
  - Submit by Saturday for full HW credit
- Are there any other accessibility issues I should know about?
- Let me know any concerns -- I will do everything I can to ensure you achieve the learning objectives

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Where I come from

- Analog VLSI Circuit Design (analog design)
- Convex Optimization (system design)
  - System Hierarchical Optimization
- Biomedical Electronics
- Biometric Data Acquisition (signal processing)
  - Compressive Sampling
- ADC Design (mixed signal)
- Low Energy Circuits (digital design)
  - Adiabatic Charging

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CIRCUITS, CIRCUITS, CIRCUITS

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Lecture Outline

- Course Overview
  - Motivating questions
  - What this course is about
  - Learning objectives
  - What you need to know
- Course Details
  - Course structure
  - Course policies
  - Course content

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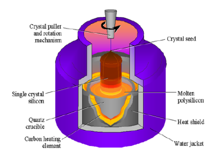
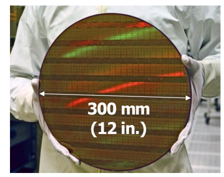
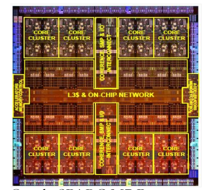
VLSI Design





Oracle SPARC M7 Processor

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Motivating Questions

- How fast can my computer run?
  - What limits this speed?
  - What can I do to make it run faster?
- How can I extend the battery life on my gadget?
  - How much energy must my computation take?
- How small can I make a memory?
  - Why does DRAM need to be refreshed?'
    - What is DRAM? SRAM? EEPROM?

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Motivating Questions (con't)

- How many bits/second can I send over a communication link?
  - What limits this?
  - How do I maximize my data rate?
- How does technology scaling change these answers?
  - What can I rely on technology to deliver?

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Motivating Questions (con't)

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  - What limits this?
  - How do I maximize my data rate?
- How does technology scaling change these answers?
  - What can I rely on technology to deliver?
- How does my application change these answers?
  - Is fastest best? Is lowest energy best? Is smallest best?

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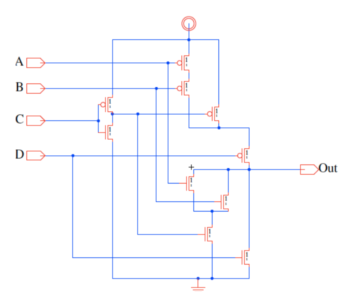
Sample Problems

- What does this circuit do?



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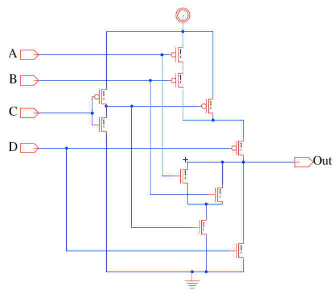
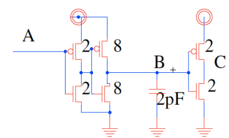
Sample Problems

- What does this circuit do? How fast does it operate?



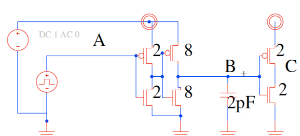
Sample Problems (con't)

- What does this circuit do? How are A, B, C related?



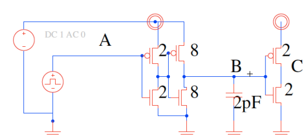
Sample Problems (con't)

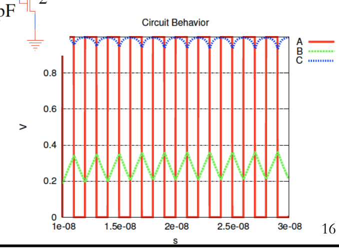
- What does this circuit do? How are A, B, C related?



Sample Problems (con't)

- What's wrong here? How do we fix it?





Limits?

- Consider a 22nm technology
- Typical gate with W=3, 2-input NOR
- Use chip in cell phone
- What prevents us from running 1 billion transistor chip at 10GHz?

Impact of Voltage?

- If we have a chip running at 1GHz with a 1V power supply dissipating 1W.
- What happens to performance if we cut the power supply to 500mV?
  - Speed?
  - Power?

What this course is about

- Modeling and abstraction
  - Predict circuit behavior
  - …well enough to know your design will work
  - …with given performance spec(ification)s
    - Speed, energy, size, etc.
  - …well enough to reason about design and optimization
    - What knob can I turn to make faster?
    - How much faster can I expect to make it?

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What this course is about (con't)

- Modeling and abstraction
  - Back-of-the-envelope calculations
    - Simple enough to reason about and estimate
      - …without a calculator
  - Sensitive to phenomena
    - Able to think through the details
  - With computer assistance
    - …understanding even that is a simplified approximation of phenomenology

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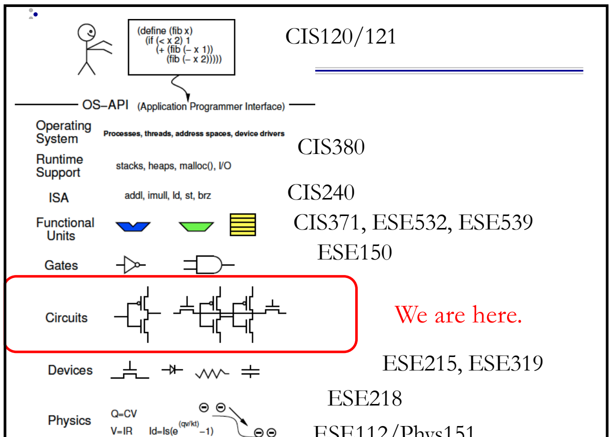

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Learning Objectives

- Disciplines for robust digital logic and signaling
  - (*e.g.*, regeneration, clocking)
- Where delay, energy, area, and noise arise in gates, memory, and interconnect
- Modeling these physical effects
  - back-of-the-envelope design
    - (*e.g.* RC and Elmore delay)
  - detailed simulation (*e.g.* SPICE)

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Learning Objectives (con't)

- Tradeoffs in performance specs
  - Among delay, energy, area, noise
- How to design and optimize
  - logic, memory, and interconnect structures
  - at the gate, transistor, and wire level
- How technology scales
  - impact on digital circuits and computer systems

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What you need to know

- See "knowledge roundup" topics page linked from course webpage
- ESE 150 (CIS 240*)
  - Gates, Boolean logic, DeMorgan's, gate optimization, K-maps
  - Review: book chapter in Canvas
- ESE 215
  - RLC circuit analysis
  - Review: 215 lectures posted in Canvas
- Diagnostic Quiz on Canvas
  - Not graded, weighted as a homework assignment
  - Complete by Tuesday 9/7 midnight
  - 150 and 215 review materials in Canvas Files section
  - TA review video posted early next week

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Course Structure: Websites

- Website (http://www.seas.upenn.edu/~ese370/)
  - Course calendar is used for all handouts (preclass, lecture slides, assignments, and readings)
  - Canvas used for assignment submission, grades and lecture recordings
  - Piazza used for announcements and discussions
    - Use for Zoom links for OHs

Course Structure: Staff

- Course Staff (complete info on course website)
- Instructor: Tania Khanna (she/her)
  - Virtual OH: T 2-3pm
  - In person OH: W 1-2:30 pm
  - Or OH by appointment
  - Email: taniak@seas.upenn.edu
    - Best way to reach me

TA: Felicity Qin

- About me: I'm a senior in EE and took ESE 370 in the Fall of 2020
- Virtual OH:
  - M 2-3pm
  - F 11am-12pm (via Zoom, see Piazza for link)
- In person OH:
  - Th 3-4:30pm (in-person, room TBD))
- "The crucial thing for 370 is going to class! **Always go to class — always ask questions**. Professor Khanna's expertise is invaluable, and getting answers in real-time is much more efficient than email or Piazza."

Course Structure: Lectures

- MWF 12-1pm Lecture in Towne 307
  - Lecture recordings posted into Canvas
- Preclass and lecture slides posted online before class
- Readings from textbook
- 3 lecture periods → Labs in Ketterer

ESE370 Fall 2021 Working Schedule

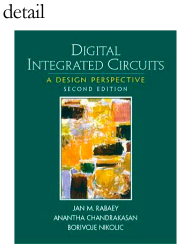
Wk	Lect.	Date		Lecture	Slides	Due	Reading
	1	9/1	W	Intro/Overview	[lec1] [lec1_6up]		1 through 1.2; review course web page completely
1	2	9/3	F	Transistor Introduction (basics) and Gates from Transistors			review ESE215; 6.2 through static properties in 6.2.1
		9/4	Sa			Access Survey (in canvas)	
		9/6	M	Labor Day			
2		9/7	Tu			Diagnostic Quiz (in Canvas)	
		9/8	W	Lab 1 (Ketterer): Gate from Discrete Transistors			
	3	9/10	F	Transistor Introduction (first order)			3.1
	4	9/13	M	Regenerative Property			1.3.2
3		9/14	T			HW 1 ADD DATE	
	5	9/15	W	Delay and RC Response			1.3.3
	6	9/17	F	MOS Model			2.1-2.3, 3.3.1
	7	9/20	M	MOS Transistor Operating Regions: Part 1		HW2	3.3.2 (to pg 94)

Course Structure: Lectures

- Mask required
  - Will be asked to leave and reported to OSC if no compliance
- Statistically and empirically speaking, you will do better if you come to lecture
- Better if interactive, **everyone** engaged
  - Asking and answering questions
  - Actively thinking about material every day
- Two things
  - Preclass worksheet exercises
    - Work during ~5 minutes before lecture starts
    - Primes you for topic of the day
    - Will be addressed during lecture
  - Ask questions of individuals

Course Structure: Textbook

- Textbook
  - *Digital Integrated Circuits, A Design Perspective*, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2nd edition
    - Great reference text with great detail
    - REALLY!! useful for projects



Course Structure: SPICE

- Simulation Program with Integrated Circuit Emphasis
  - Industry standard analog circuit simulator
  - Non-linear, differential equation solver specialized for circuits
- Integrated circuits – simply impractical to build to debug
  - Must simulate to optimize/validate design

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Course Structure: Assignments/Exams

- Homework – week long (7 total) [25%]
  - Due (mostly) F at midnight
  - Submit in Canvas
- Projects – 1-3 weeks long (2 total) [30%]
  - Design/Simulation oriented
  - On three main topics
    - 1: Computation - Individual
    - 2: Storage - Team
- Midterms [20%] (2 total)
  - 2 hours in the evening
- Final exam [25%]

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Course Structure: Admin

- Use course calendar
  - Lectures and preclass online before class
    - Will post night before class
    - Reserve the right to change them (usually minor)
  - Homework/projects linked
    - Homework 1 out now
  - Reading for whole term specified
- Take notes!
  - Especially on the examples we do in class
  - Slides have a lot of questions – not a lot of answers

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Course Policies

See course web page for full details

- Turn assignments in on Canvas
  - Anything handwritten/drawn must be clearly legible
    - No handwritten work allowed on projects
  - Submit CAD generated figures, graphs, results when specified
  - Late Policy – allowed 4 late days for whole semester
    - Can only use a max of one day on projects
- Individual work (HW & Project*)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

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Course Content

- Logic (Computation) [10 weeks]
  - Combinational logic
  - Sequential logic
- Memory/Storage [2 weeks]
- Communication/Interconnect [3 weeks]

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Course Content (con't)

- Logic
  - Transistors → Gates
  - **Lab:** build gate, measure delay
  - Regeneration (noise margins)
  - Delay
  - Area (no layout → ESE370)
  - Energy
  - Synchronous (flip-flops, clocking, dynamic)
  - **Project 1:** fast ripple-carry adder

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Course Content (con't)

- Memory/Storage
  - No Lab component
  - RAM Organization
    - Memory cells and periphery circuits
  - Driving Large Capacitances
  - Signal amplification/regeneration
  - **Project 2:** design a SRAM

Course Content (con't)

- Communication/Interconnect
  - Repeaters in wiring
  - **Lab:** Cable noise
    - Measure inductive ground bounce, crosstalk
    - Experiment with PCB transmissions lines, termination
  - Noise
    - Crosstalk
    - Inductive
    - Ionizing particles, shot
  - **Lab:** PCB trace T-line behaviour
  - Transmission Lines

Advice

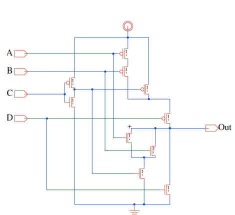
- Course is hard (but valuable)
- Should be thinking about this material every day
- Go to office hours
- MUST READ TEXT!
- Learning is spread over all components
  - Lecture, reading, **homework, projects**, exams
- Cannot pass the class if you don't turn in projects
  - Give yourself enough time. They will take you longer than you think

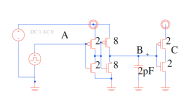
Advice from your fellow students:

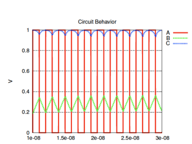
- Q: As a current or former student that did very well in ESE 370, what advice do you have for future students to be successful in ESE 370?
  - "The most important thing for me was to **attend lecture**"
  - "make sure you **start early** on the projects"
  - "ESE 370 is a class that **moves quickly**… best ways to stay abreast of the material was to engage with it … **ask questions and engage** in conversation in class (or in office hours) regularly"
  - "ESE 370 is a very **rewarding class, but not an easy class**. The biggest advice I can offer is to **stay on top of the work**."
  - "will be both very **challenging and rewarding**, and quite **unique compared to other classes at Penn**"
- See course webpage for full answers

Big Ideas

- Model (a.k.a. analysis and simulation) to enable real-life robust design and optimization







Admin

- Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese370
  - https://piazza.com/upenn/fall2021/ese370/
  - https://canvas.upenn.edu/courses/
- To do:
  - Submit Accessibility Survey (in canvas) – due Sa 9/4
    - Required/Recommended technology
  - Diagnostic Quiz (in Canvas) – due by T 9/7
    - Review as needed
  - HW 1 out now – due Tu 9/14
    - Need lab and future lectures to finish