ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

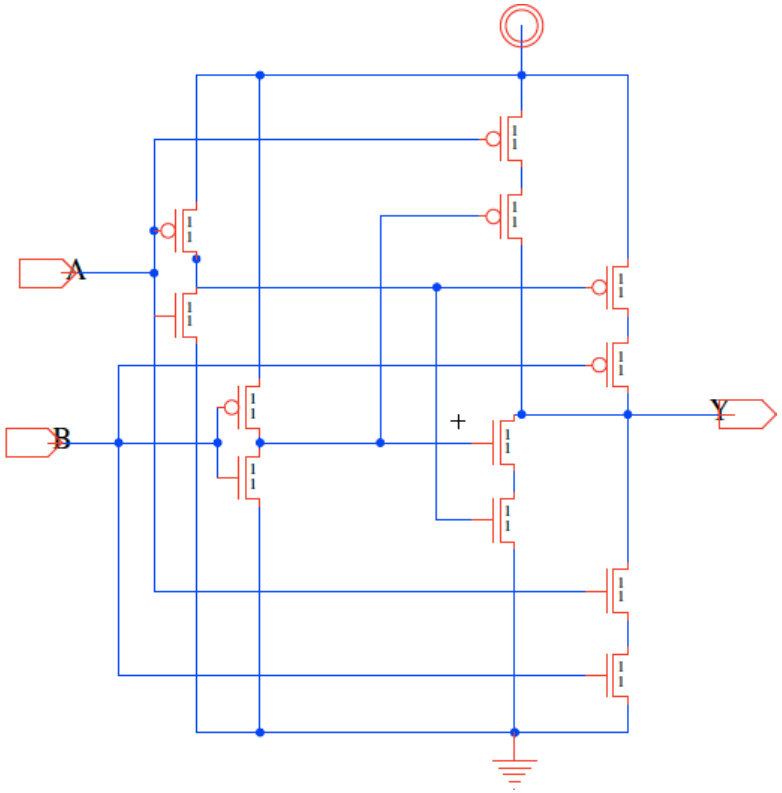
Lec 20: October 25, 2021

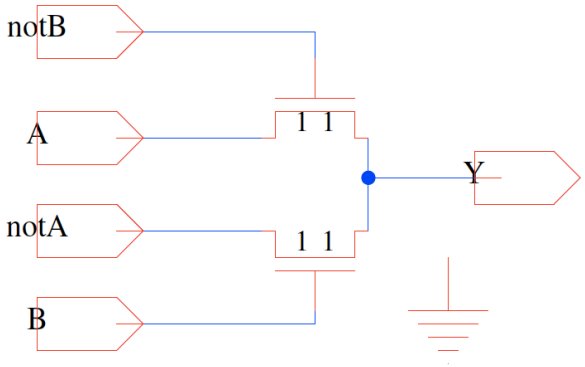
Pass Transistor Logic, Pt2

Today

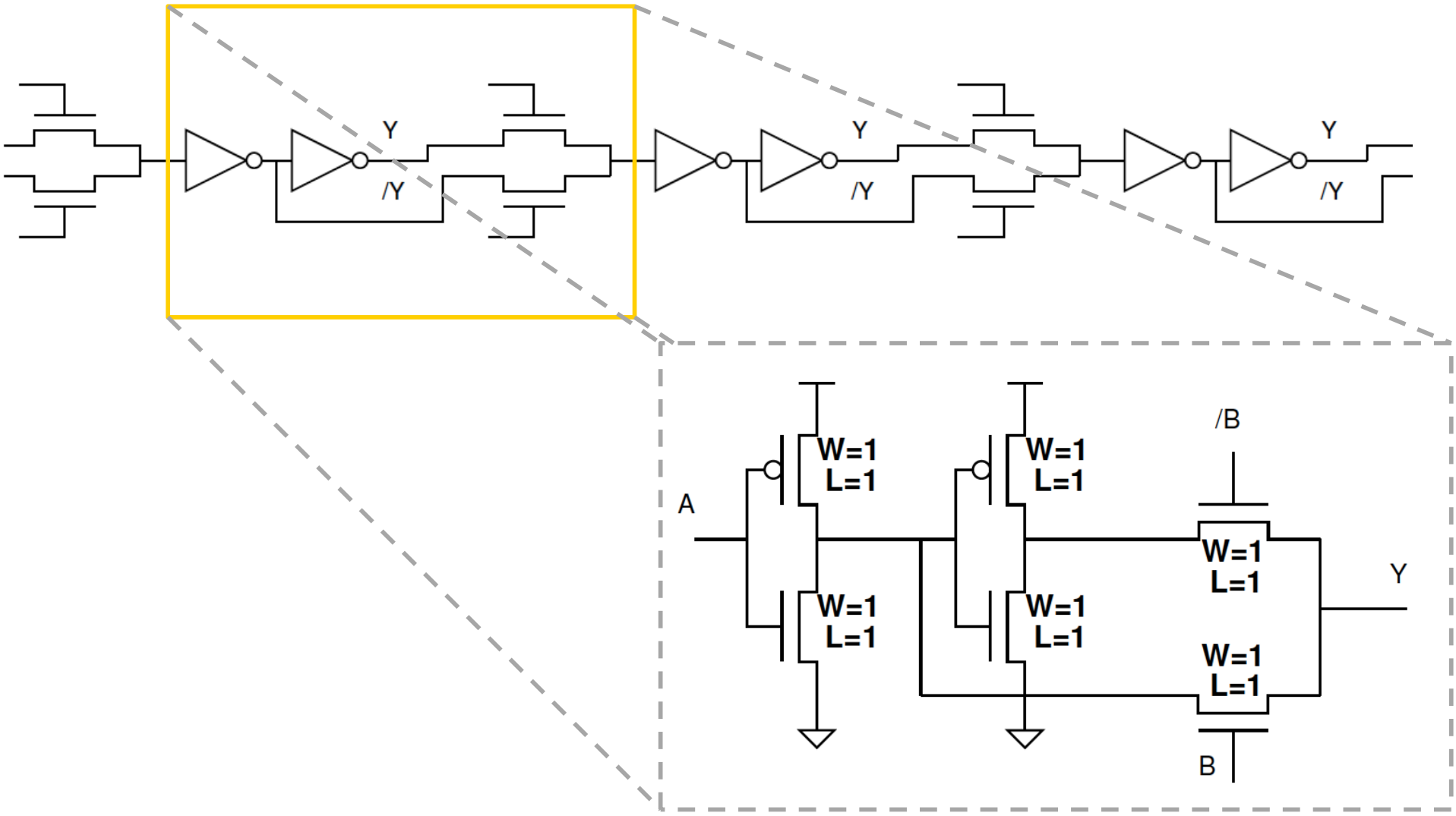
- Pass Transistor Circuit
  - $C_{diff}>0$
  - Output levels
  - Cascading
    - Series pass transistors?
    - Delay
- Start on Distributed RC
  - Analyzing delay for pass-tr designs

Previously: Two XOR Gates



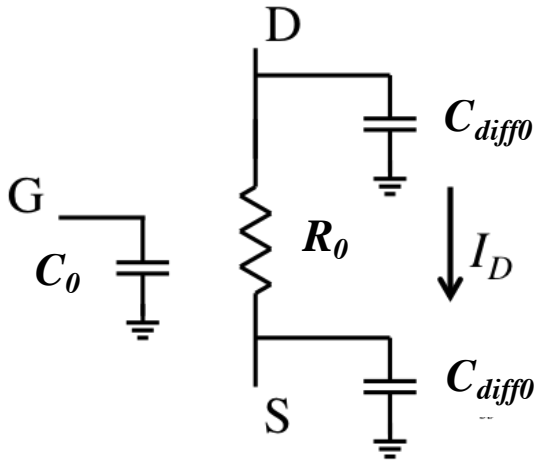


Cascaded Pass Gates



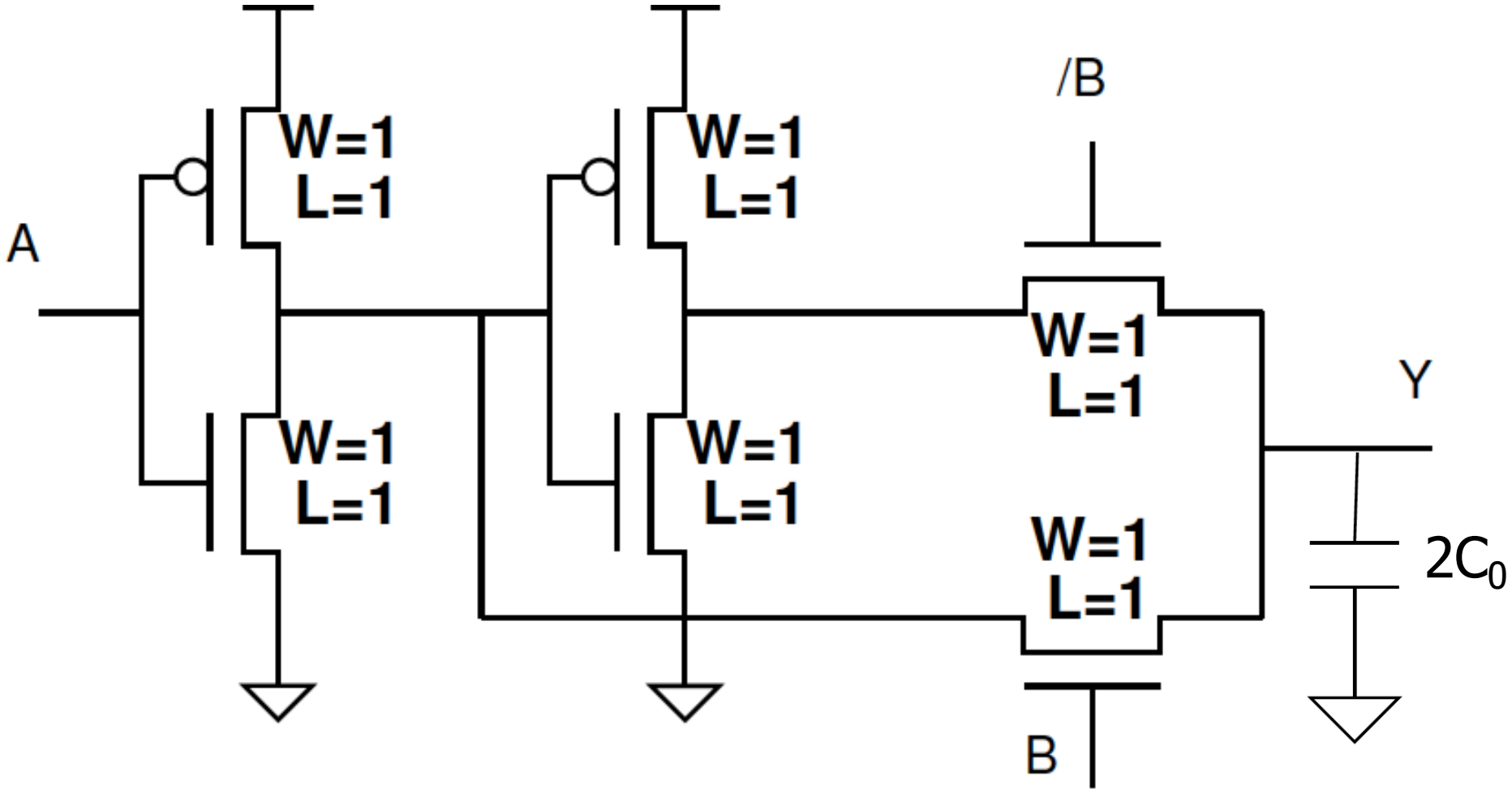
First Order Delay

- R_0 = Resistance of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- C_{diff0} = diffusion capacitance on minimum size NMOS
  - $C_{diff0} = \gamma C_0$
- $R_{drive} = R_0/W$
- $C_g = WC_0$
- $C_{diff} = WC_{diff0}$



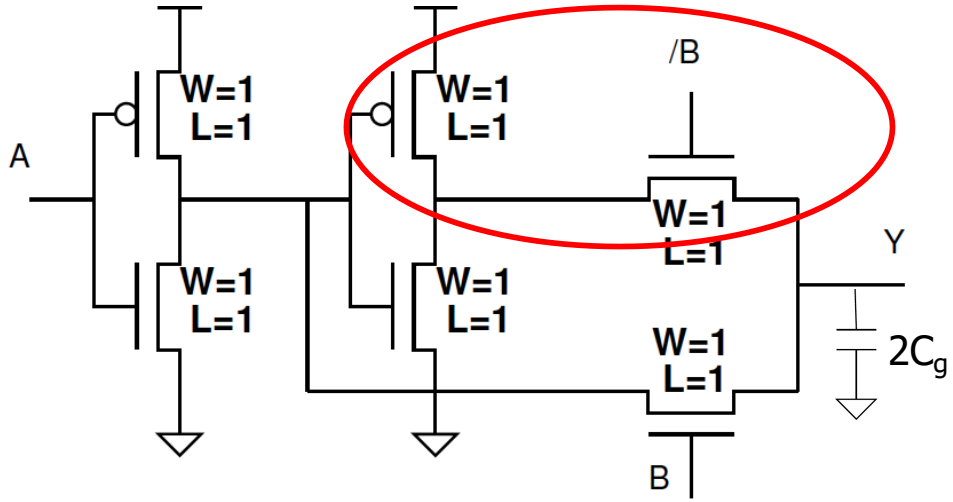
Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 1)

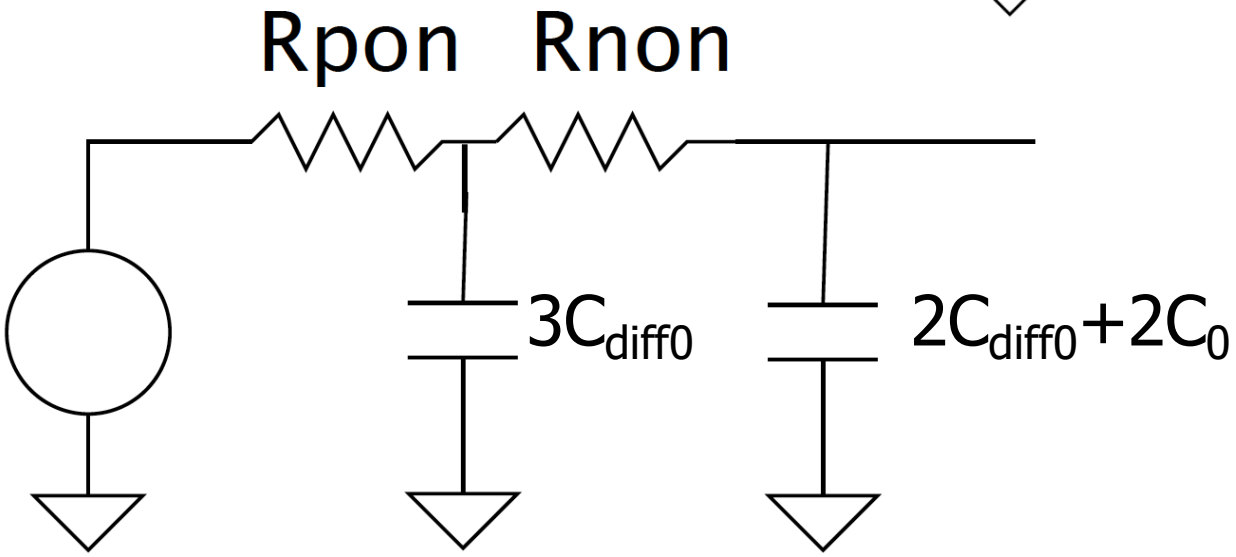
- What's the equivalent RC circuit?



Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 1)

- What's the equivalent RC circuit?
  - What is the total delay?
    - From A to Y





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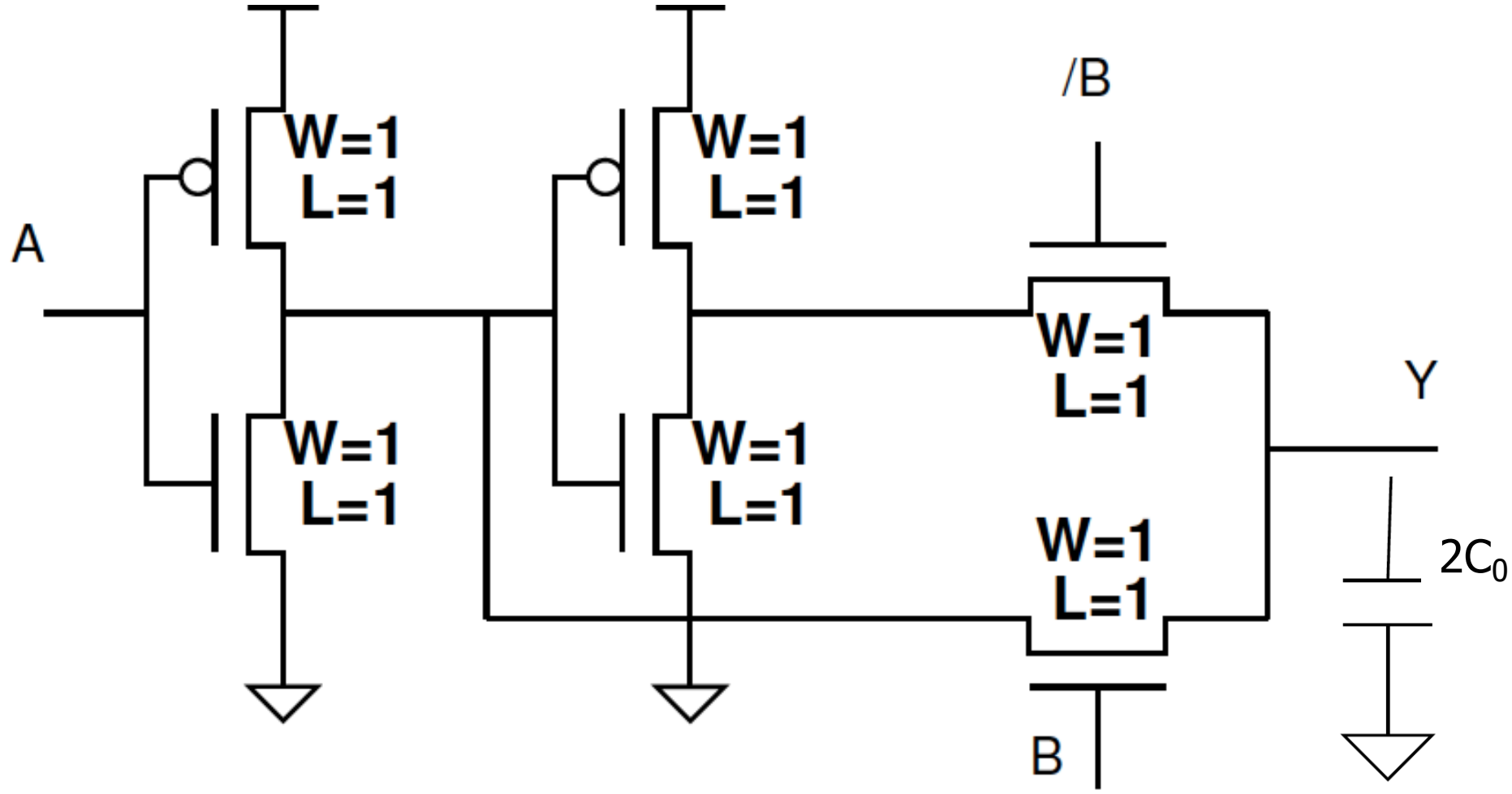

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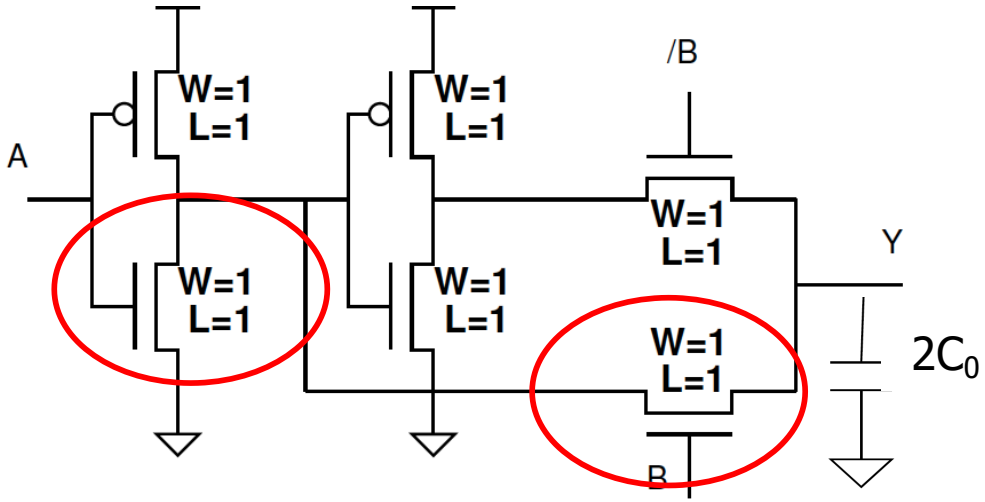
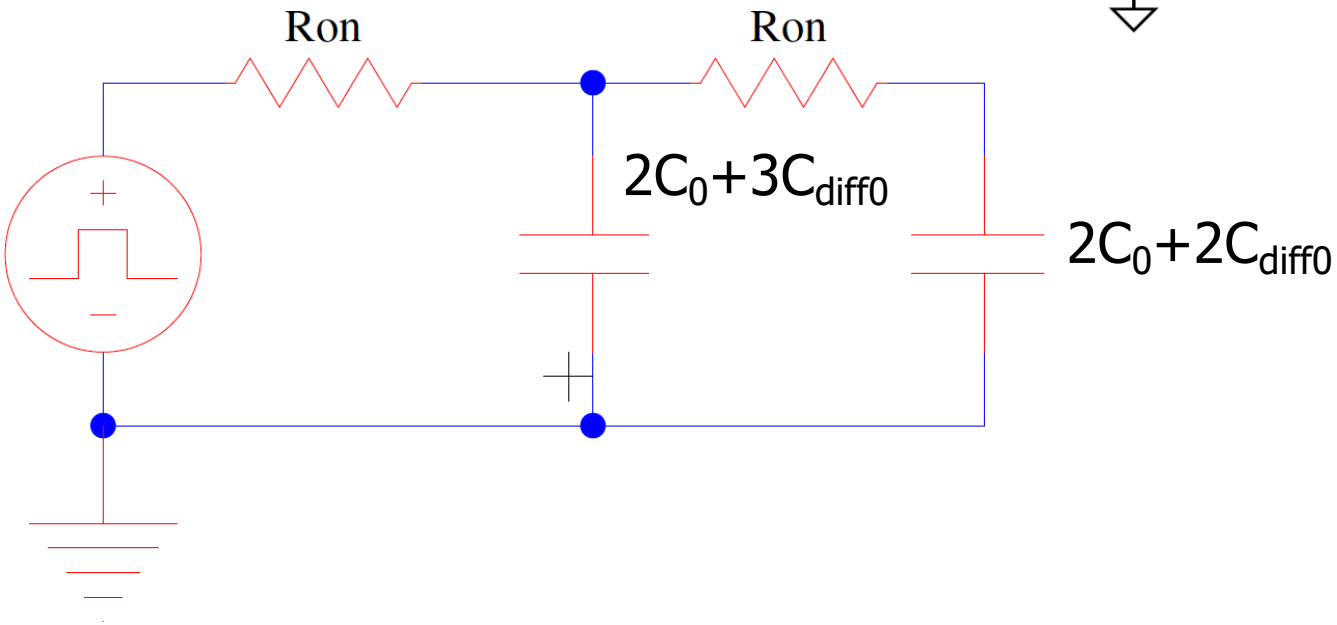
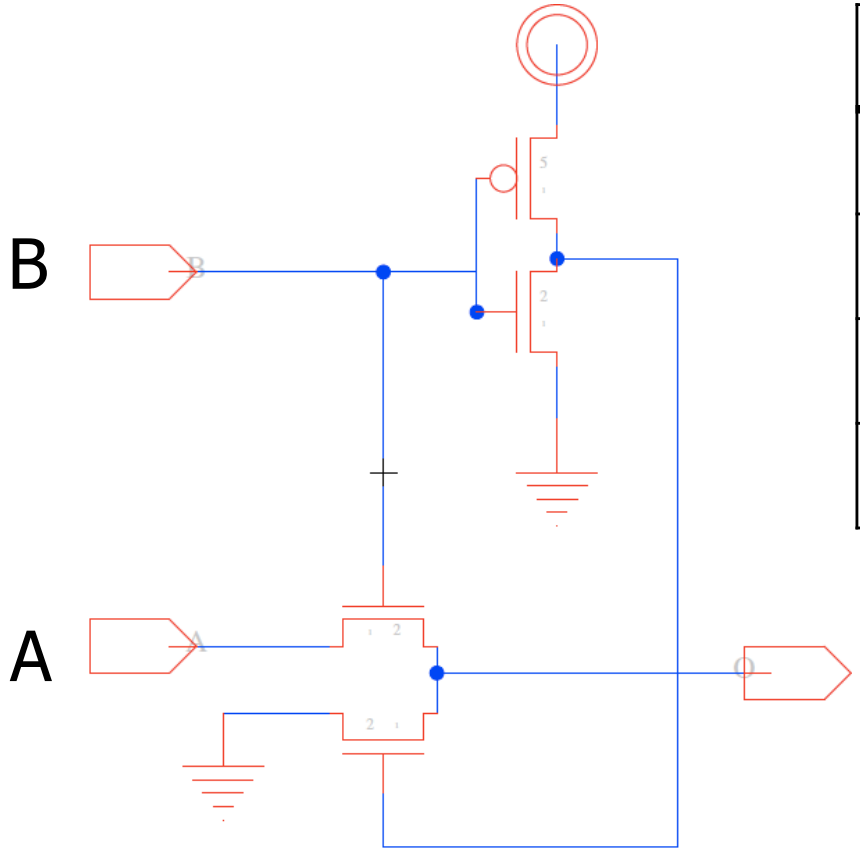




Bonus

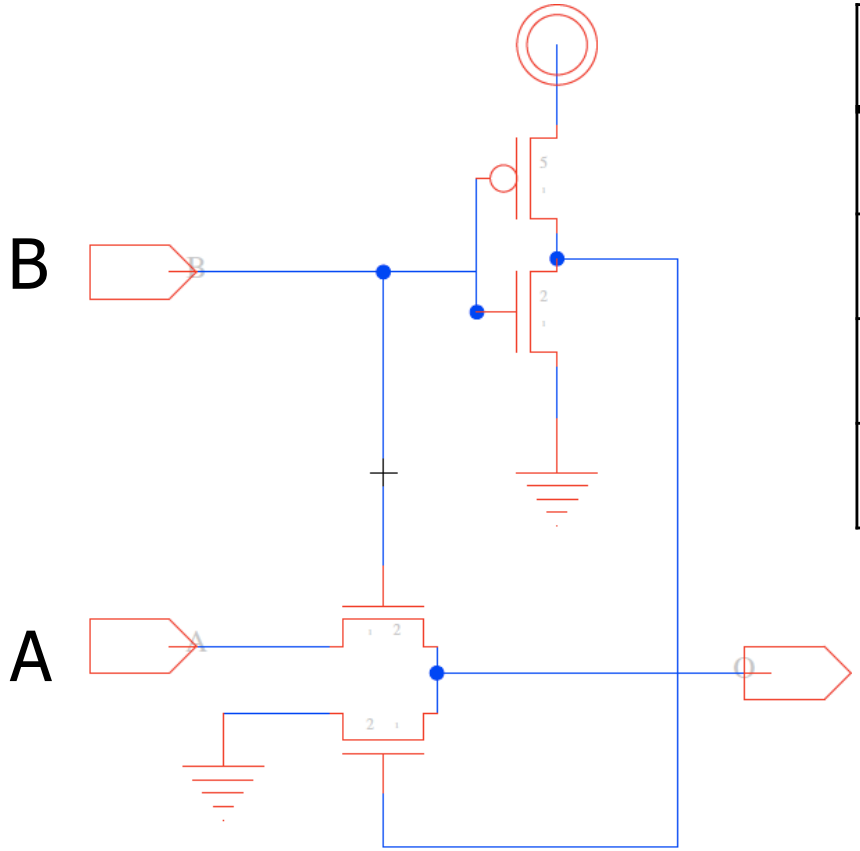
- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

Bonus

- What does this do?



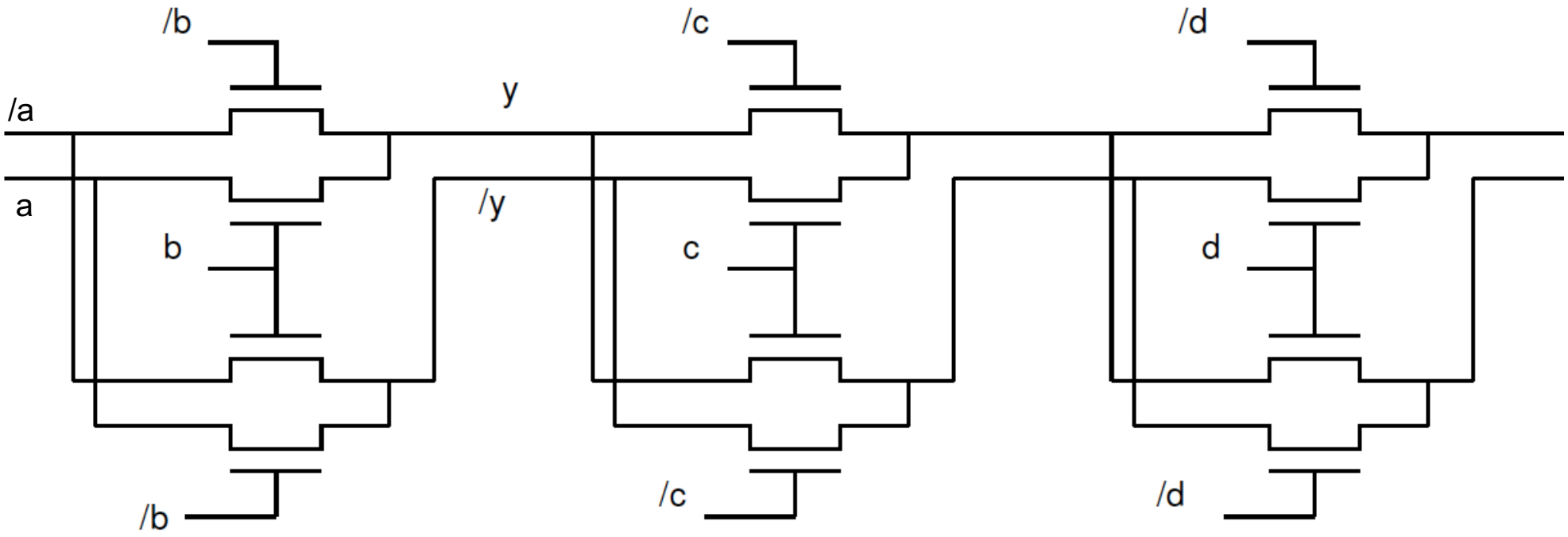
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

More examples in the text

Cascading Pass Transistors

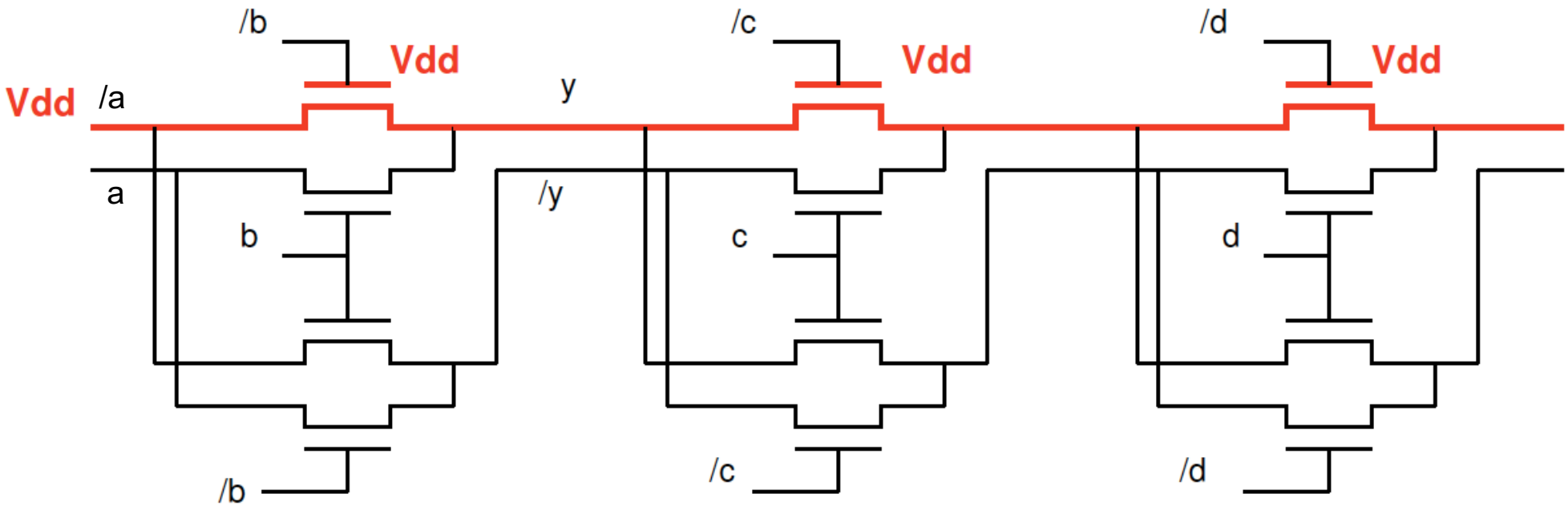
Chain without Inverters

- What if we did this?



Chain without Inverters

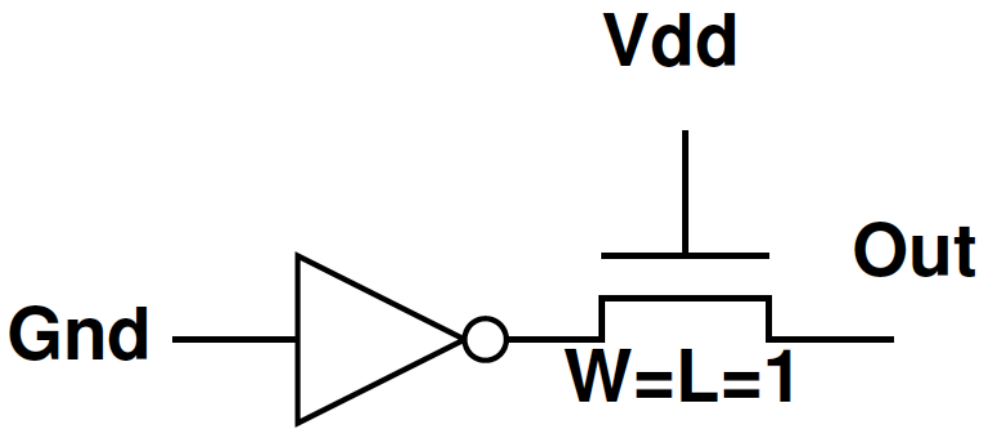
- Extract key path



Voltage of Chain (Preclass 2)

- What is voltage at output?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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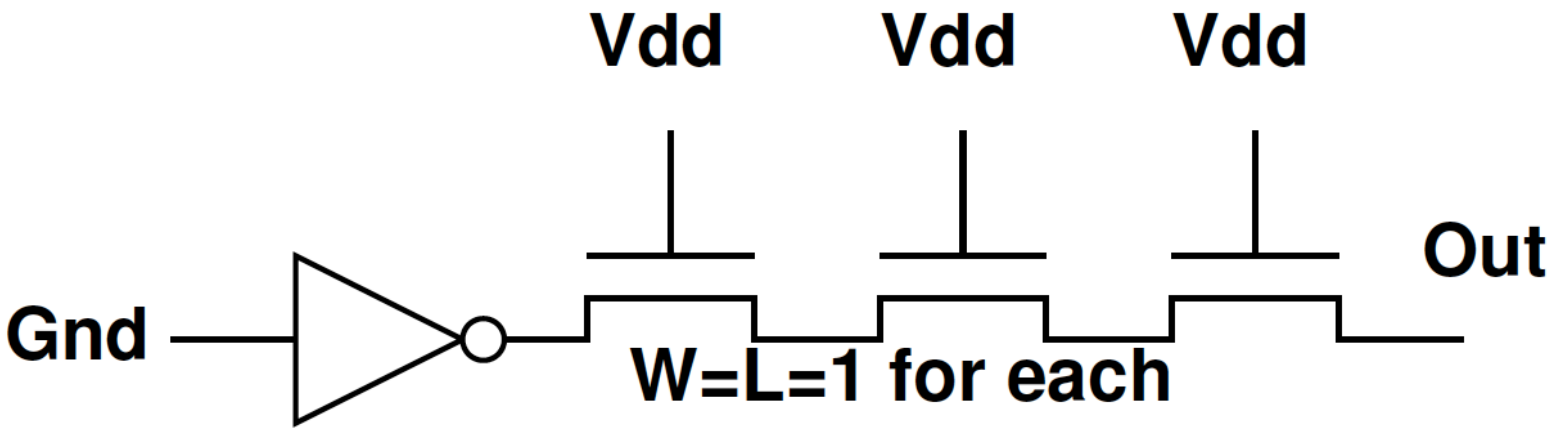
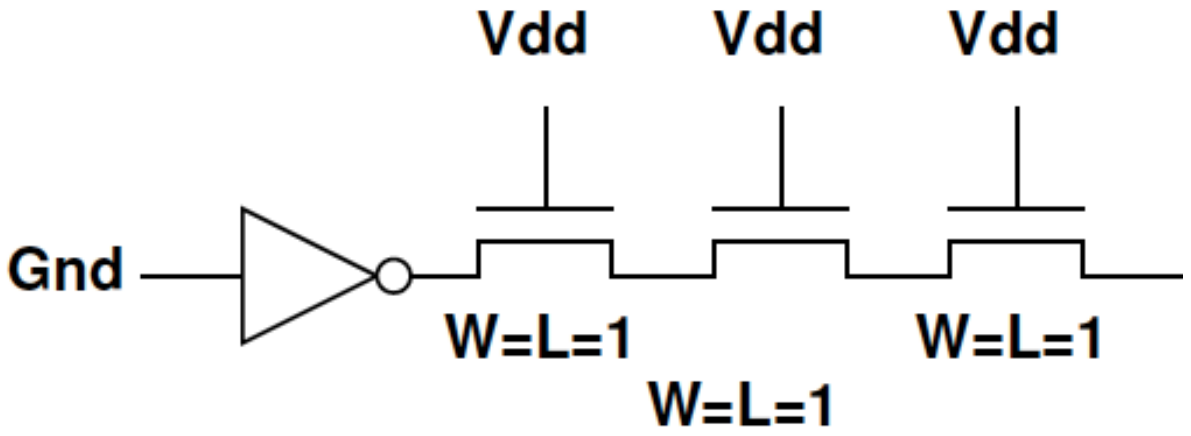
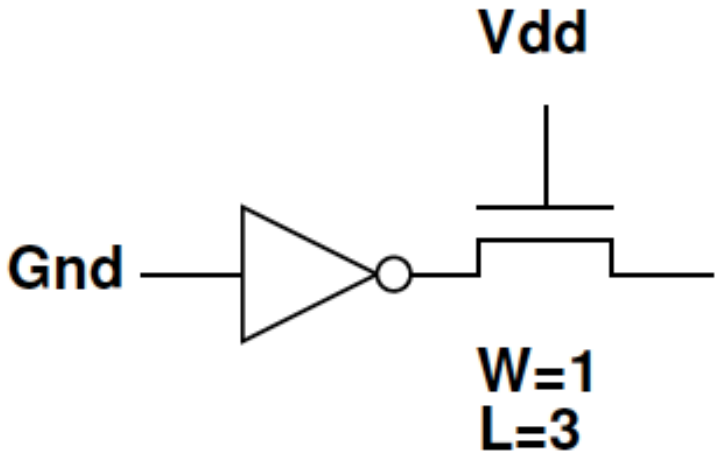


How compare (Preclass 2)

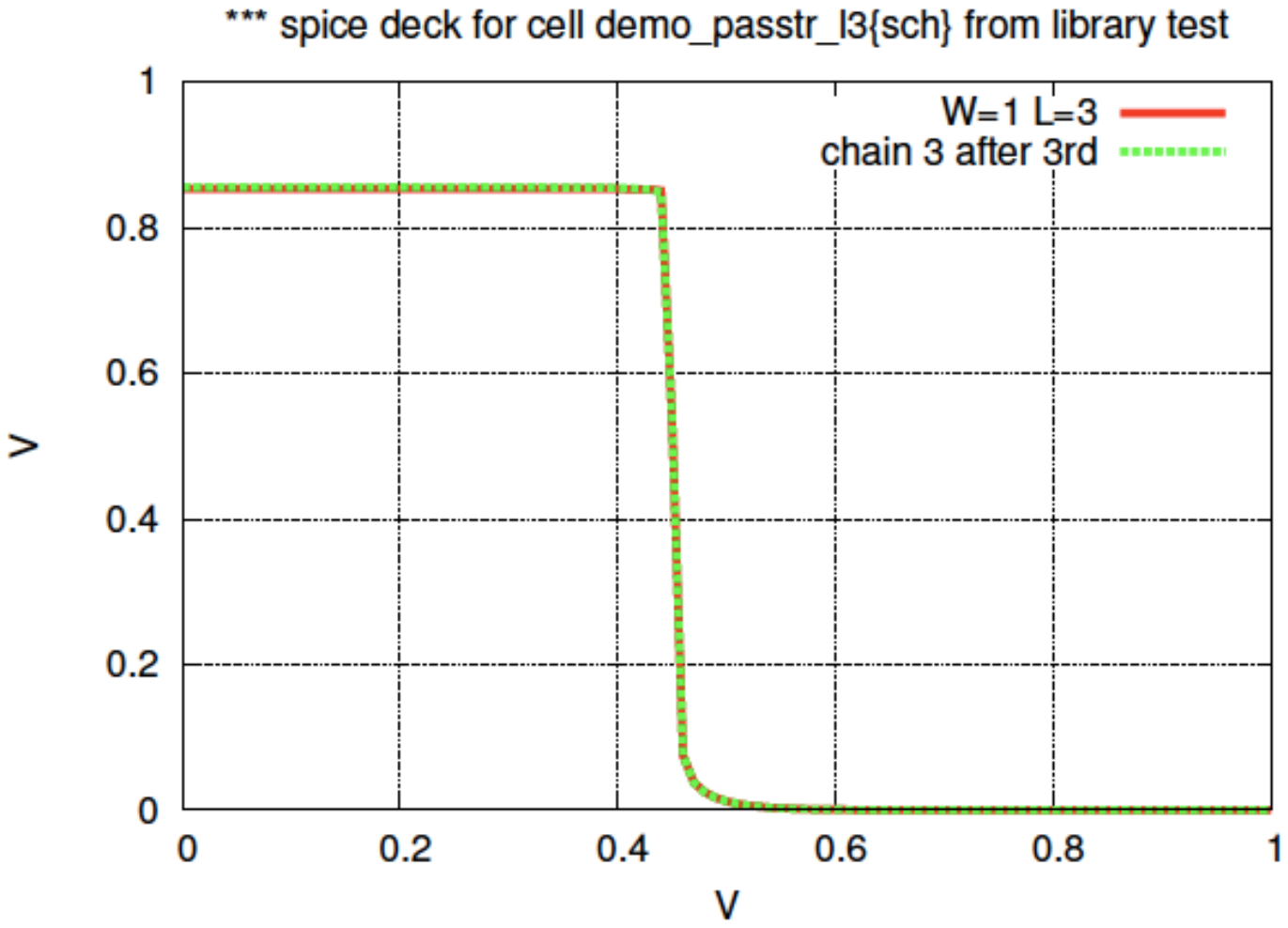
- Compare

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



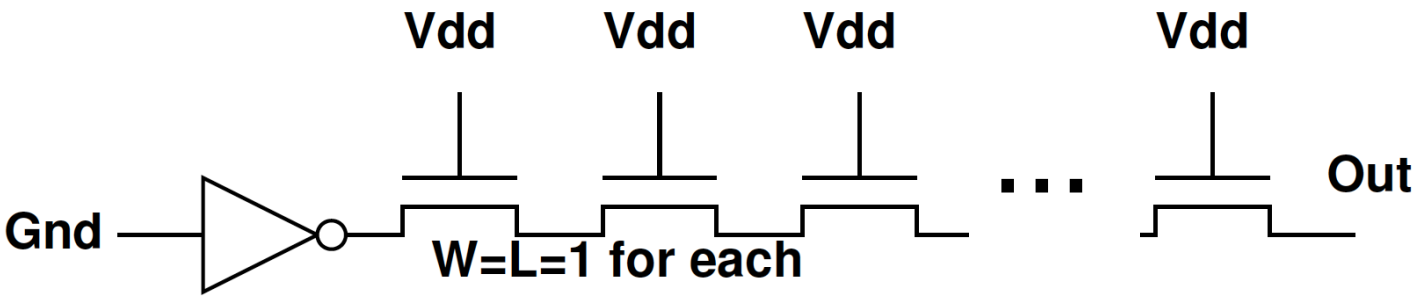


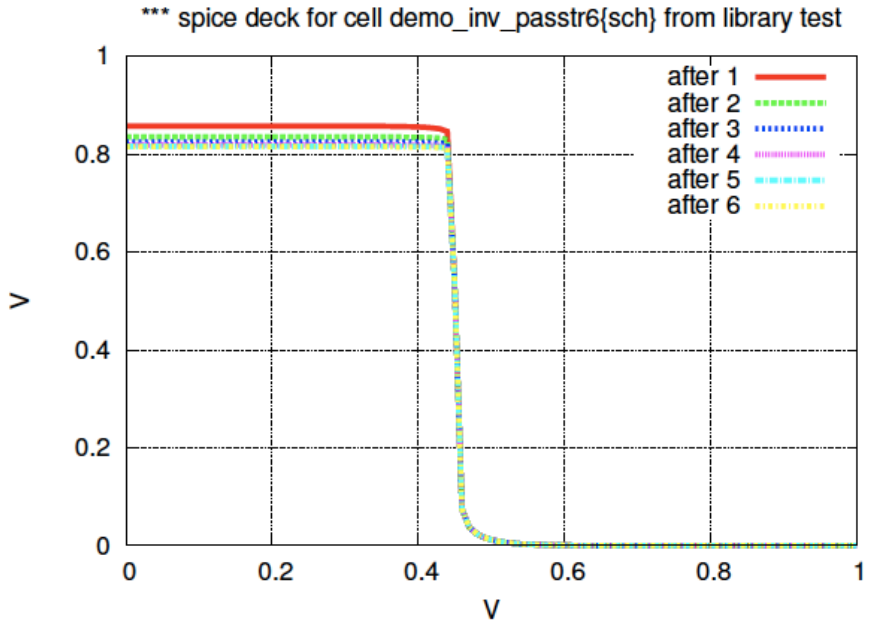
DC Analysis – chain of 3 vs length of 3



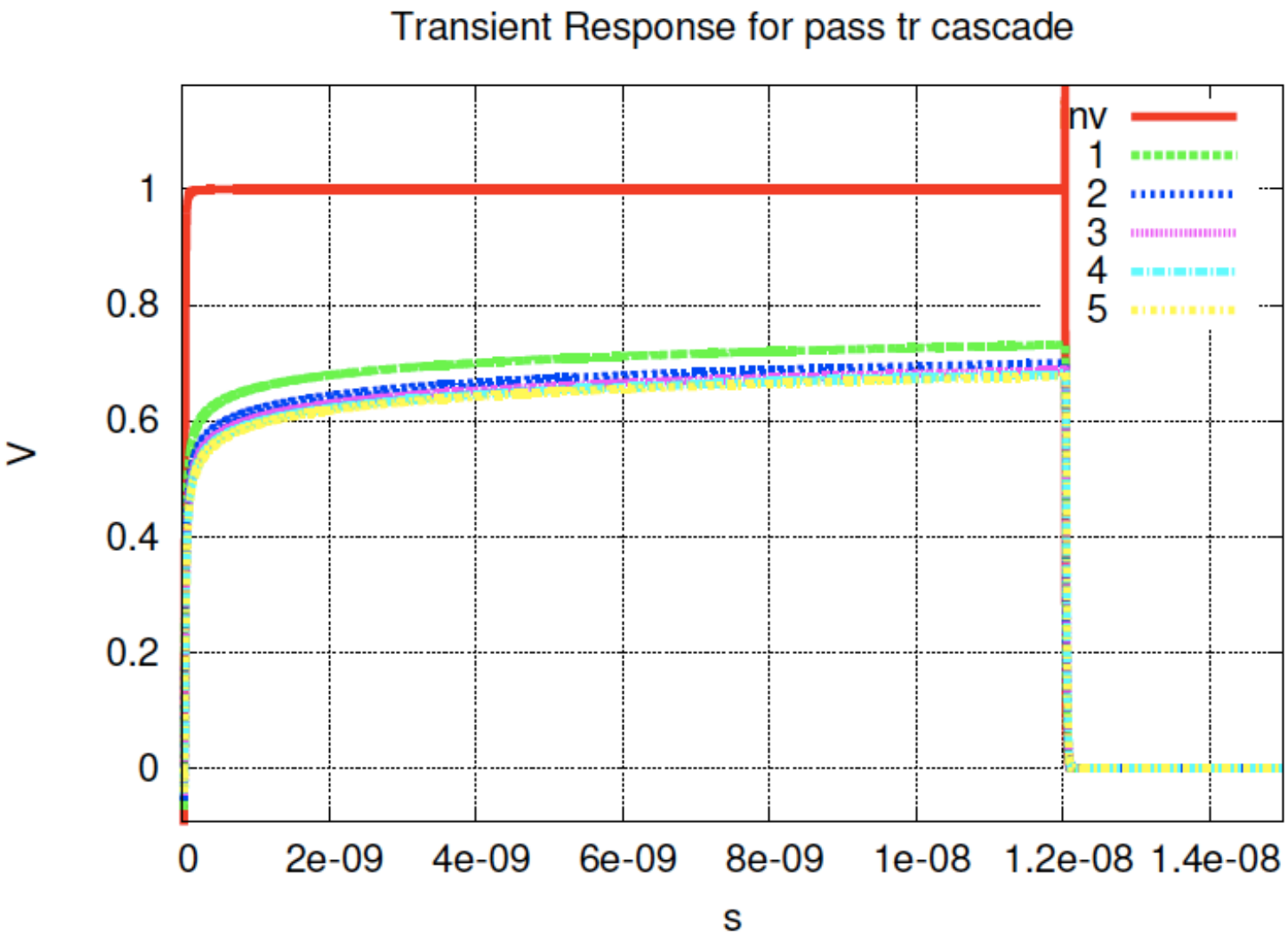
Conclude

- Can chain any number of pass transistors and only drop a single V_{th}

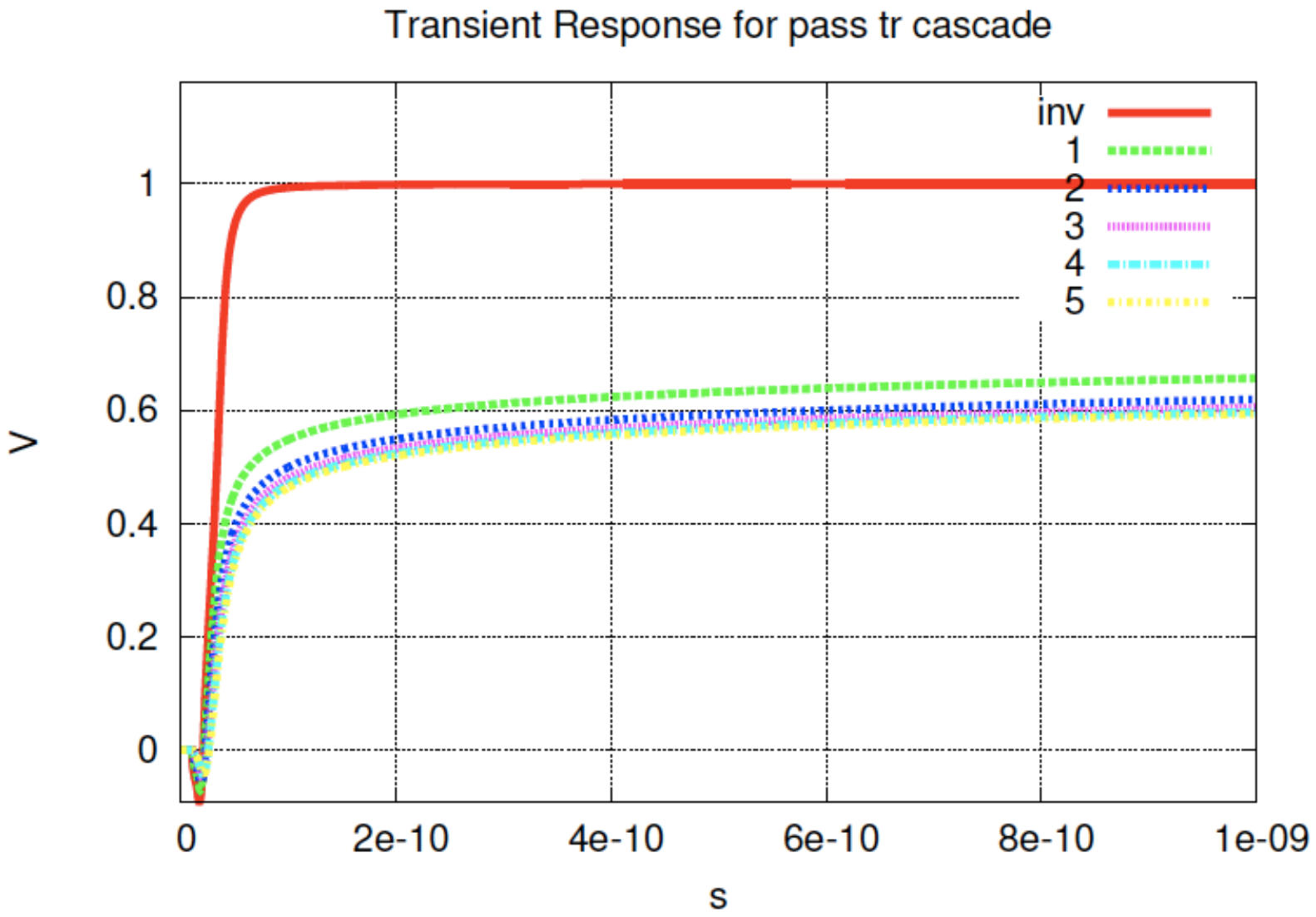




Transient

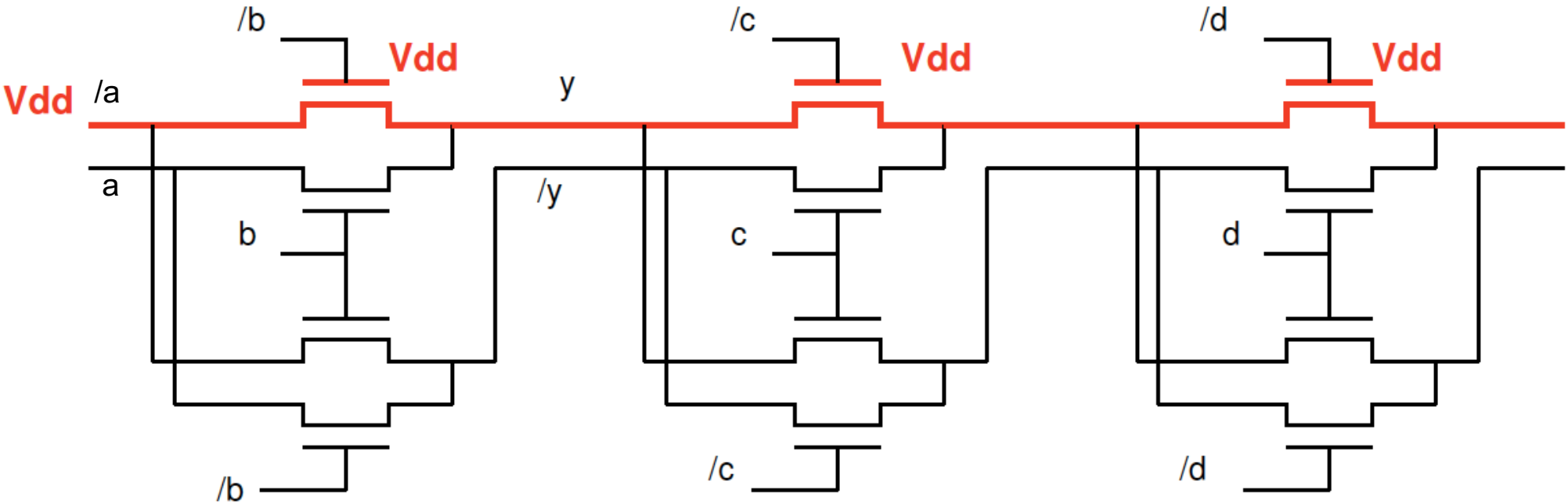

Transient Response for pass tr cascade
nv
1
2
3
4
5
V
1
0.8
0.6
0.4
0.2
0
0
2e-09
4e-09
6e-09
8e-09
1e-08
1.2e-08
1.4e-08
s

Transient: Zoomed Closeup



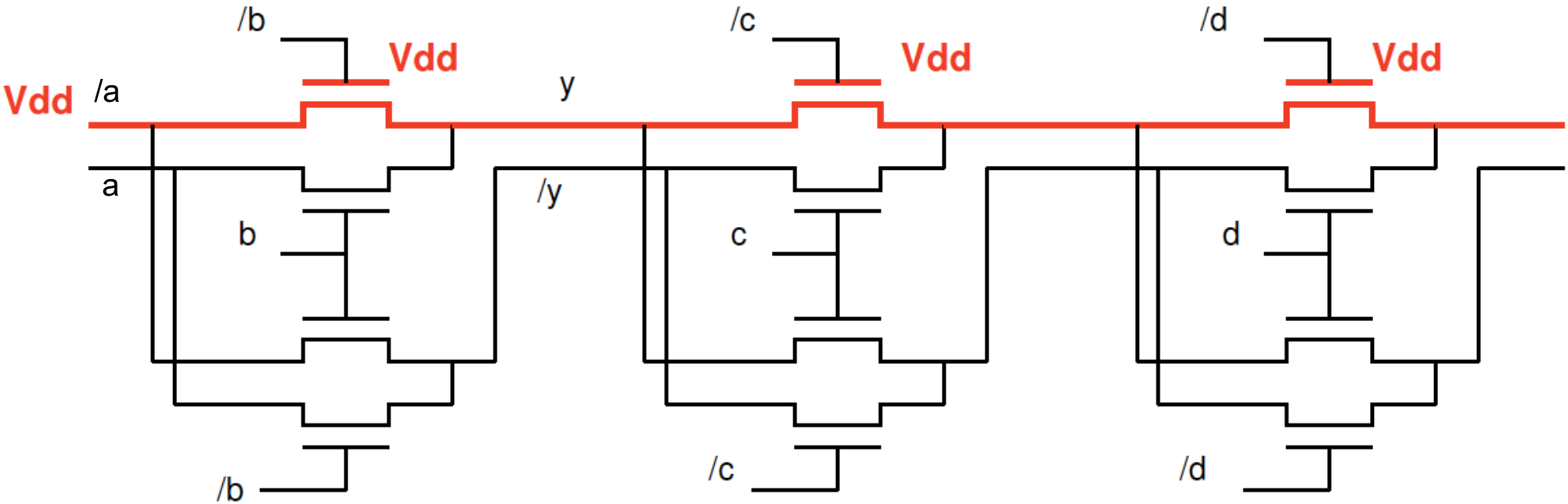
Capacitance

- What is output capacitance per stage?
  - I.e. What is the capacitance at output y?



Delay Setup

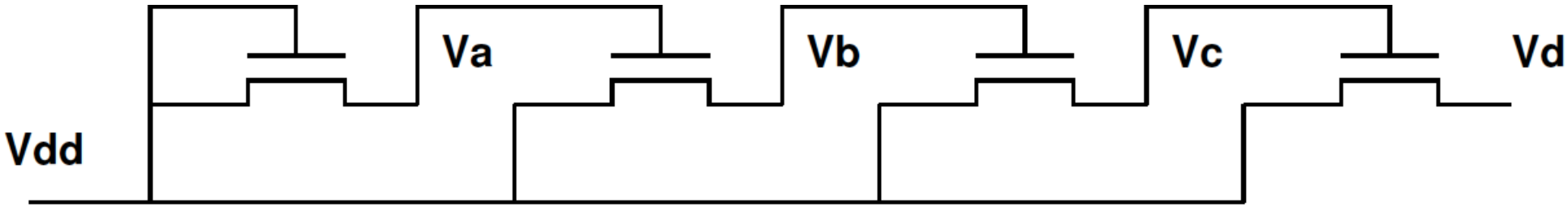
- What does RC circuit look like?



Gate Cascade? (Preclass 3)

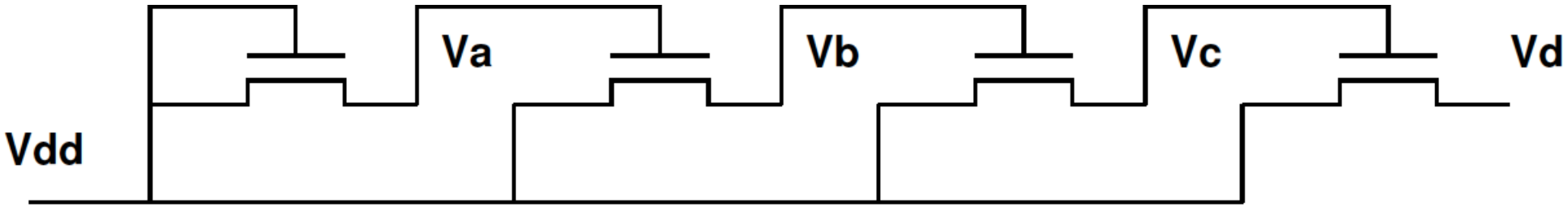
- What are the voltages?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



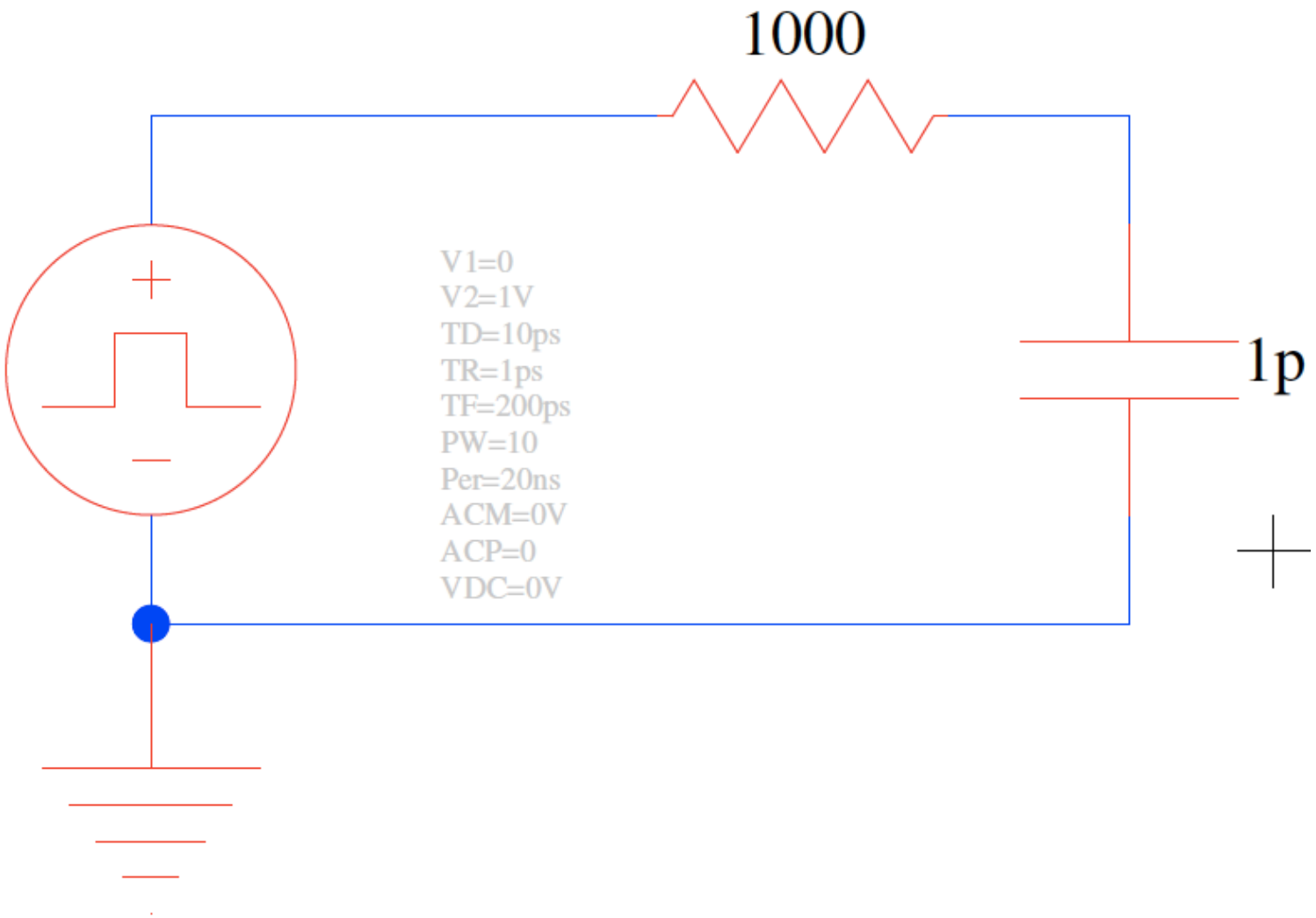
Conclude

- Cannot cascade degraded inputs into **gates**.



Distributed RC (setup)

What is response? (Preclass 4)



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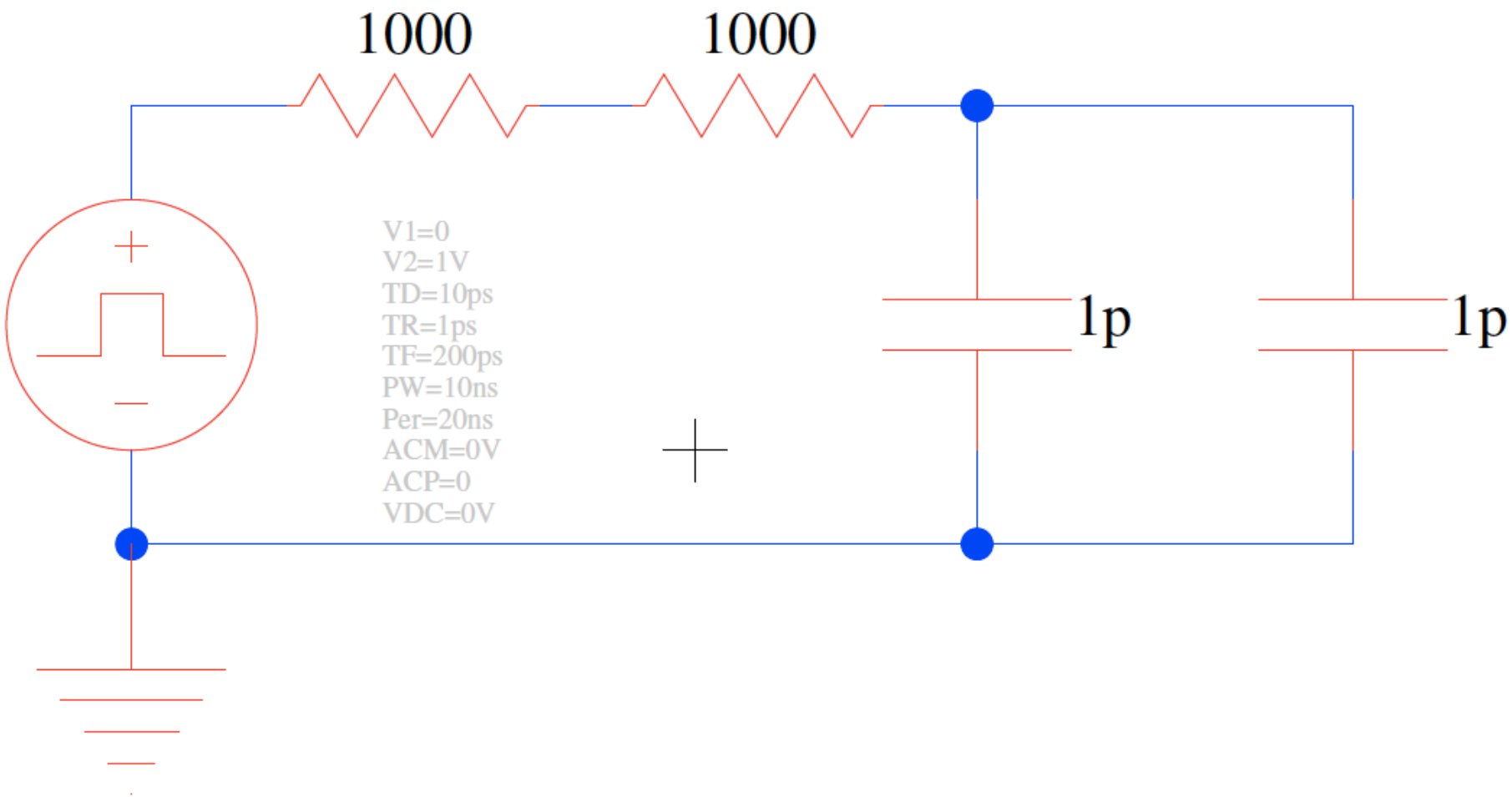
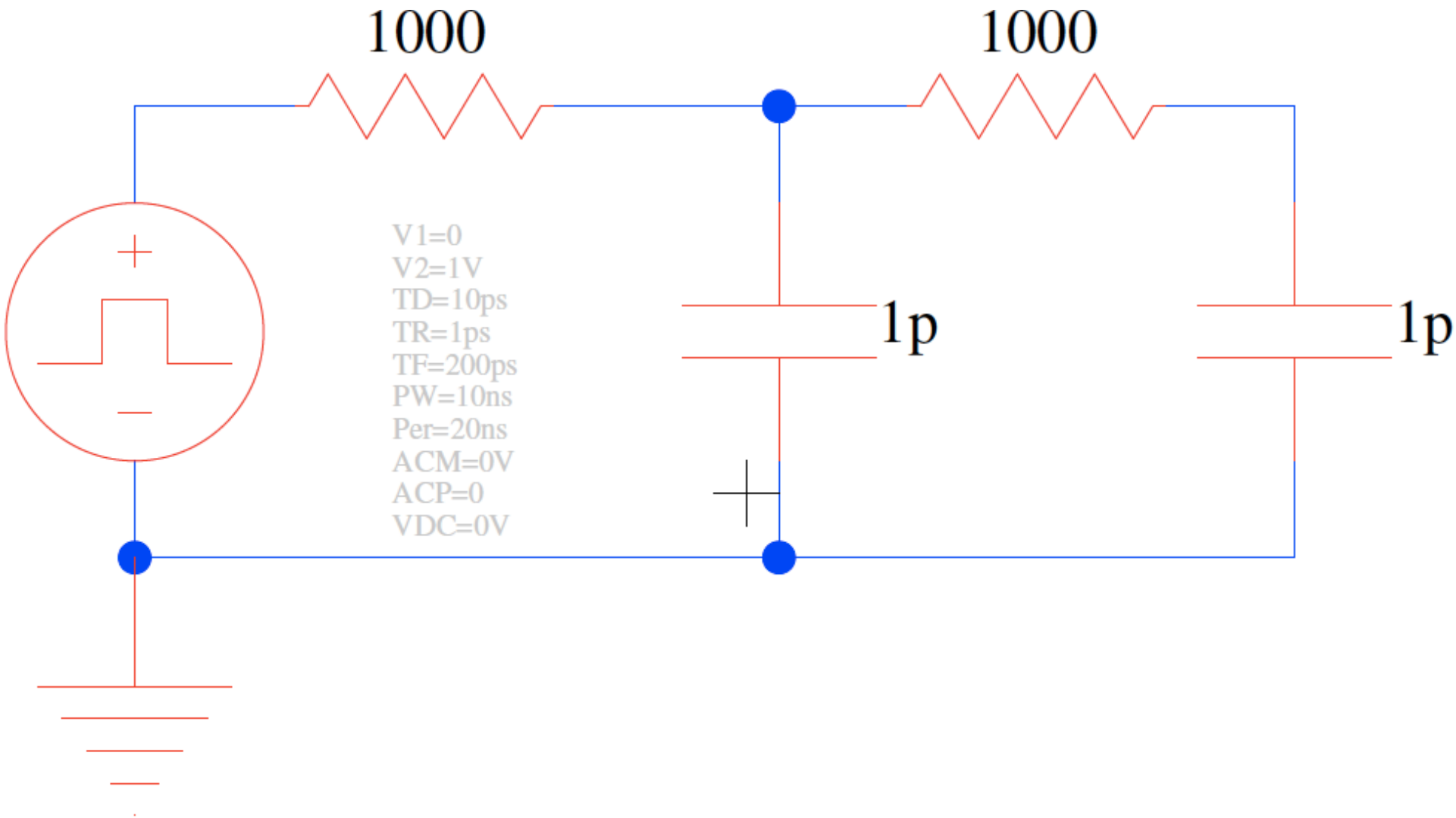
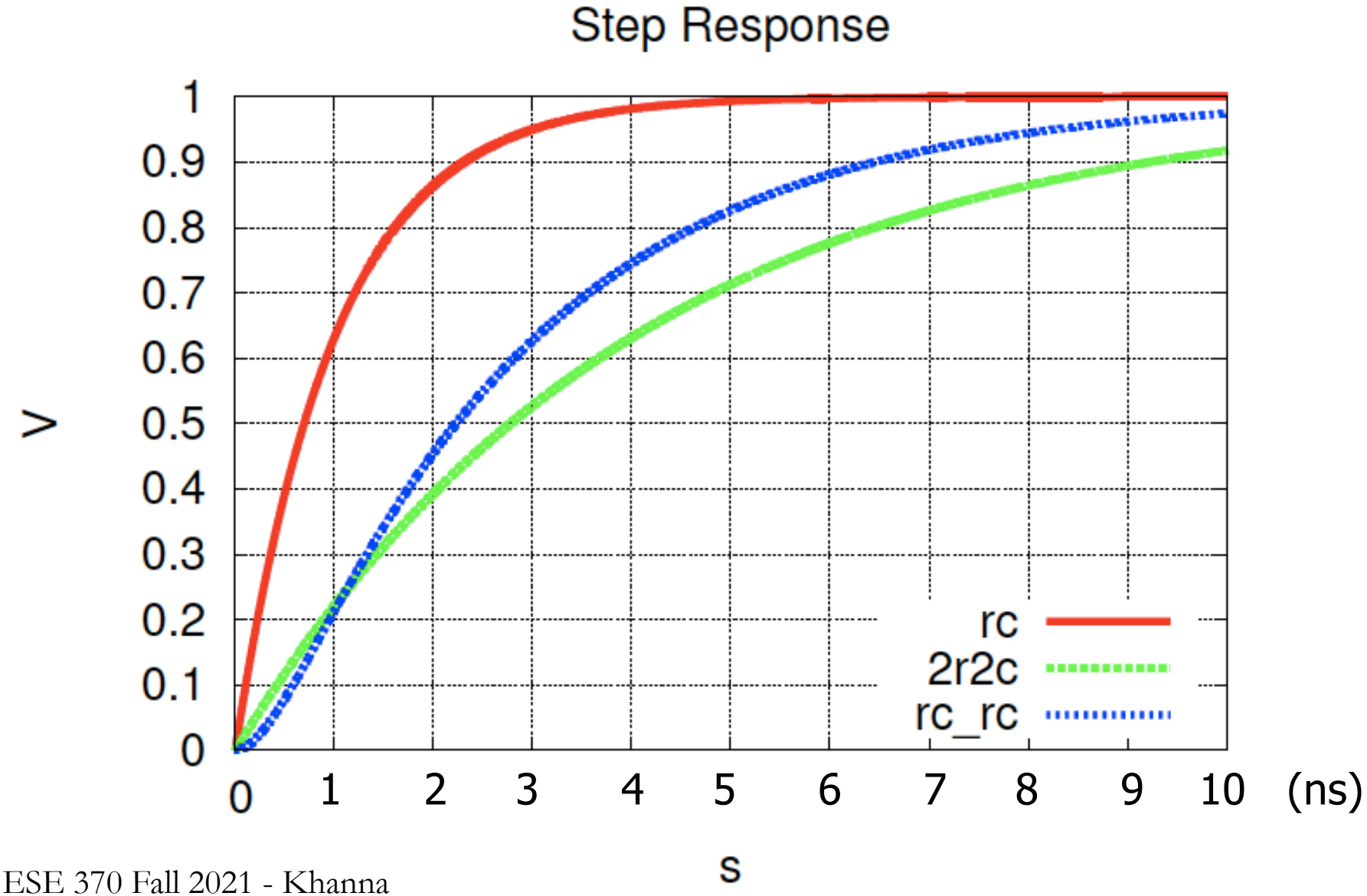


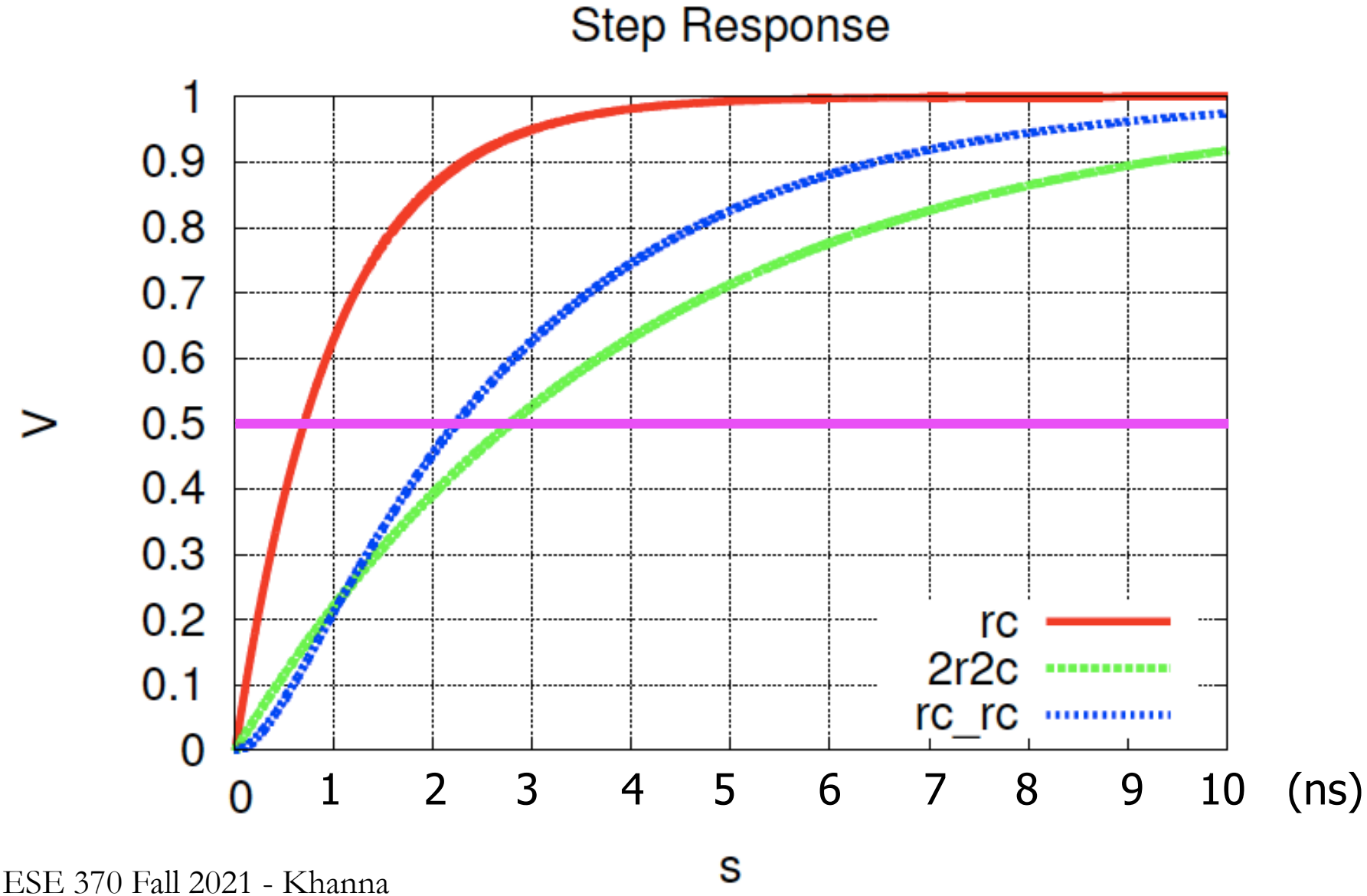
What is response? (Preclass 4)



SPICE Response

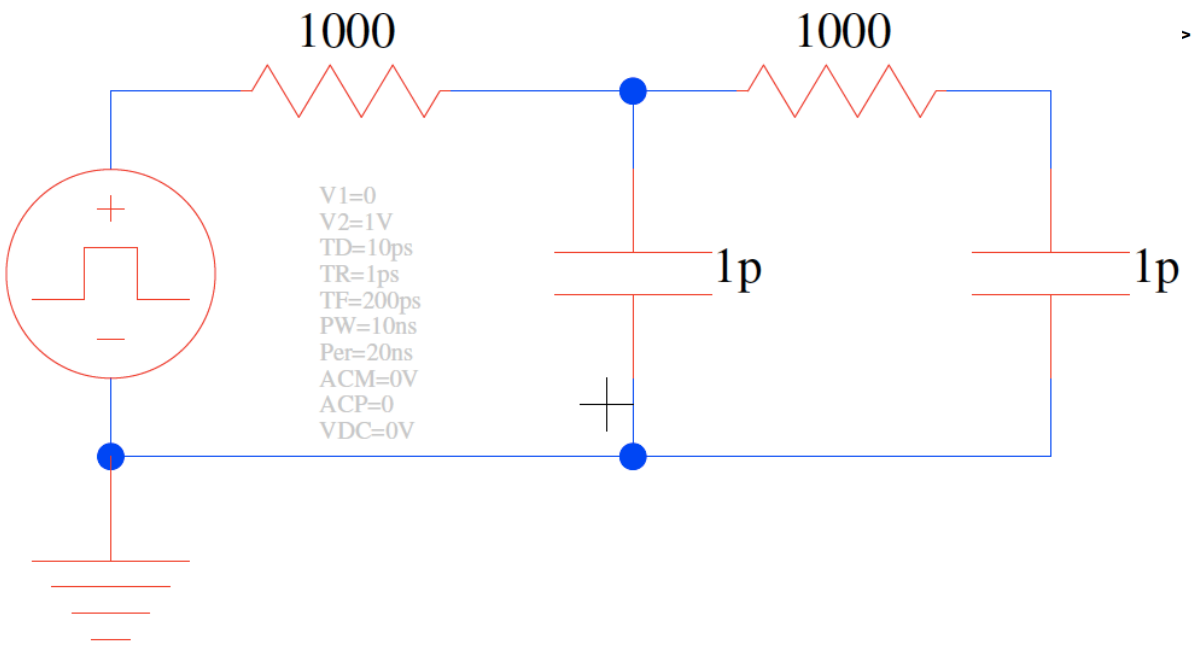


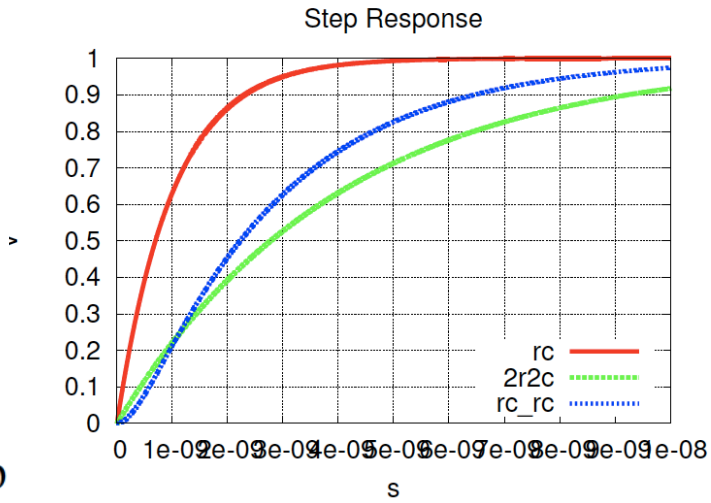
SPICE Response



Intuition

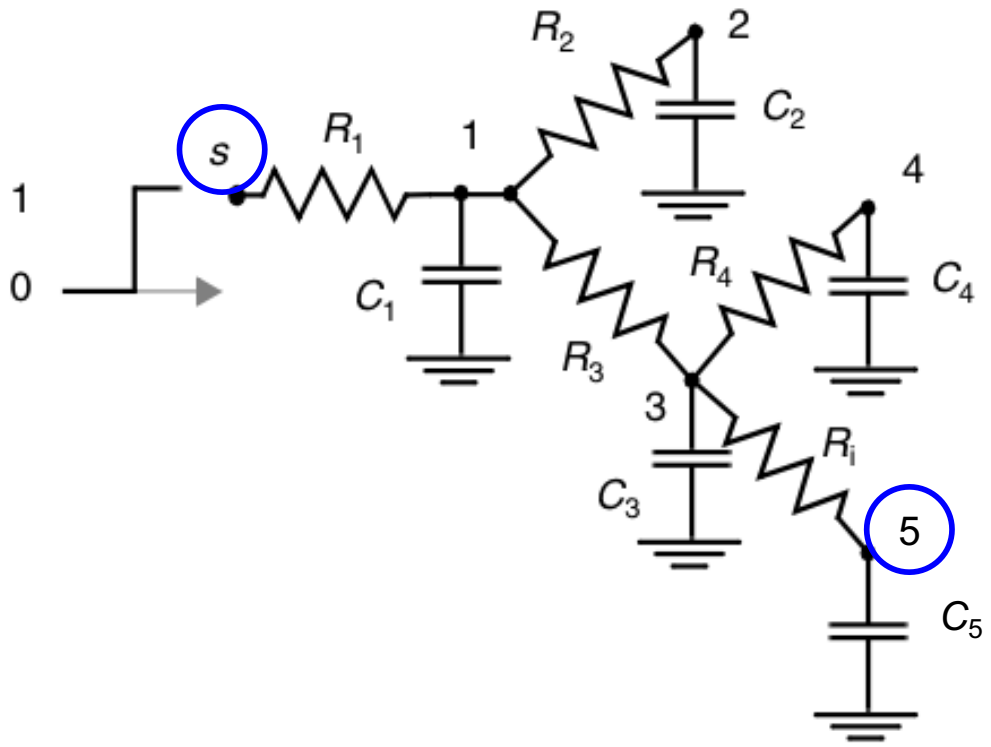
- Look at series of R's on path
  - Must move Q=V(ΣC) across each R





Elmore Delay: Distributed RC network

- The delay from source *s* to node *5*
  - N = number of nodes in circuit



Elmore Delay: Distributed RC network

- The delay from source *s* to node *5*
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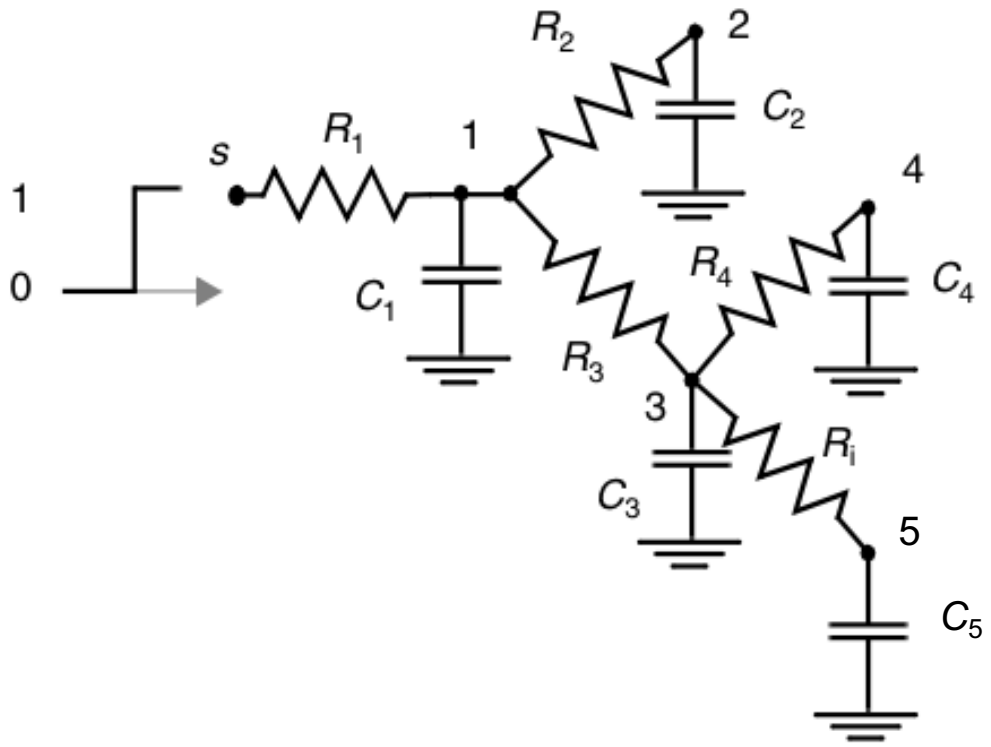
$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow 5) \cap path(s \rightarrow k)])$$

$$\tau_{D5} = \sum_{k=1}^{N} C_k R_{5k}$$



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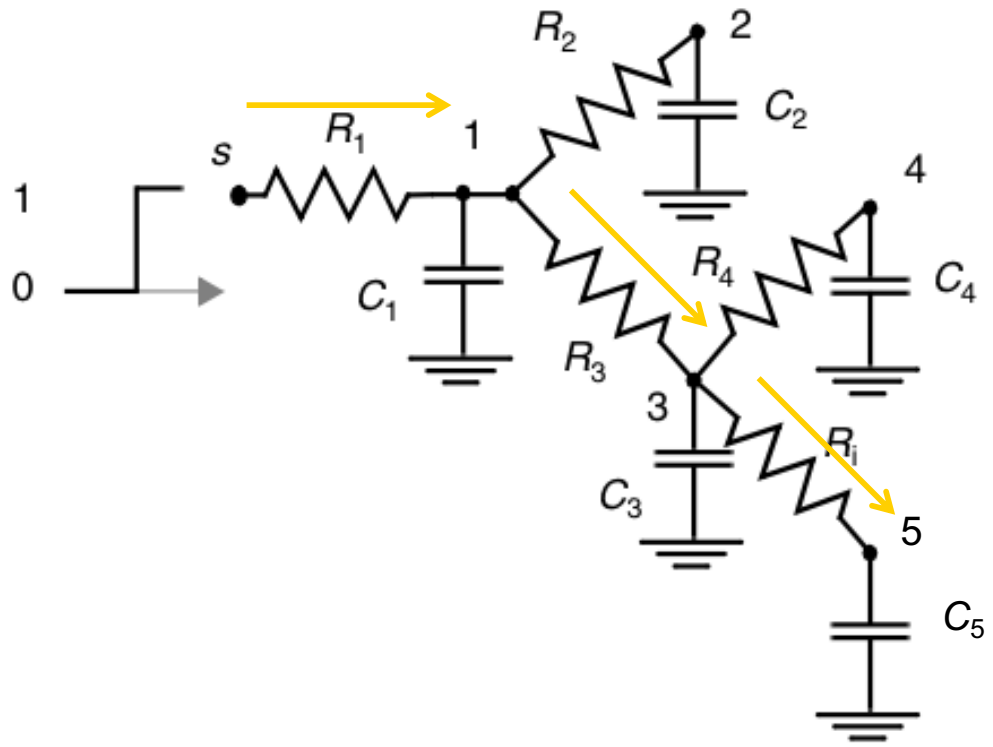

Elmore Delay: Distributed RC network

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k=4

$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow 5) \cap path(s \rightarrow k)])$$

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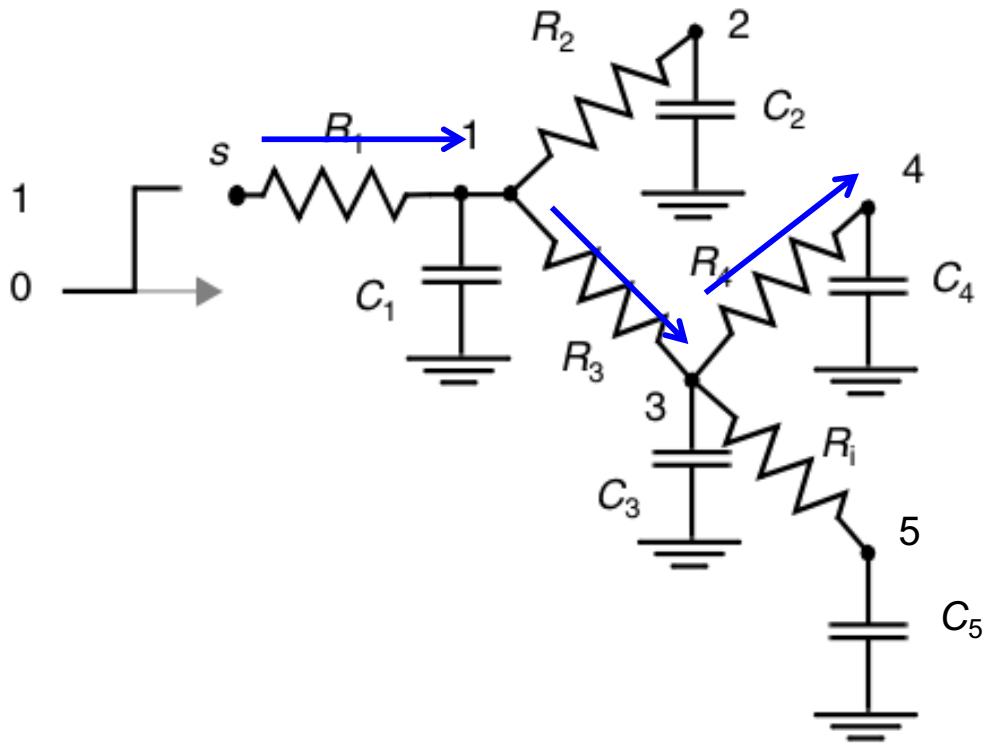

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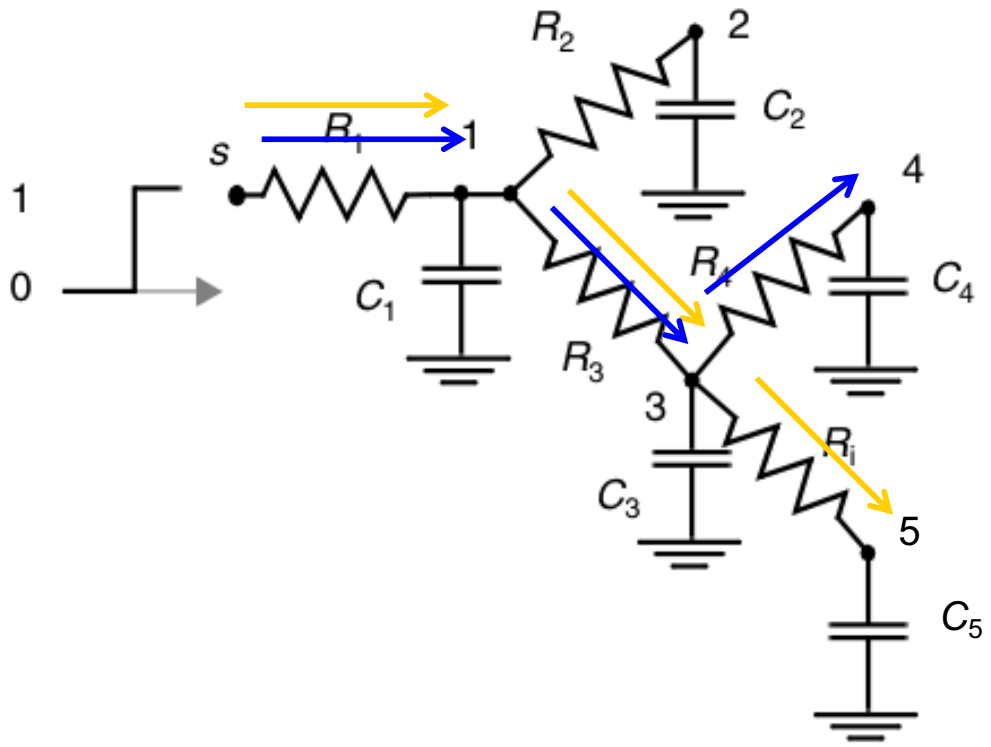

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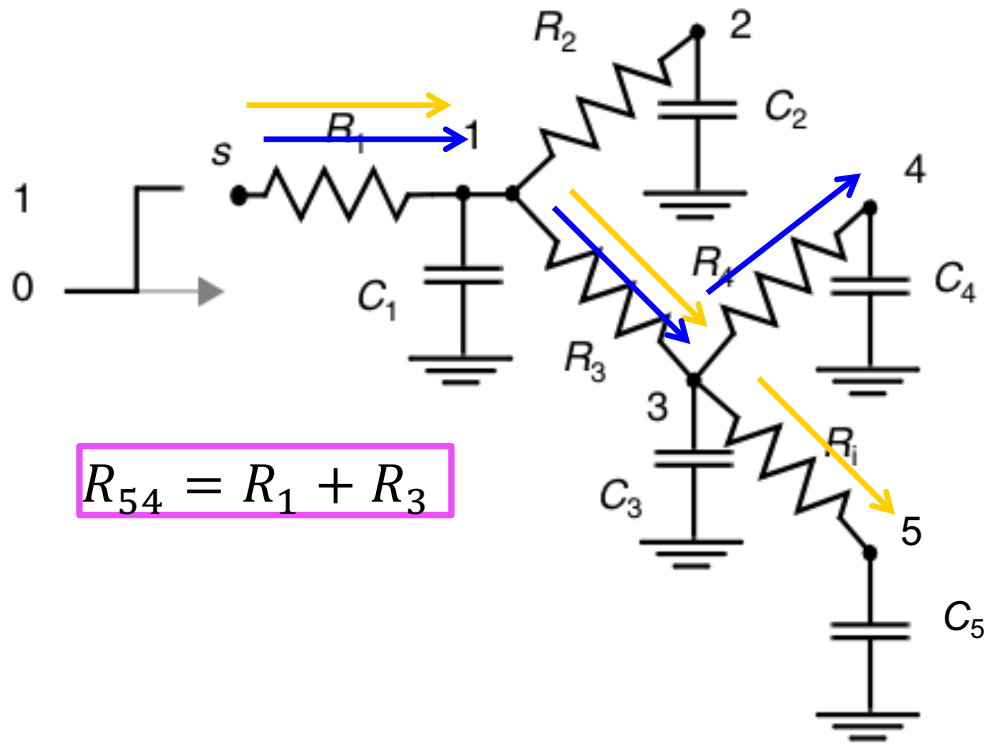

$R_{54} = R_1 + R_3$

Elmore Delay: Distributed RC network

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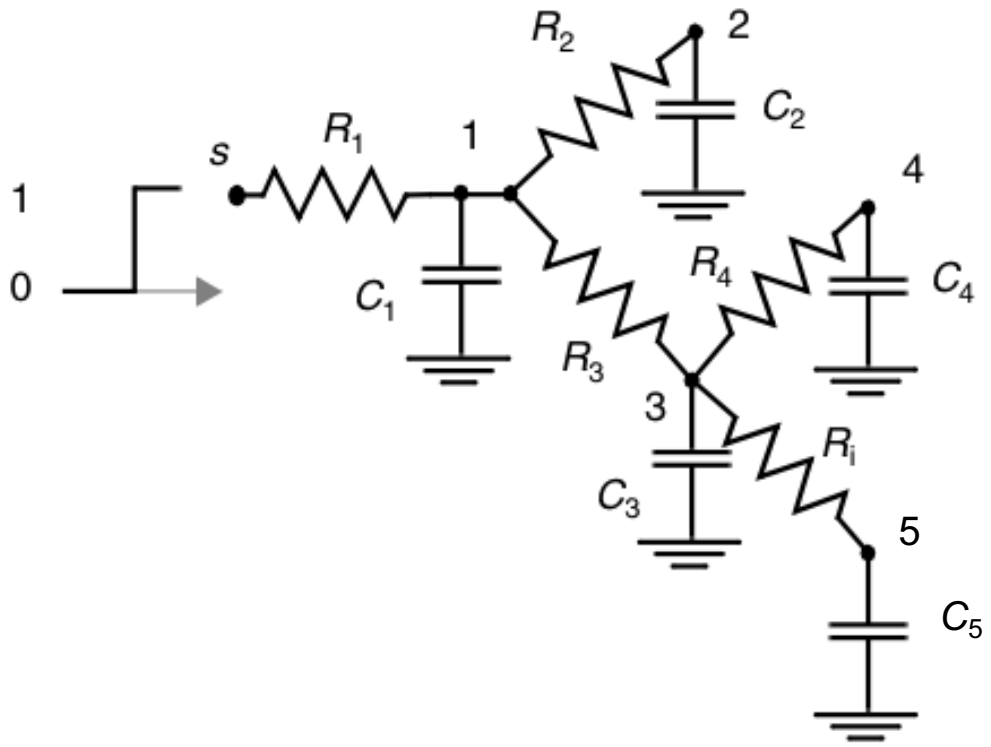
$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow 5) \cap path(s \rightarrow k)])$$

$$\tau_{D5} = \sum_{k=1}^{N} C_k R_{5k} = ?$$

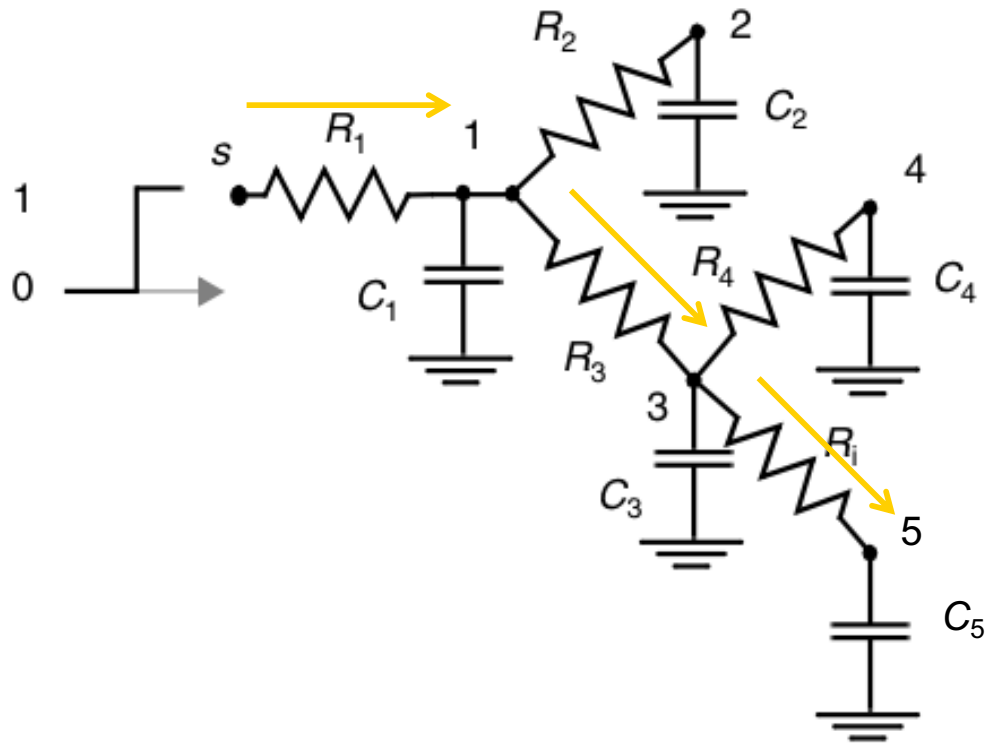


Elmore Delay: Distributed RC network

- The delay from source *s* to node *5*
  - N = number of nodes in circuit

$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow 5) \cap path(s \rightarrow k)])$$

$$\tau_{D5} = \sum_{k=1}^{N} C_k R_{5k} = ?$$

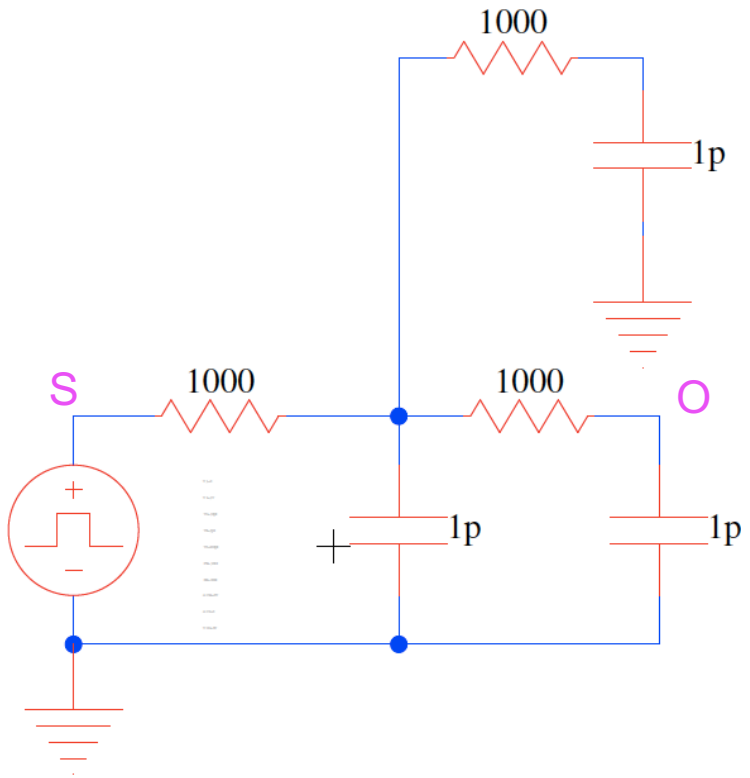


Elmore Delay: Practice

- The delay from source s to node O
  - N = number of nodes in circuit

$$R_{Ok} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow O) \cap path(s \rightarrow k)])$$

$$\tau_{DO} = \sum_{k=1}^{N} C_k R_{Ok} = ?$$



Idea

- There are other circuit disciplines
- Can use pass transistors for logic
  - Even chains of pass transistors
  - Mostly gives area win, sometimes gives delay win
    - Will talk more about delay on Monday
- Do not cascade as easily as CMOS
- Additional diffusion capacitance leads to distributed RC networks
  - More next lecture

Logic Types

- CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- Pass Gates
  - Implement logic gate as switch network for reduced area and load capacitance
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins (V_T drop)
    - Use level-restoring buffers to improve noise margins

- Dynamic logic … coming up soon

Admin

- Project 1
  - Milestones were mostly all good
    - Show me the results! Justify all metrics
  - Use Piazza and office hours
  - Should be working hard on project
    - Not enough to know what to do. You have to actually do it.
  - Rewarding experience and worth the time once you get it
    - Design and test takes time