ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 22: October 29, 2021

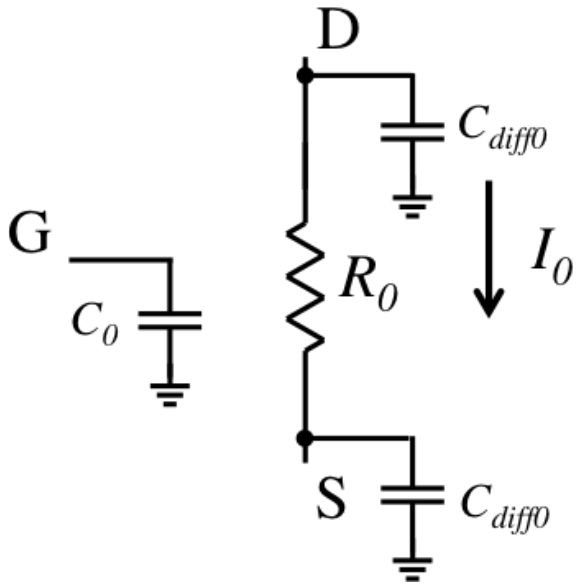
CMOS Worst Case Analysis and Logic Type Comparisons

Lecture Outline

- Pass transistor Round-up
- CMOS Gates Review
  - CMOS Worst Case Analysis
- Logic Type Comparisons

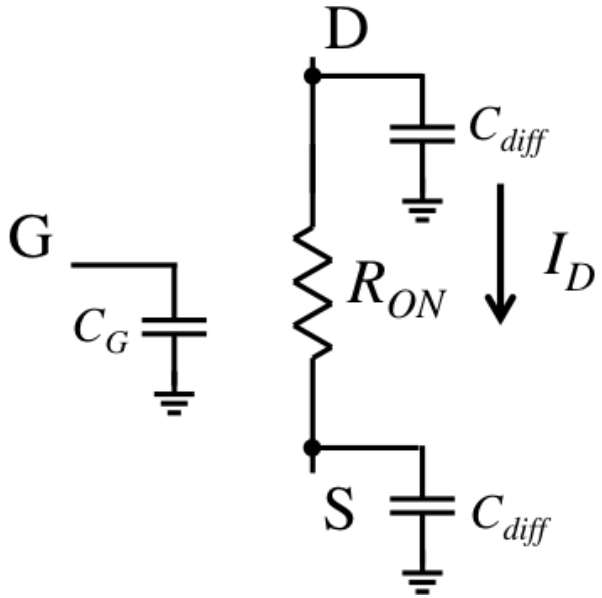
Previously: First Order Delay

- R_0 = Resistance of minimum size NMOS device
- $I_0 = I_{ds}$ of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- C_{diff0} = diffusion capacitance of minimum size NMOS device
  - $C_{diff0} = \gamma C_0$



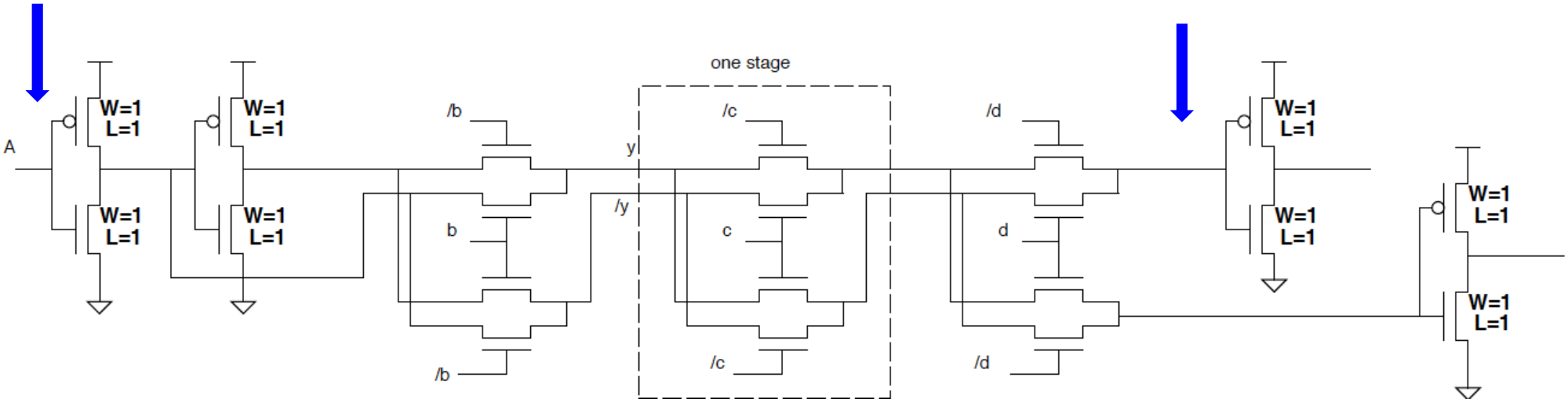
Previously: First Order Delay

- For device of width W (multiple of minimum size)
- $R_{ON} = R_0/W$
- $I_D = W*I_0$
- $C_G = W*C_0$
- $C_{diff} = W*C_{diff0}$
  - $C_{diff} = W*\gamma C_0$



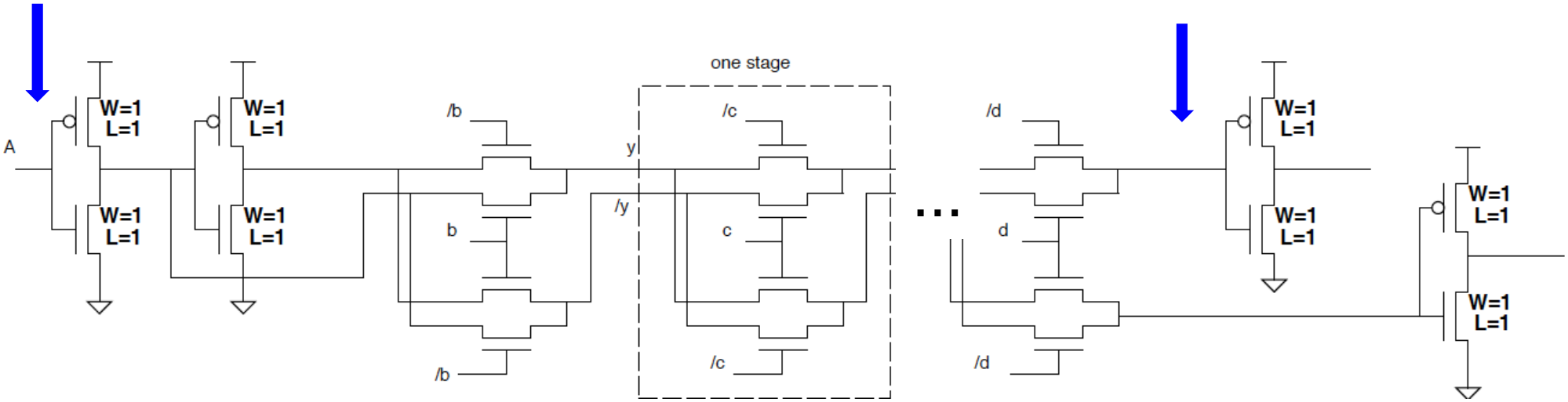
Unbuffered

- Circuit → Delay?
  - 3 stages



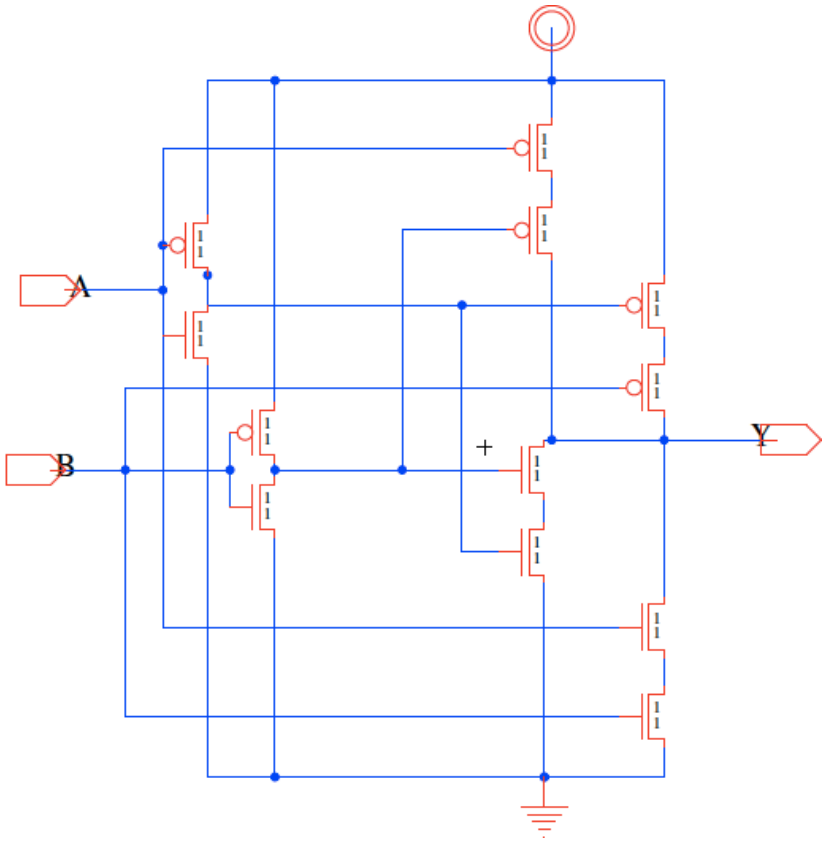
Unbuffered

- Delay as a function of number of stages, k?

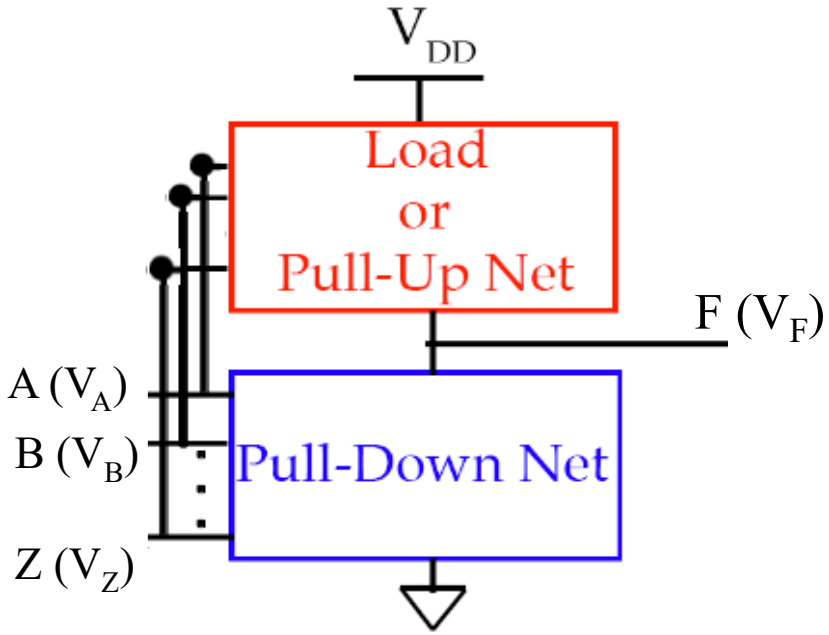


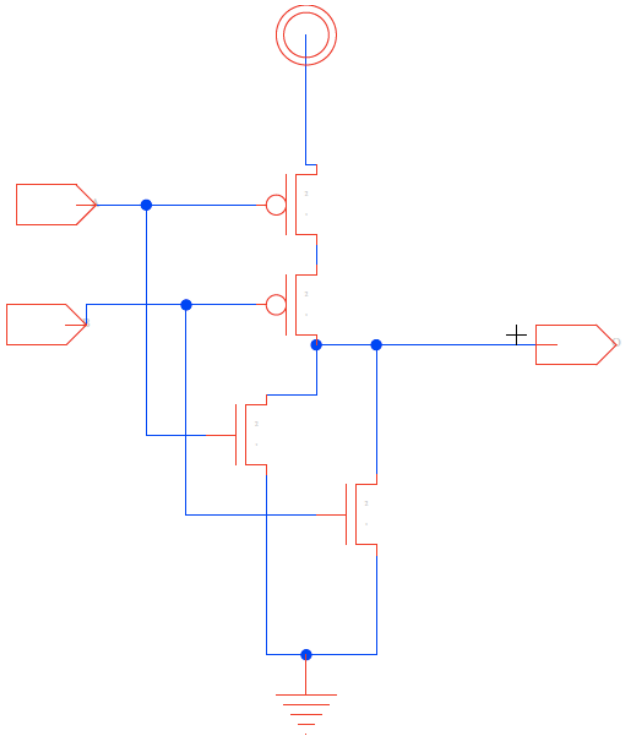
CMOS XOR

- Delay with Cdiff>0?



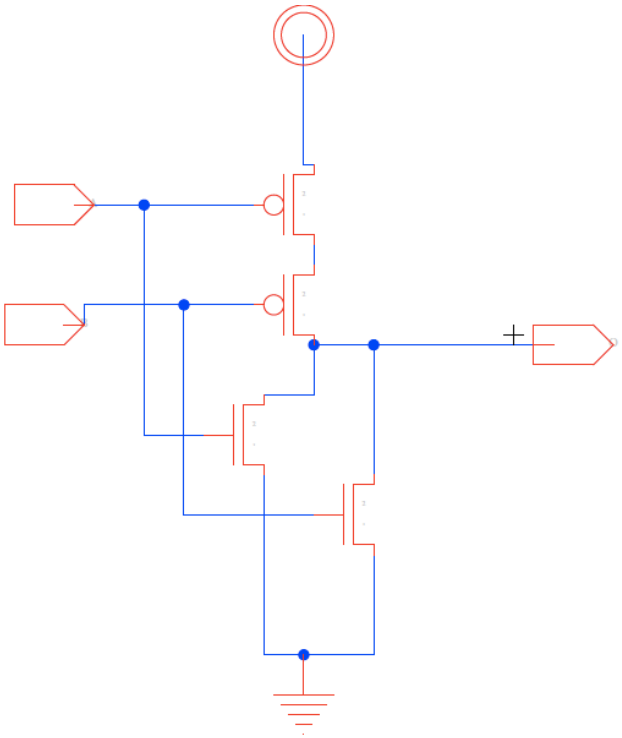
Review: Two-Input NOR Gate (NOR2)

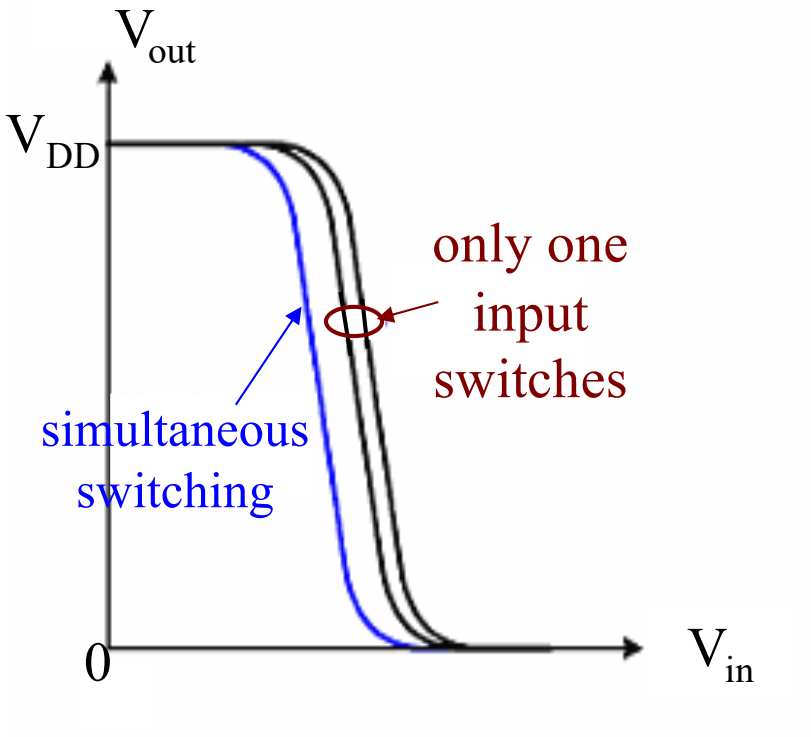




- Worst case delay of NOR2?
  - Minimum size, Loaded with itself

NOR2 Transfer Curve





3 VTC Cases

$V_1 = 0$ V; $V_2 = 0 \rightarrow V_{DD}$

$V_1 = 0 \rightarrow V_{DD}$; $V_2 = 0$

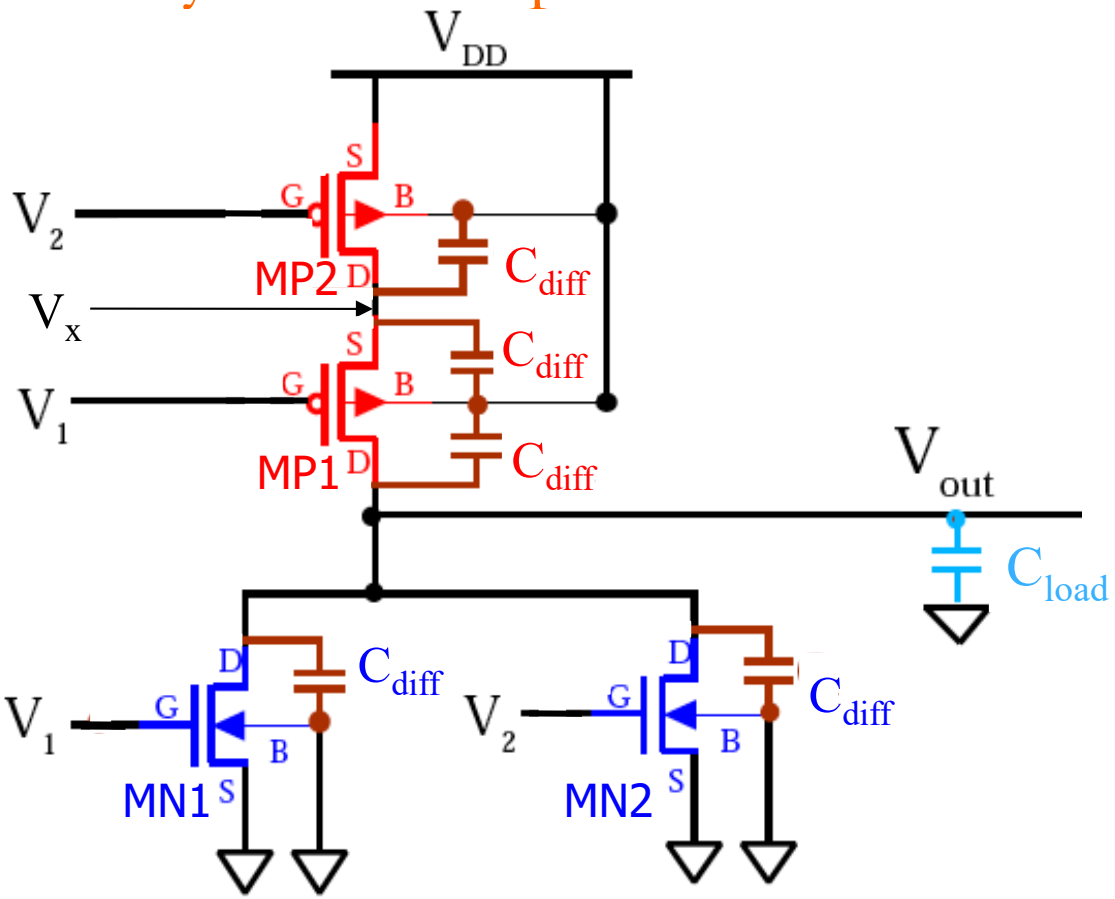
V_1 and $V_2 = 0 \rightarrow V_{DD}$ simultaneously

Switching Threshold Voltage:

$V_1 = V_2 = V_{out} = V_t$

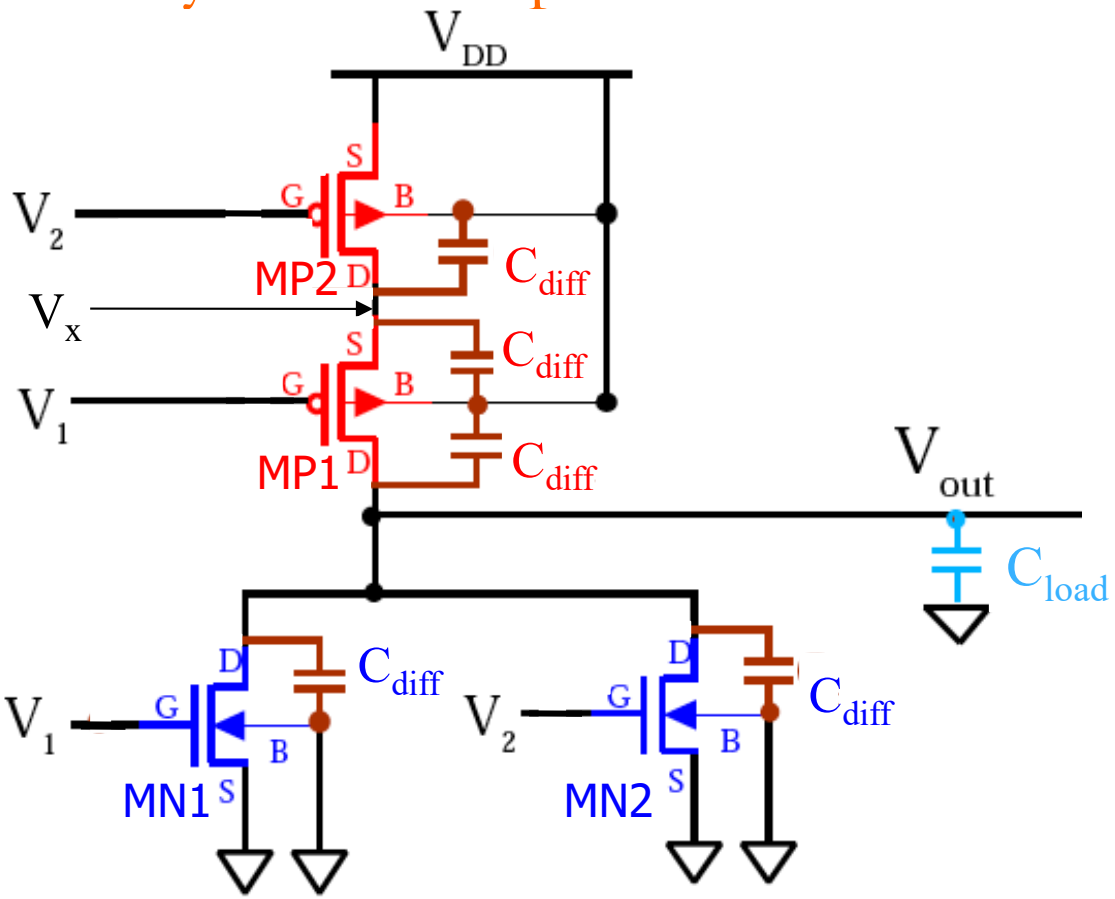
NOR2 Delay (preclass 1)

- Worst case delay for Pull-up?



NOR2 Delay

- Worst case delay for Pull-up?



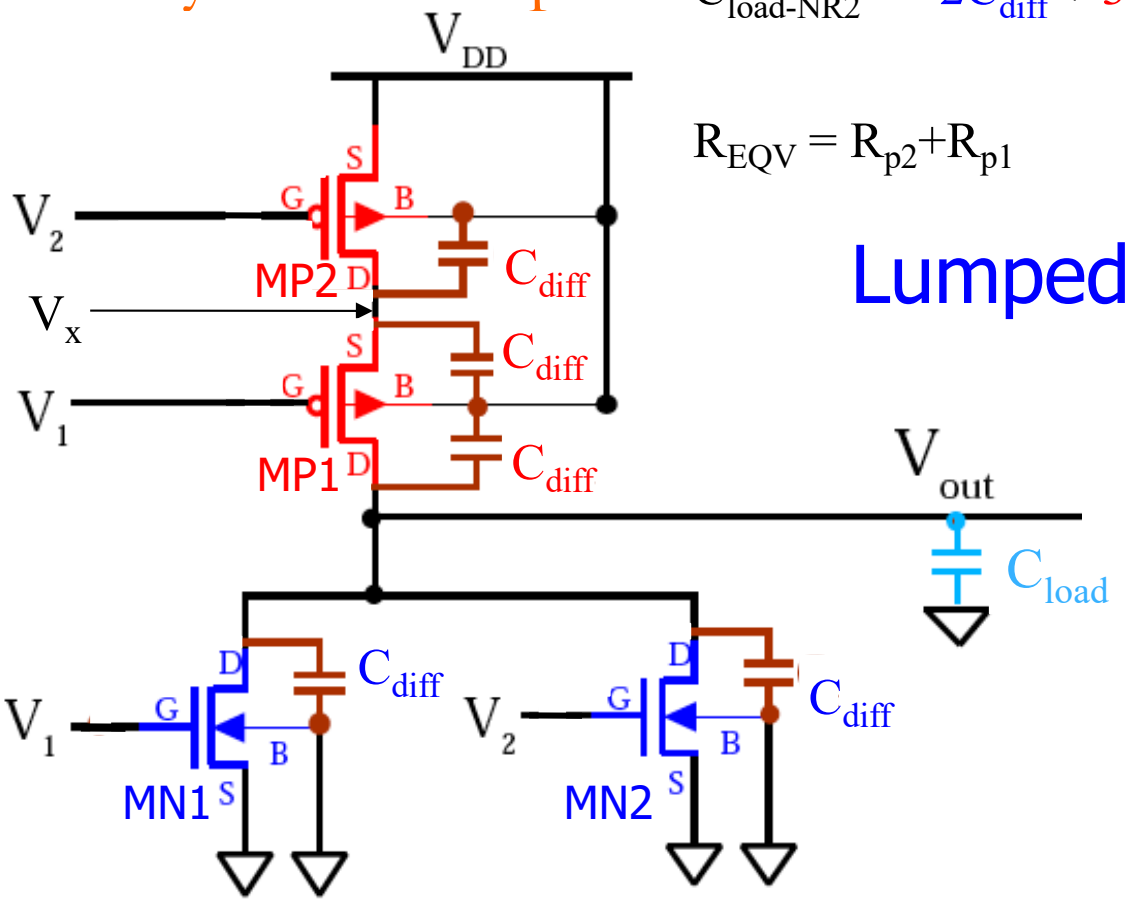
Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

NOR2 Delay

- Worst case delay for Pull-up?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load}$

$R_{EQV} = R_{p2} + R_{p1}$



Lumped Model

Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

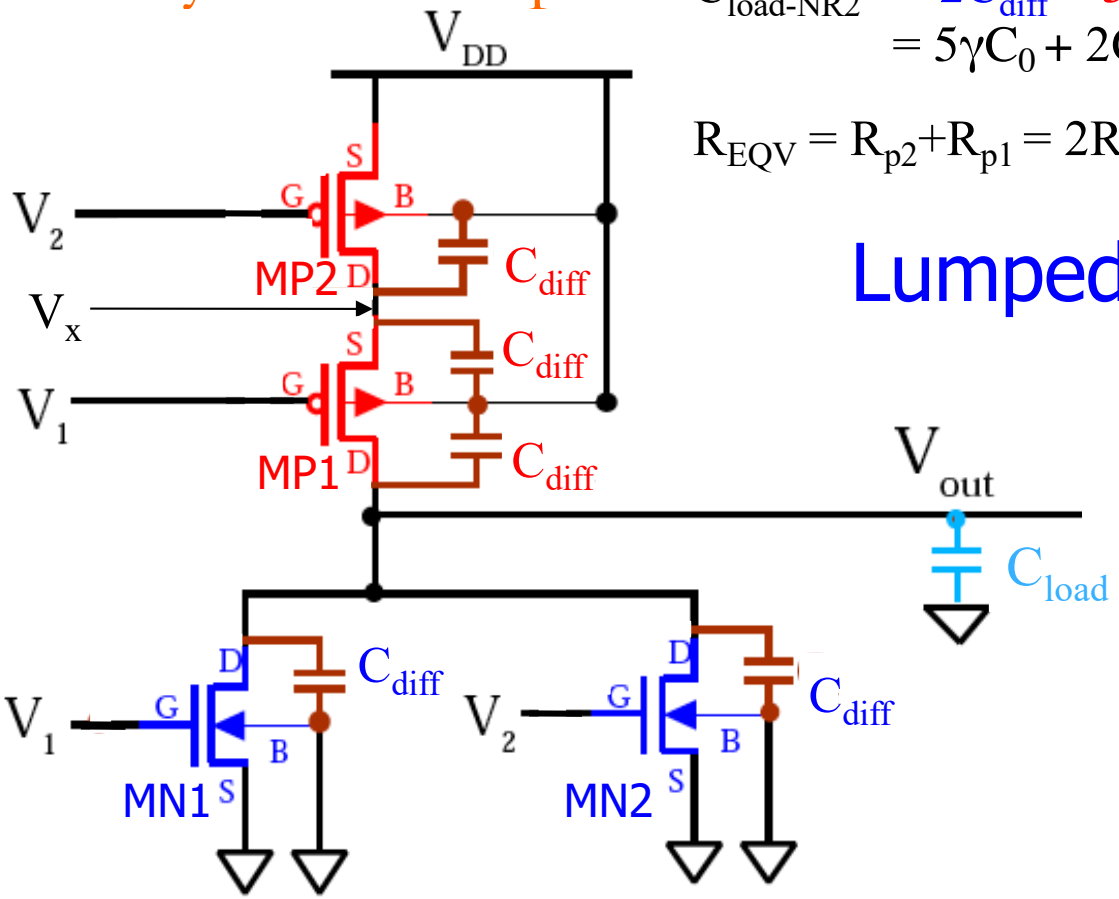
NOR2 Delay

- Worst case delay for Pull-up?

$$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load} = 5\gamma C_0 + 2C_0$$

$$R_{EQV} = R_{p2} + R_{p1} = 2R_0$$

Lumped Model



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

$$delay = (5\gamma C_0 + 2C_0)(2R_0) = (10\gamma + 4)\tau$$

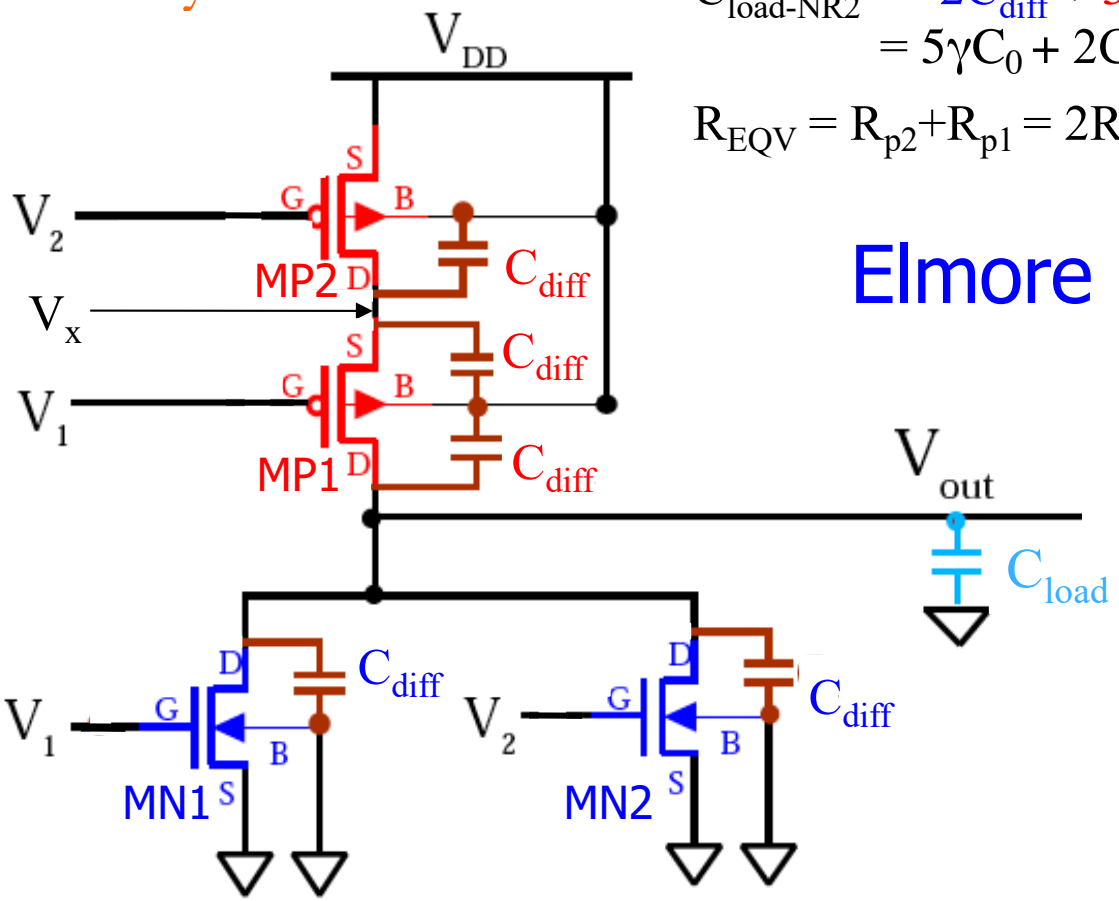
NOR2 Delay

- Worst case delay?

$$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load}$$
$$= 5\gamma C_0 + 2C_0$$

$$R_{EQV} = R_{p2} + R_{p1} = 2R_0$$

Elmore Model?



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

NOR2 Delay

- Worst case delay?

$$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load}$$
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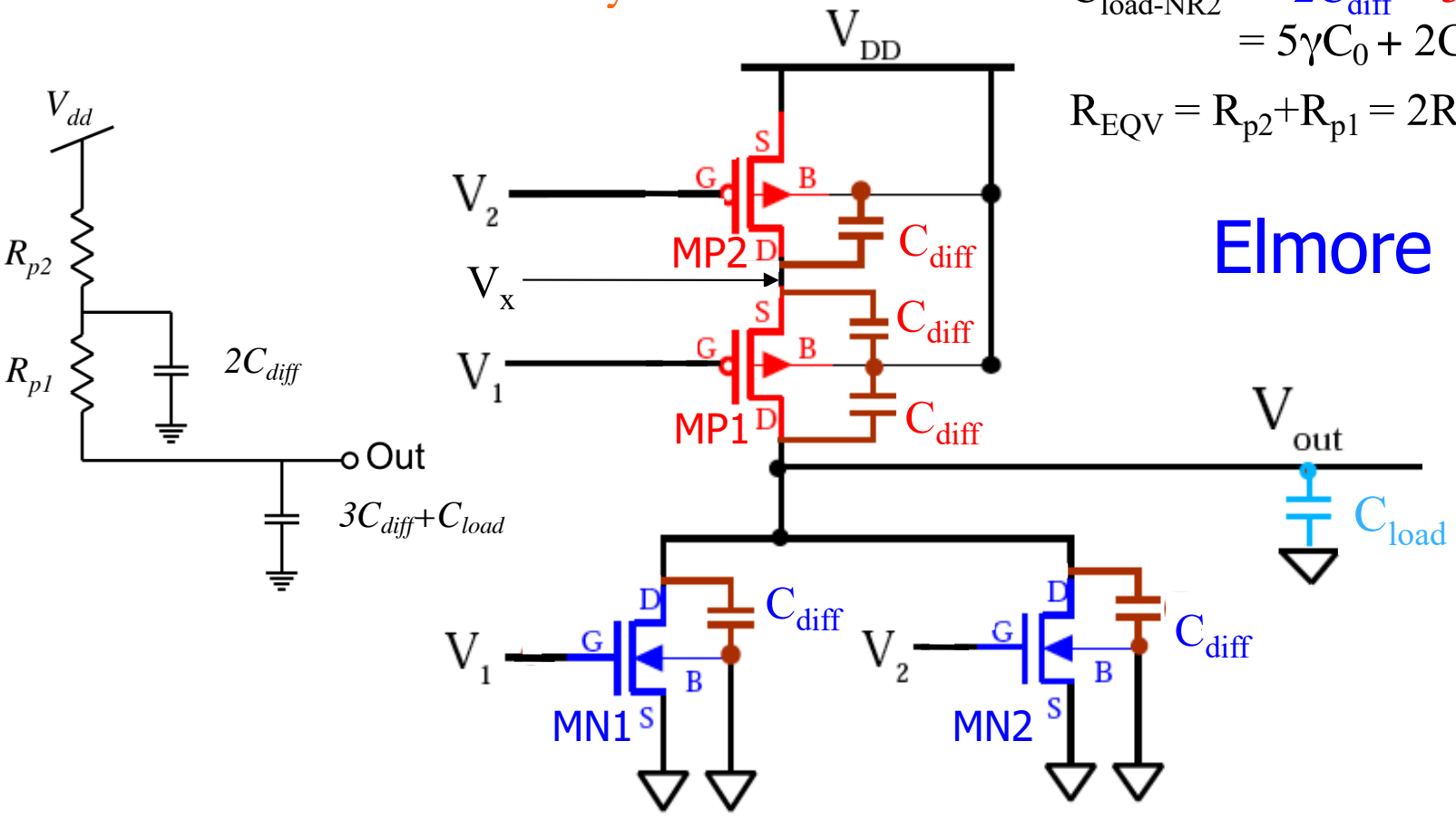


Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

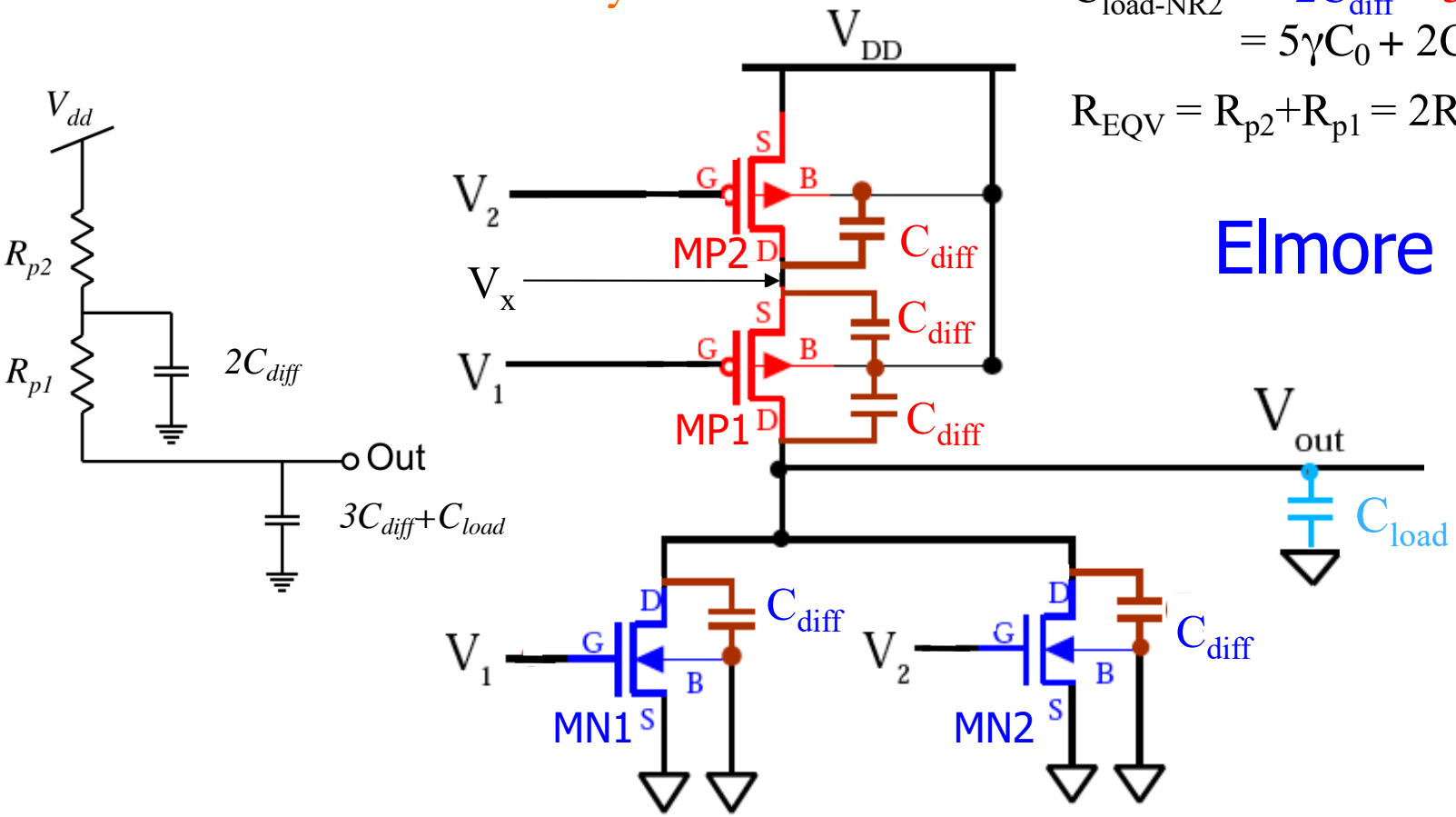
NOR2 Delay

- Worst case delay?

$C_{load-NR2} \approx 2C_{diff} + 3C_{diff} + C_{load}$
$= 5\gamma C_0 + 2C_0$

$R_{EQV} = R_{p2} + R_{p1} = 2R_0$

Elmore Model?

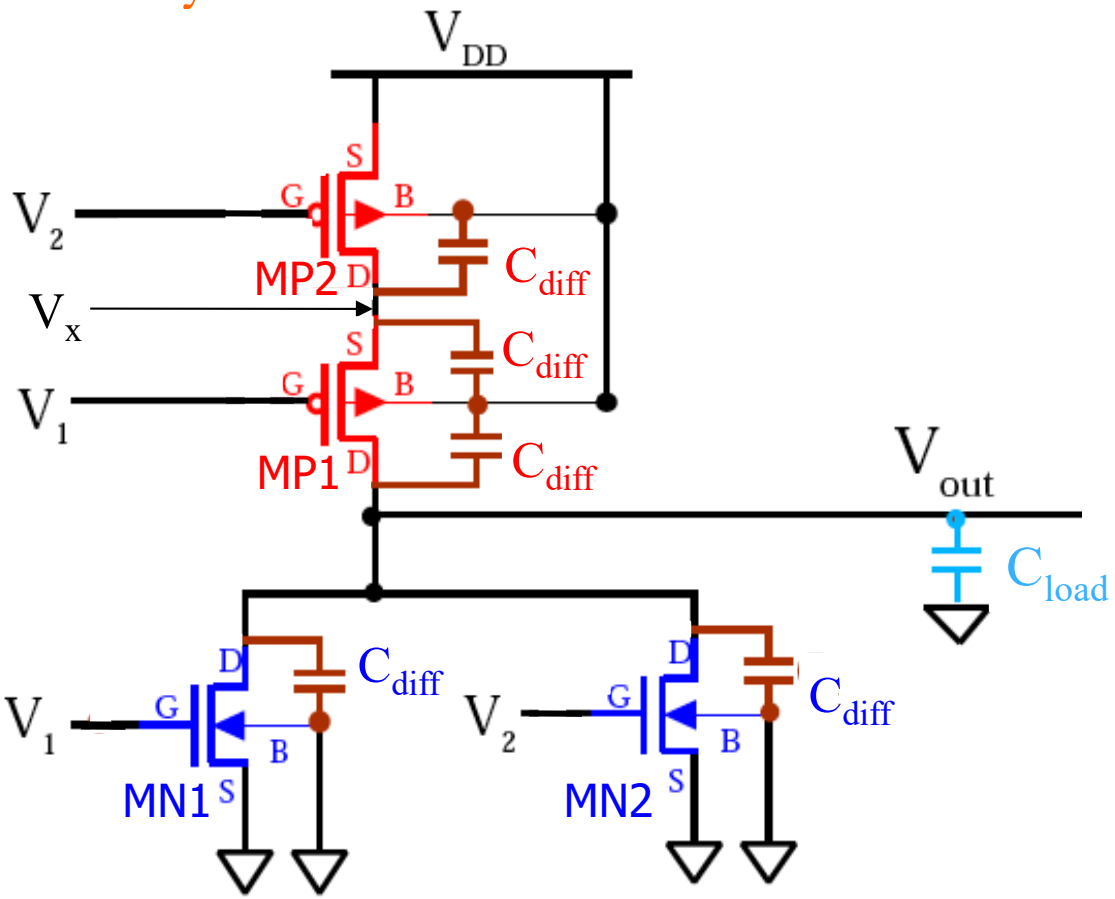


Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

$$delay = (2C_{diff})(R_{p2}) + (3C_{diff}+C_{load})(R_{p1}+R_{p2}) = (8\gamma+4)\tau$$

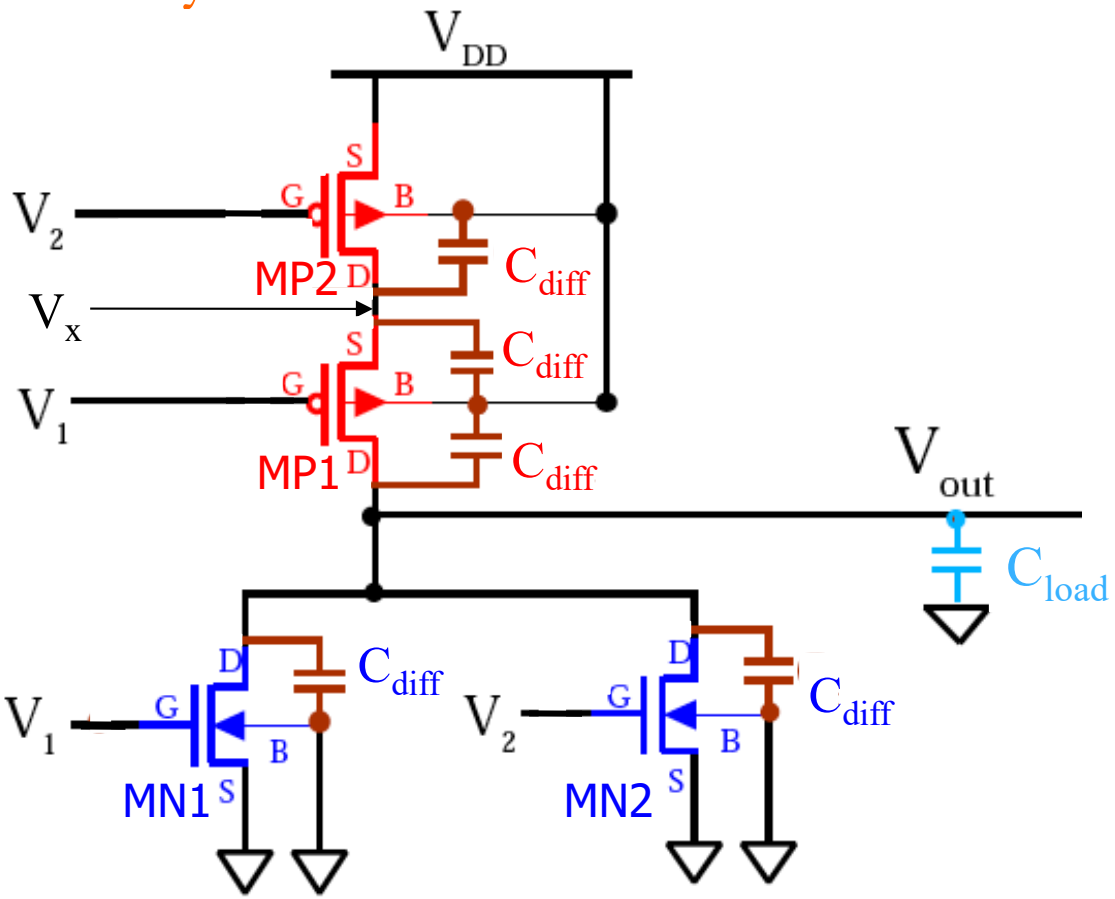
NOR2 Delay

- Worst case delay Pull-down?



NOR2 Delay

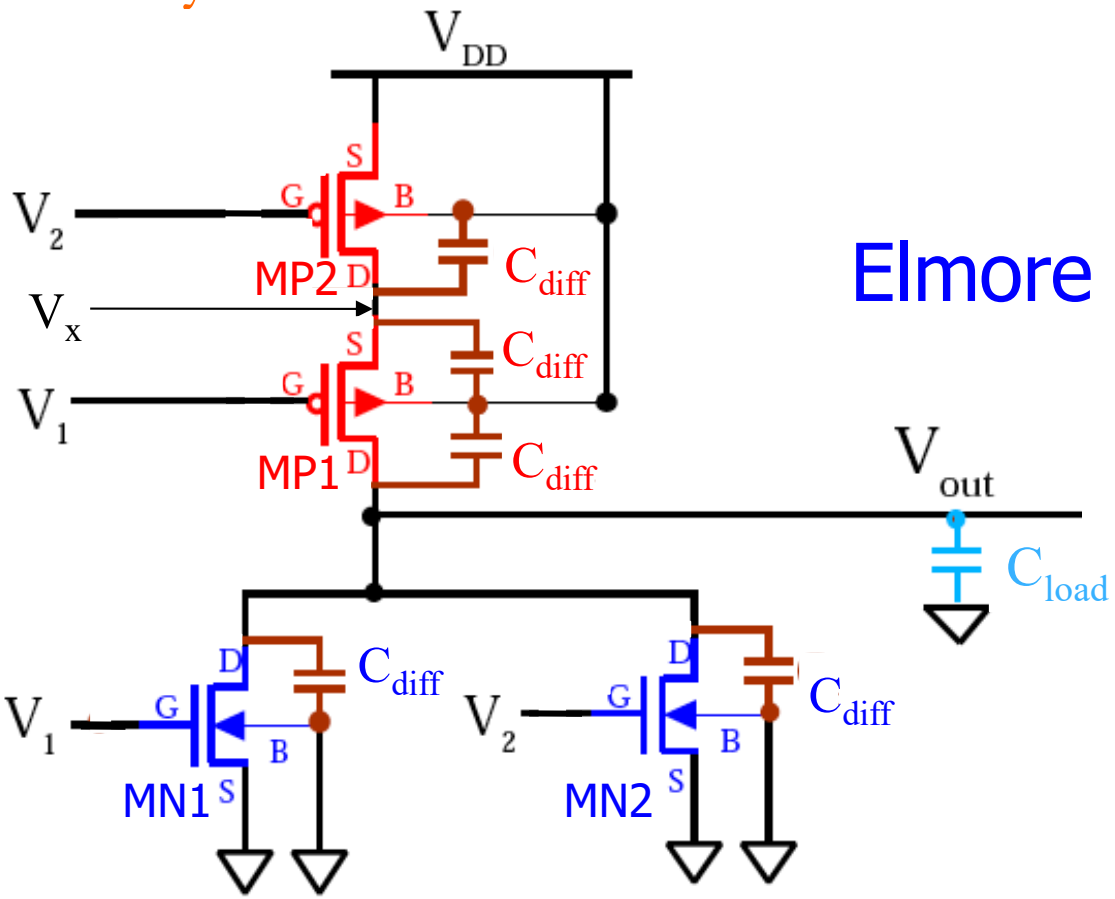
- Worst case delay Pull-down?



Worst case for Pull-down → $V_1 = 0$, $V_2 = 0$ ->V_{DD} @t=0 & $V_x \approx V_{out}=V_{DD}$-> 0

NOR2 Delay

- Worst case delay Pull-down?

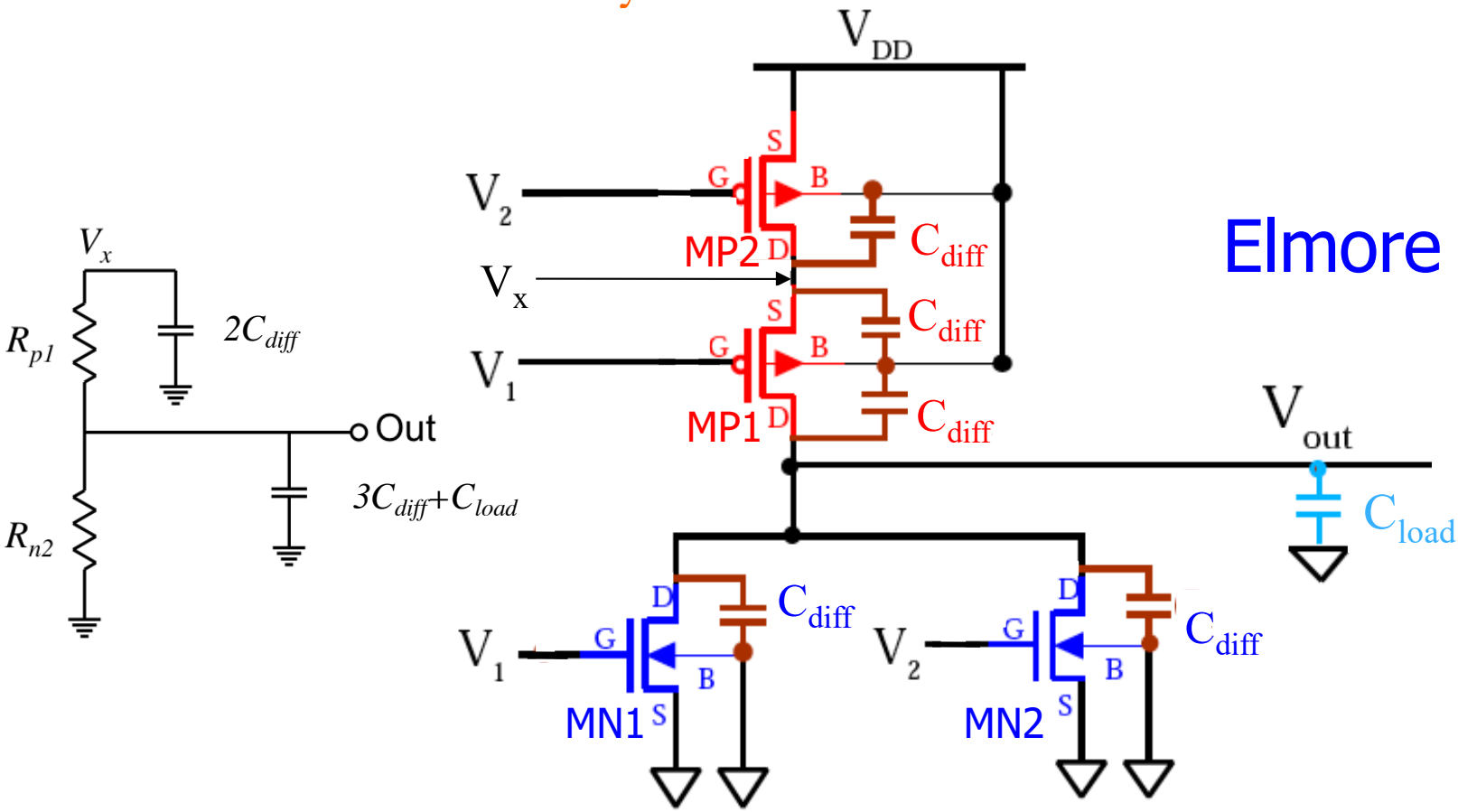


Elmore Model?

Worst case for Pull-down → $V_1 = 0$, $V_2 = 0$ ->V_{DD} @t=0 & $V_x \approx V_{out}=V_{DD}$-> 0

NOR2 Delay

- Worst case delay Pull-down?

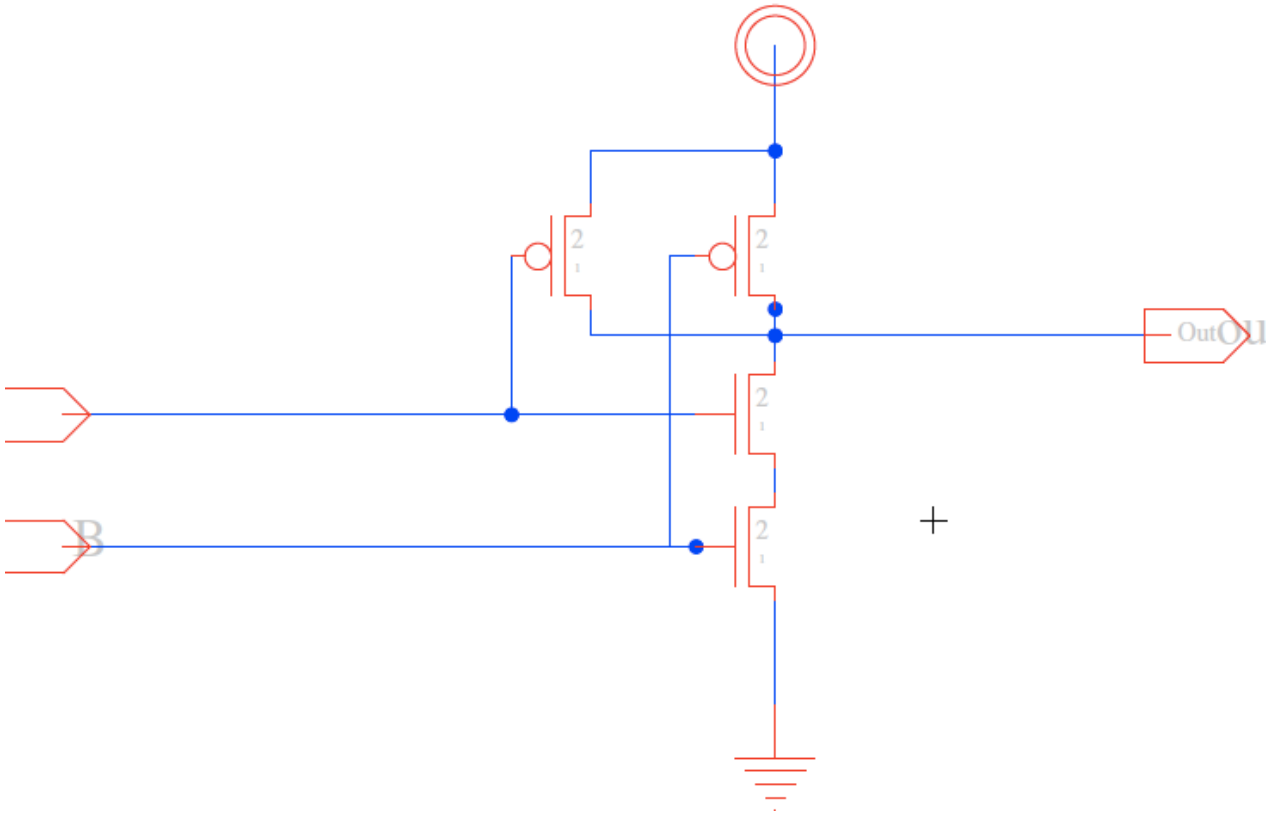


Elmore Model?

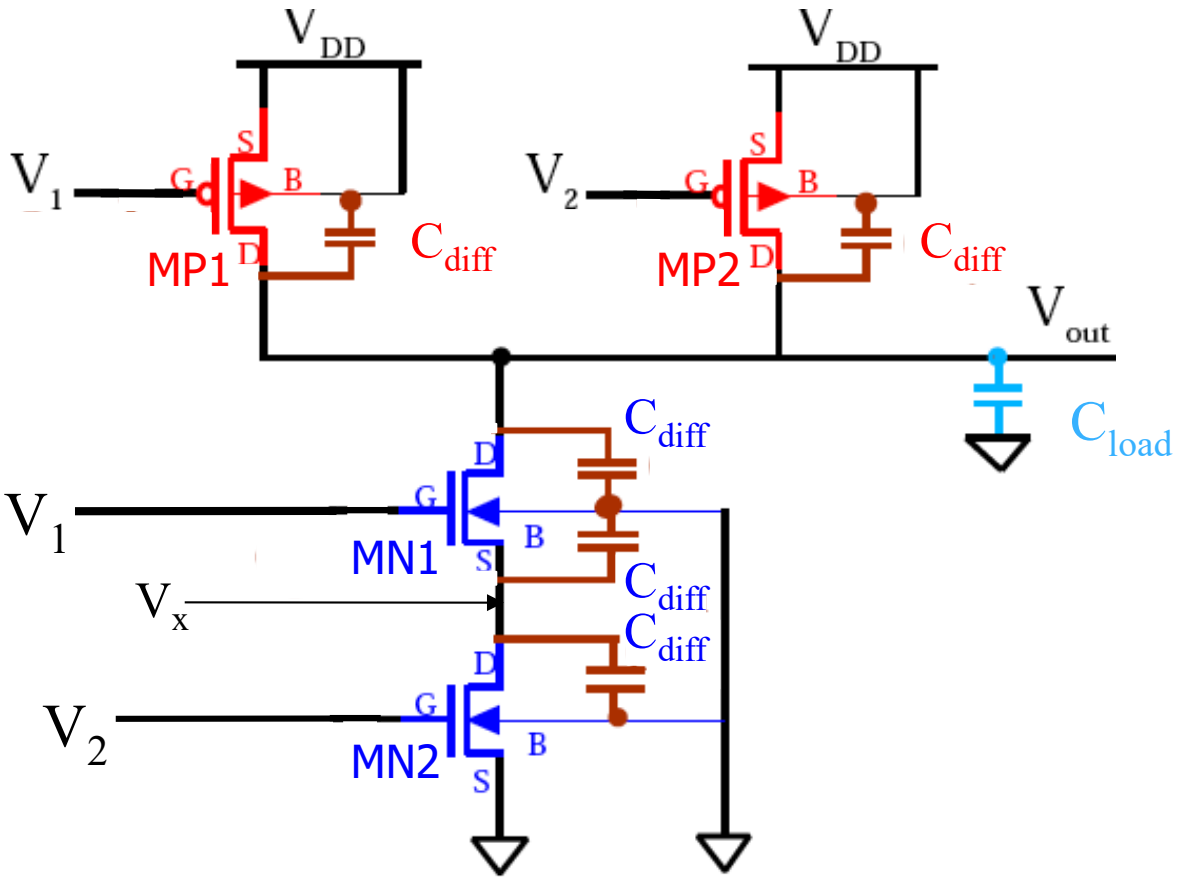
Worst case for Pull-down → $V_1 = 0$, $V_2 = 0$ -> V_{DD} @t=0 & $V_x \approx V_{out} = V_{DD}$-> 0

$$\text{delay} = (2C_{diff})(R_{p1}+R_{n2})+(3C_{diff}+C_{load})(R_{n2})=(7\gamma+2)\tau$$

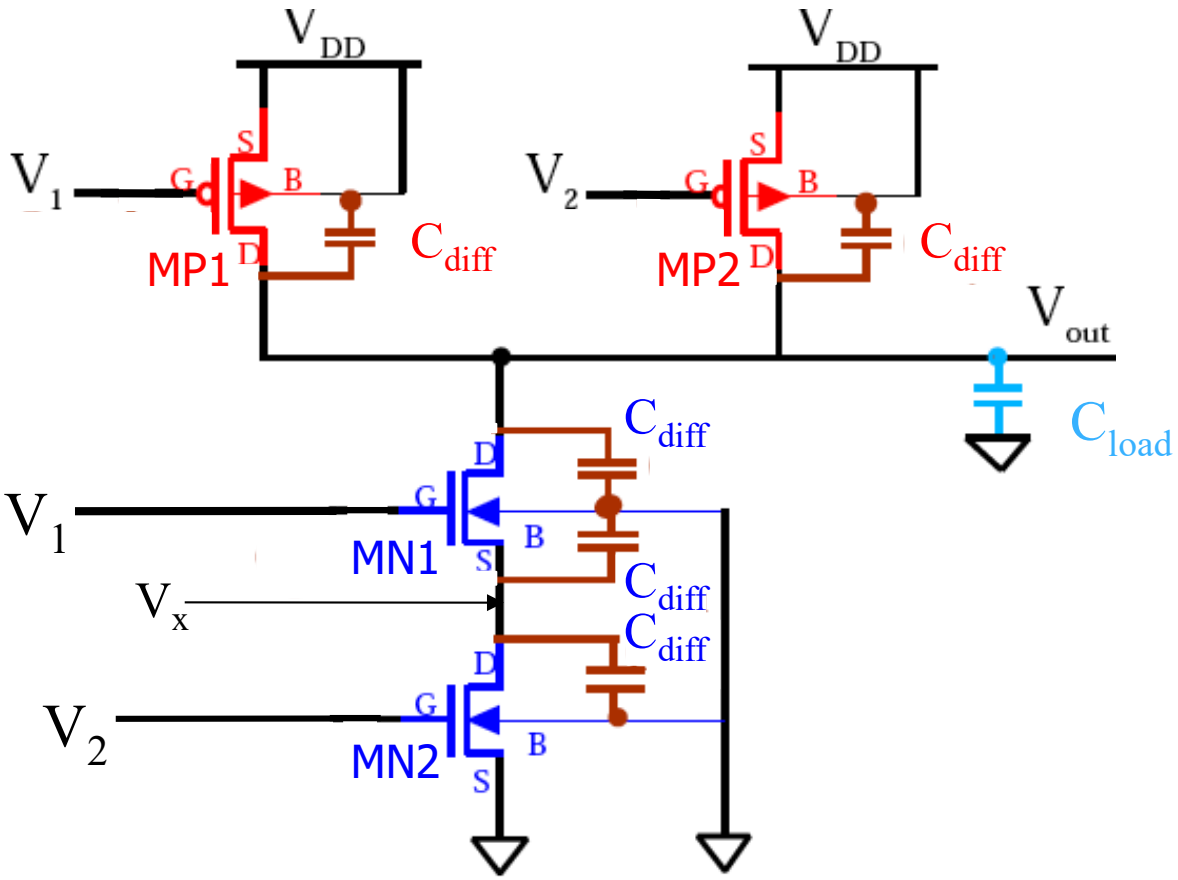
NAND2 Delay (preclass 2)



Parasitic Caps for NAND2 (worst case)

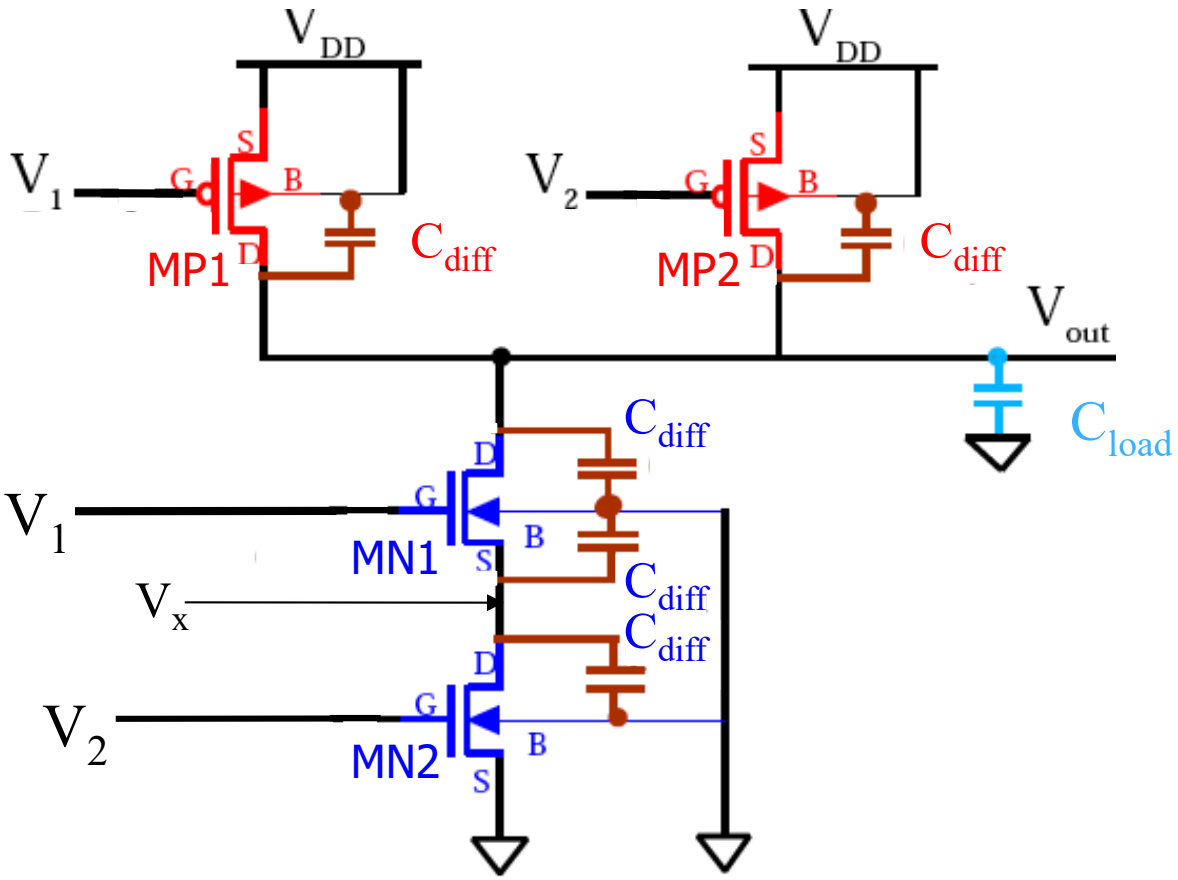


Parasitic Caps for NAND2 (worst case)



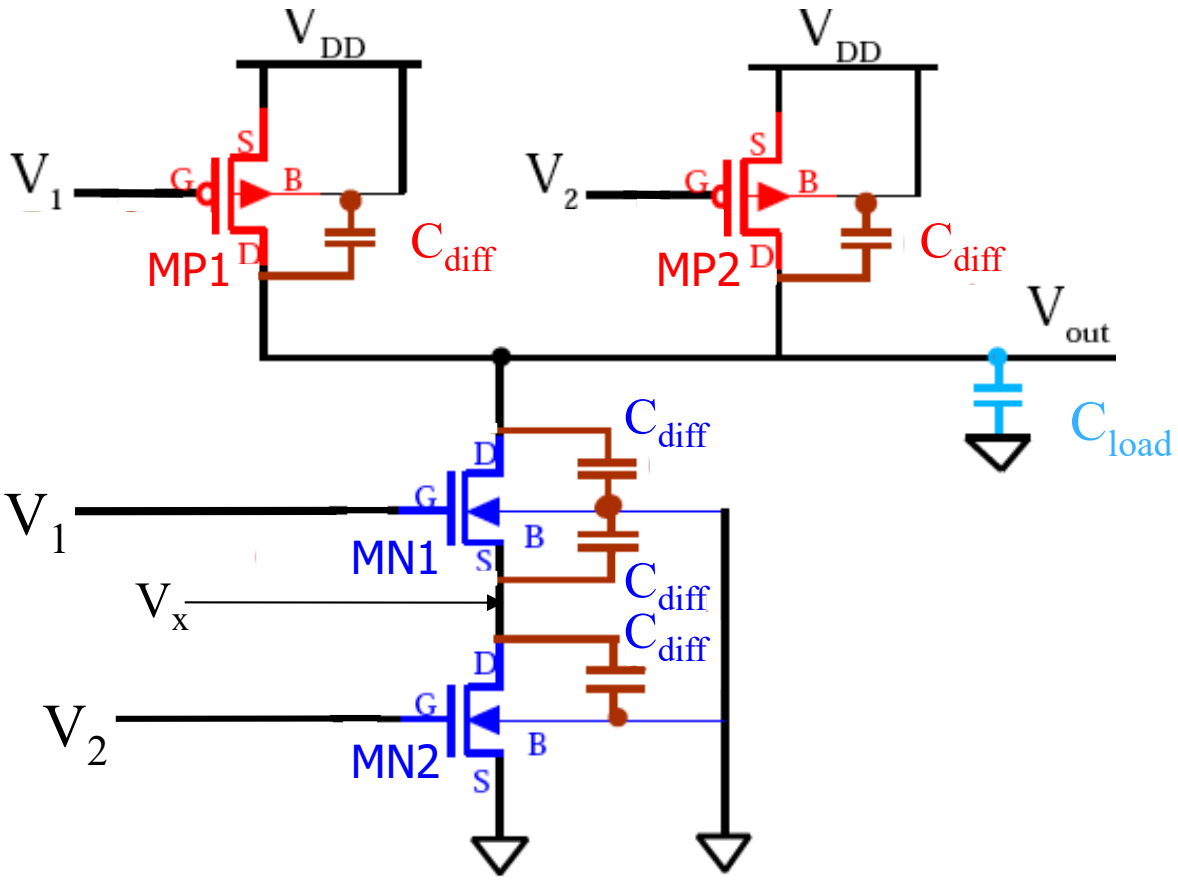
Worst case for Pull-up →

Parasitic Caps for NAND2 (worst case)



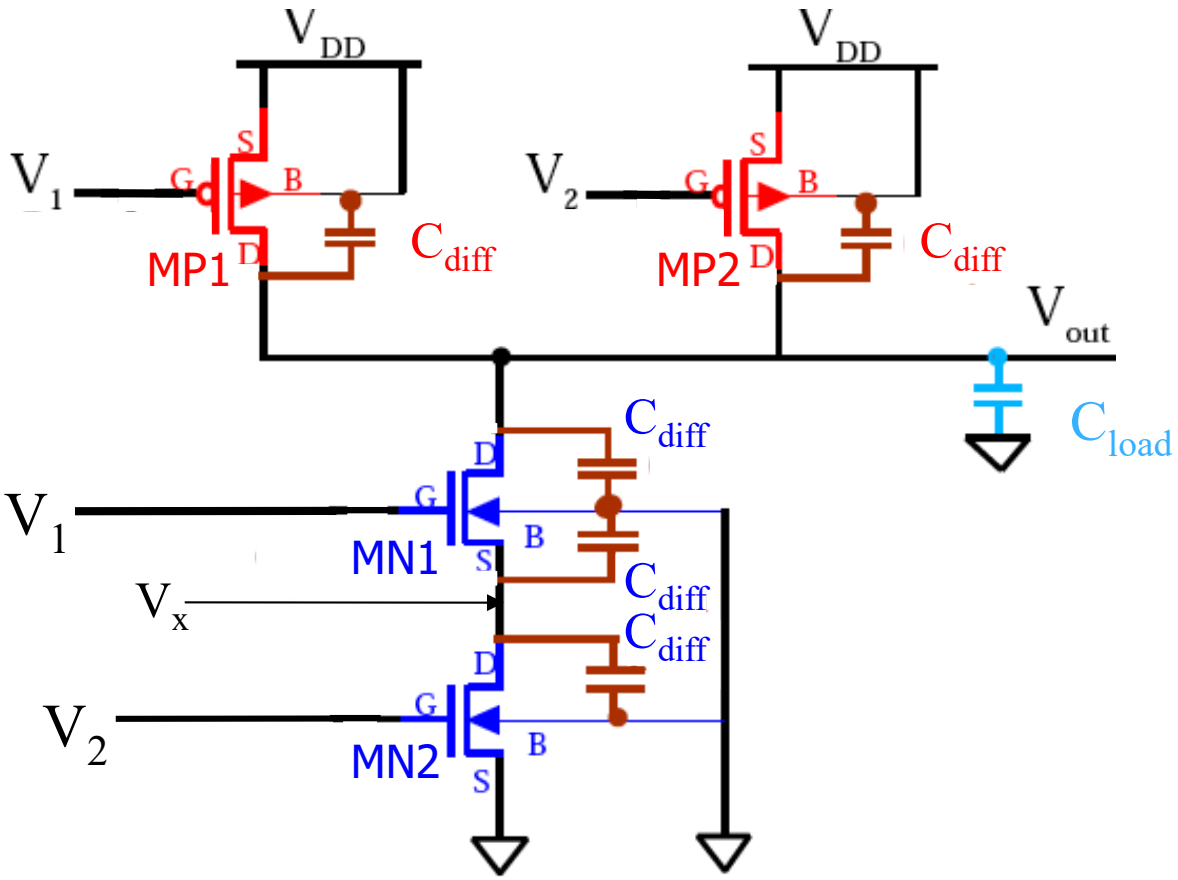
Worst case for Pull-up → $V_1 = V_{DD}$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ ->V_{DD}

Parasitic Caps for NAND2 (worst case)



Worst case for pull down →

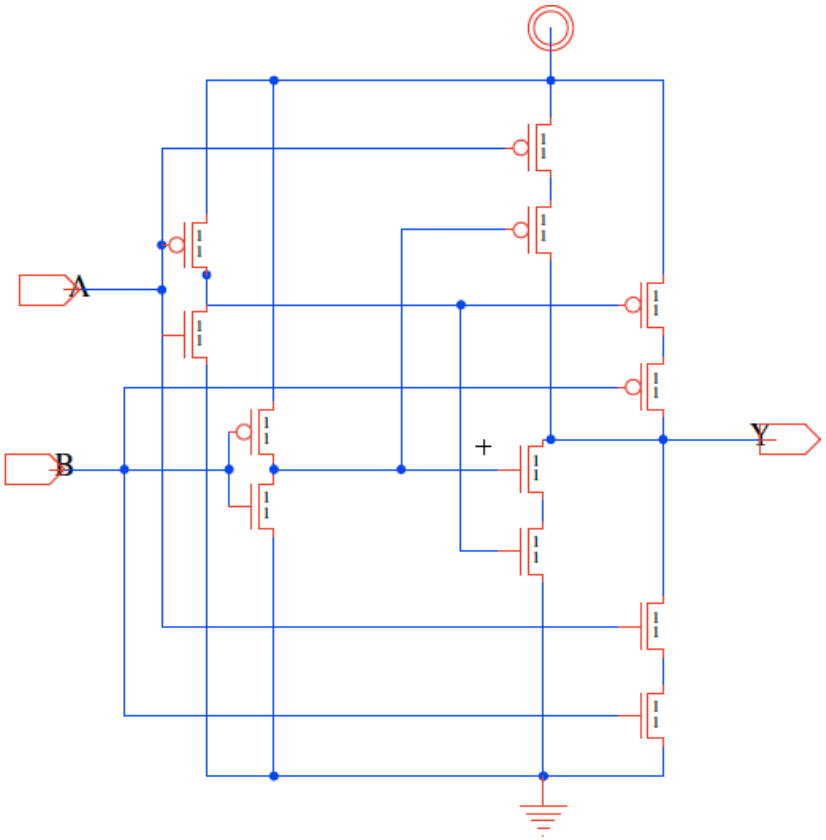
Parasitic Caps for NAND2 (worst case)

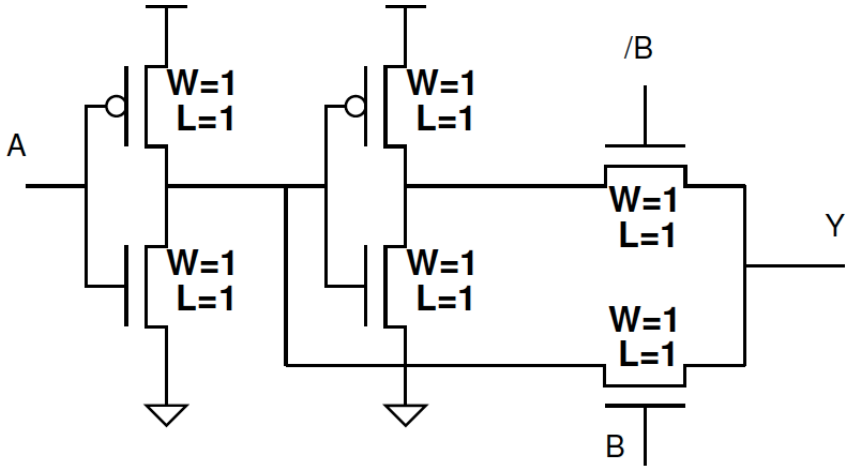


Worst case for pull down → $V_1 = V_{DD}$, $V_2 = 0 \rightarrow V_{DD}$ @t=0 & $V_x \approx V_{out} = V_{DD} \rightarrow 0$

CMOS XOR

- Delay with Cdiff>0?





Logic Types

- CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- Pass Gates
  - Implement logic gate as switch network for area and often delay win
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins (V_T drop)
    - Use level-restoring buffers to improve noise margins
- Dynamic logic … next time

Idea

- CMOS Logic
  - Complimentary dual pull-up/down networks
- There are other logic disciplines
  - We have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates static power in one mode
- Can use pass transistors for logic
  - Sometimes gives area or delay win

Admin

- Project 2 due tonight @ midnight
  - Leave time to write the report!
- Wednesday 11/3 Midterm 2 (next week)
  - 7-9pm DRLB 3C2
  - Lectures 1-22
  - Closed note, calculator allowed
  - All old exams online
    - focus on 2015-2019 ← taught in person by me
    - Study them!
  - Felicity review session
    - Monday 11/1, keep eye on Piazza

Admin: Midterm 2 Topics (up to Lec 22)

- Sizing
- Tau-model
  - Estimation and optimization
- Elmore-delay
  - Estimation and optimization
- Energy and power
  - Estimation and optimization
  - Dynamic and static
- Logic
  - CMOS
  - Ratioed
  - Pass transistor
- Transistor
  - Regions of operation
  - Parasitic Capacitance Model

"idea" slides