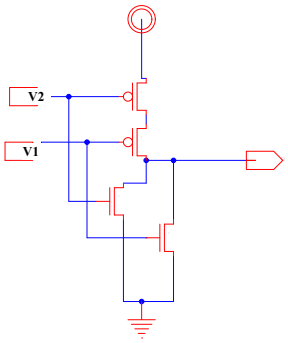
For this preclass we are going to analyze the worst case delays for a nor2 and nand2 gate with $C_{diff} \neq 0$. Assume each gate has minimum size transistors and is loaded with an identical gate.

1. First we will look at the CMOS NOR2 gate.



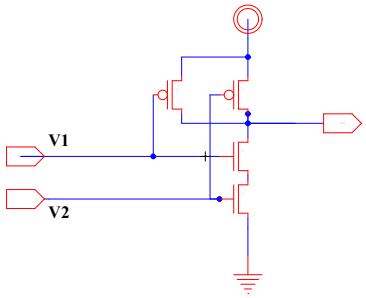
(a) What is the input switching case for the nor2 worst case rise time (i.e. pull-up delay)?

(b) What is the equivalent RC circuit? What is the τ estimate delay?

(c) What is the input switching case for the nor2 worst case fall time (i.e. pull-down delay)?

(d) What is the equivalent RC circuit? What is the τ estimate delay?

2. Next we will look at the CMOS NOR2 gate.



(a) What is the input switching case for the nand2 worst case rise time (i.e. pull-up delay)?

(b) What is the equivalent RC circuit? What is the τ estimate delay?

(c) What is the input switching case for the nand2 worst case fall time (i.e. pull-down delay)?

(d) What is the equivalent RC circuit? What is the τ estimate delay?