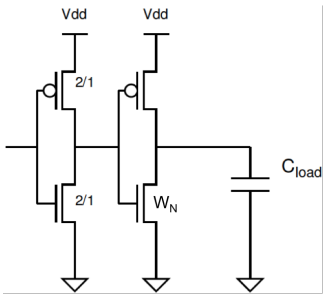
Today's Question: How do we drive a large load ($e.g.\ C_{load} = 4 \times 10^4 C_0$) with minimum delay? Detail buffer count and sizing.

Assume:

- velocity saturated sizing for gate drive; inverter sizing is: W_n=2, W_p=2
- Start with $C_{diff} = 0$ case (for simplicity)

1. If we had one inverter stage to size, how should it be sized?

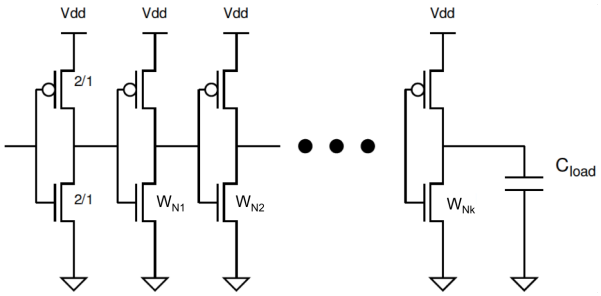


   (a) Write delay equation from $R_0/2$ drive through driving C_{load}.

   (b) Symbolic expression for delay-minimizing W_N.

   (c) Concrete size, W_N, for $C_{load} = 4 \times 10^4 C_0$.

2. If we had k inverter stages to size, how should the each be sized?



   (a) Write delay equation.

   (b) Symbolic expression for delay-minimizing W_{Ni}.

   (c) Symbolic expression for total delay using solution above.

3. What number of stages, N, minimizes total delay?

   (a) Expression to minimize total delay.

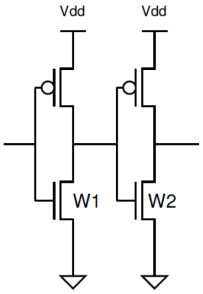
   (b) Solve for k.

   (c) What is the stage size relation at the optimal k?

   (d) What is the stage count for $C_{load} = 4 \times 10^4 C_0$?

   (e) What is the minimum delay for $C_{load} = 4 \times 10^4 C_0$?

4. If $C_{diff} = \gamma C_{gate}$, what is the stage delay for a $W1$ inverter driving a $W2$ inverter?



5. How does optimal stages and buffering change if we include $C_{diff} = \gamma C_{gate}$?

   (a) Write delay equation.

   (b) Symbolic expression for delay-minimizing W_{Ni}.

   (c) Compare with $C_{diff} = 0$ ($\gamma = 0$) case above.

   (d) Symbolic expression for total delay.

   (e) What is the optimal stage size relation when $\gamma \geq 0$?

   (f) For what γ are the following the optimal ρ?

   (**Hint:** solve for γ in terms of ρ)

ρ	γ
3	
4	