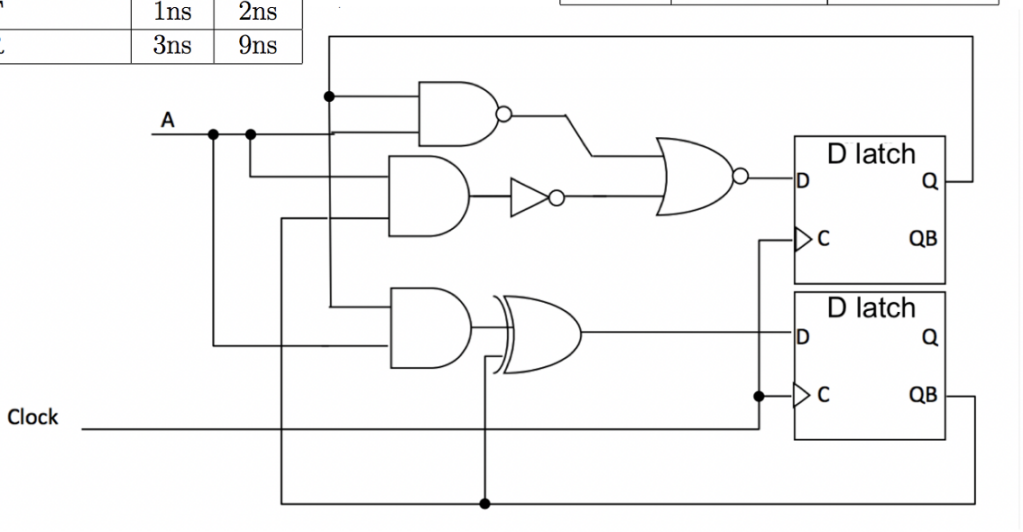
	Min	Max
OR/AND	3ns	5ns
NOR/NAND	2ns	4ns
NOT	1ns	2ns
XOR	3ns	9ns

Latch:		Min	Max
	Clock to Q	2ns	3ns
	Setup time	7ns	
	Hold time	6ns	



1. Timing Constraints:

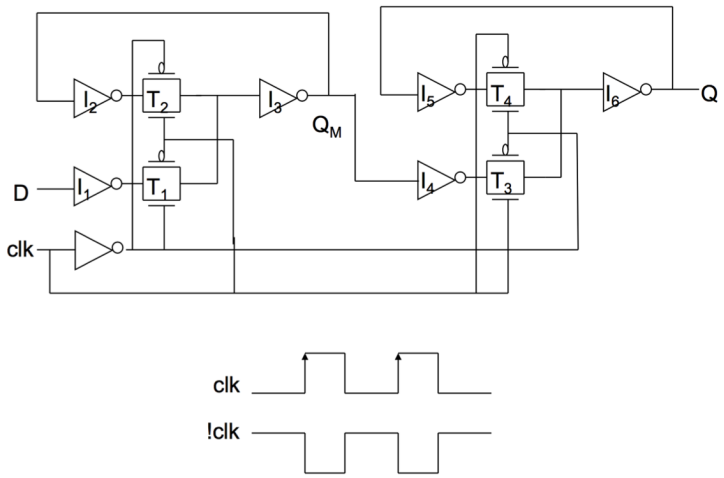
$$T \geq t_{c-q} + t_{plogic} + t_{su} \quad (1)$$

$$t_{cdregister} + t_{cdlogic} \geq t_{hold} \quad (2)$$

(a) What is the minimum clock period, T, that ensures correct operation?

(b) Add inverter pairs to the design above such that there are no hold time variations.

2. Below is a register built with two latches built from transmission gate muxes cascaded together controlled by non-overlapping clocks.



(a) Is this a positive or negative edge-triggered register?

Assume propagation delays are $t_{pd,inv}$ and $t_{pd,tx}$ and the inverter delay to drive $\overline{clk}$ is 0.

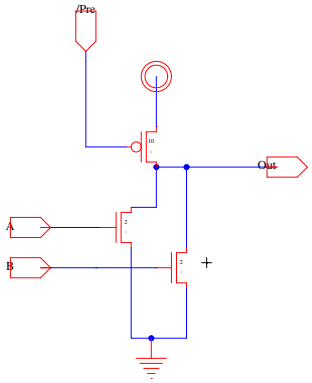
(b) What is the setup time for the register?

(c) What is the CLK→Q propagation delay?

(d) What is the hold time?

Assume: velocity saturated, $R_0/2$ sizing for gate drive; inverter sizing is: W_n=W_p=2

3. Consider:



(a) if A=B=0 and /pre is 0, what voltage does Out hold?

(b) if /pre switches from 0 to 1, and A=B=0, what voltage settles on Out?

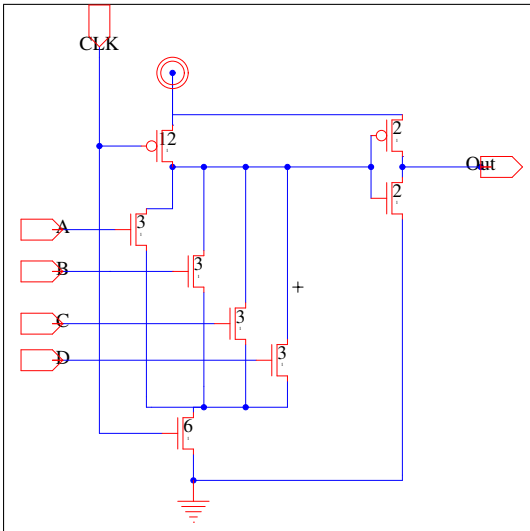
(c) if /pre is at 1 and, B switches from 0 to 1 what voltage settles on Out?

(d) What are the sizing constraints on the NMOS devices (compare to ratioed logic)?

(e) What concerns might we have with this logic?

(f) What requirements must we satisfy for correct operation?

4. Determine delays (express in τ units in terms of γ):

	Precharge	Drive Input	Drive Inv. and Self Output
	(pullup transistor charging inverter)		
	—	Input	Self Output Delay